Mixed ESL Power/Performance Estimation using SystemC/TLM2.0 Modeling and PwClkARCH Library

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SECURE CONNECTIONS
FOR A SMARTER WORLD

Agenda

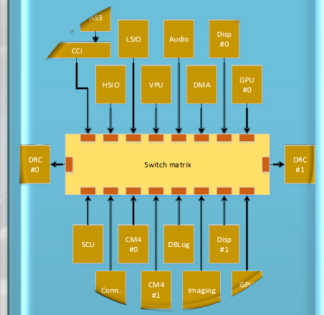
Automotive Multimedia

Context

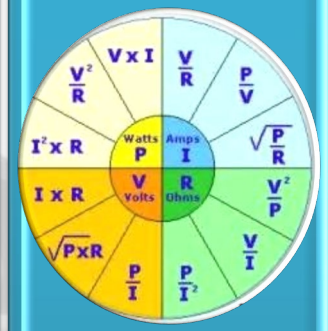
Early stage power estimation

PwrClkARCH

Power and Clock Intent definition



Evaluation based on Interconnect subsystem



Simple multi-task use case and results

Summary & Outlook

Automotive multimedia

- Feel at home on the road
- Complex SoCs for simplification of in-car media entertainment and mobile devices connection
- Strong relation between Comfort and Power consumption
- Each Watt counts …

Context

Power-aware designs era

Increasing SoC performances?!

Great, but at what price?

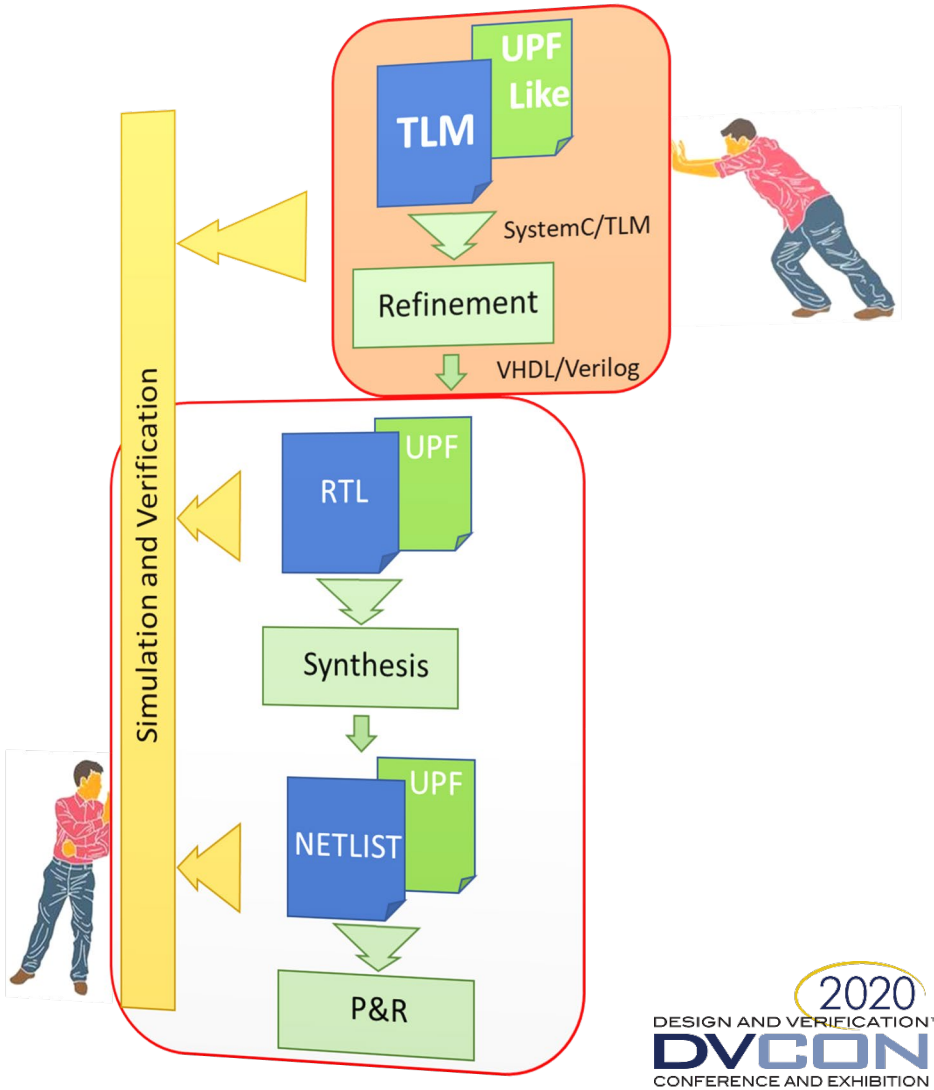
Insufficient early stage architecture investigation capabilities

- Architecture power waste
- Increased production cost and time-to-market period
- Architecture definition - tremendous Power/Perf trade-off impact

It is always good to make abstractions …

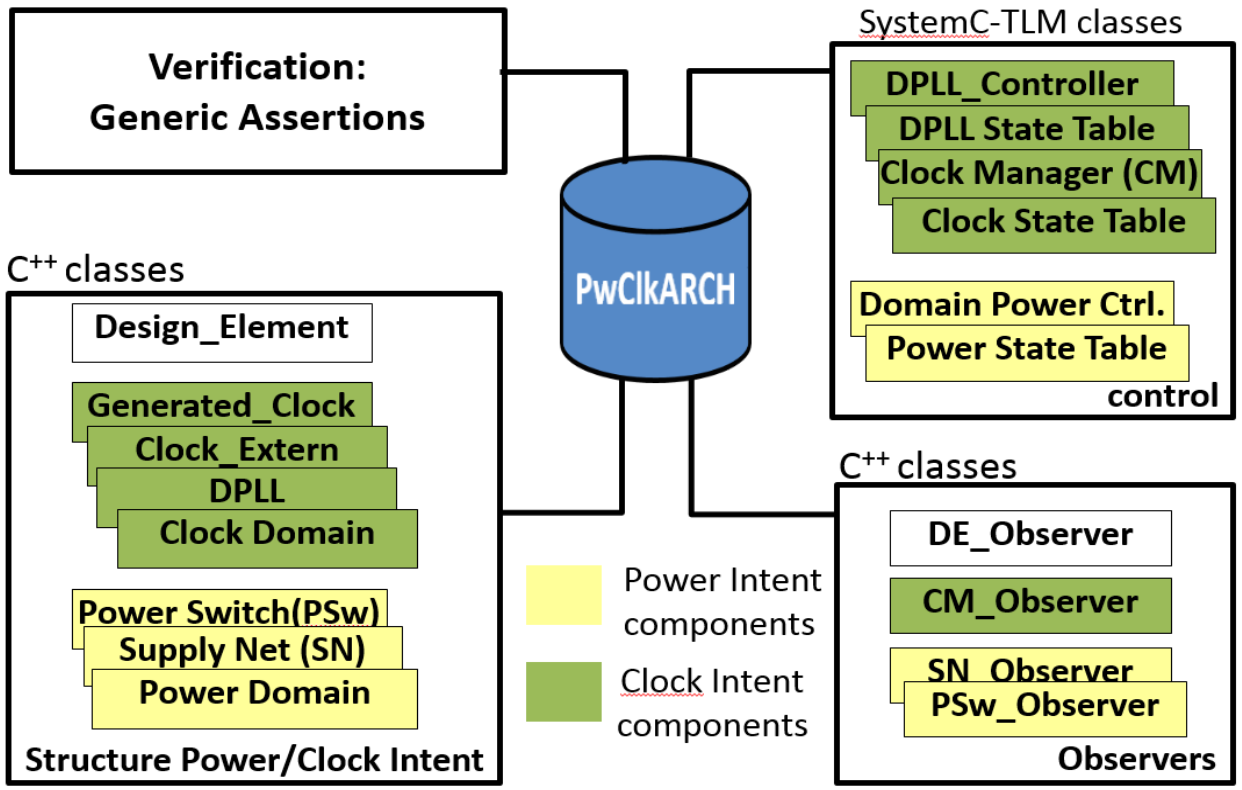
Early Stage power estimation

- **What?**
  - *Power estimation in the very first stages of Design Flow (before RTL)*
  - *DYNAMICALLY estimate power on complex use cases*
- **Why?**
  - *Study different architecture options from beginning*
  - *Creating references for developers*
  - *Catching/Avoiding bugs earlier in the flow*
  - *Reduce design iterations*
- **How?**
  - *High-Level Virtual Prototyping using SystemC/TLM2.0 for behavioral/communication model*
  - *Using PwClkARCH library for power intent description*



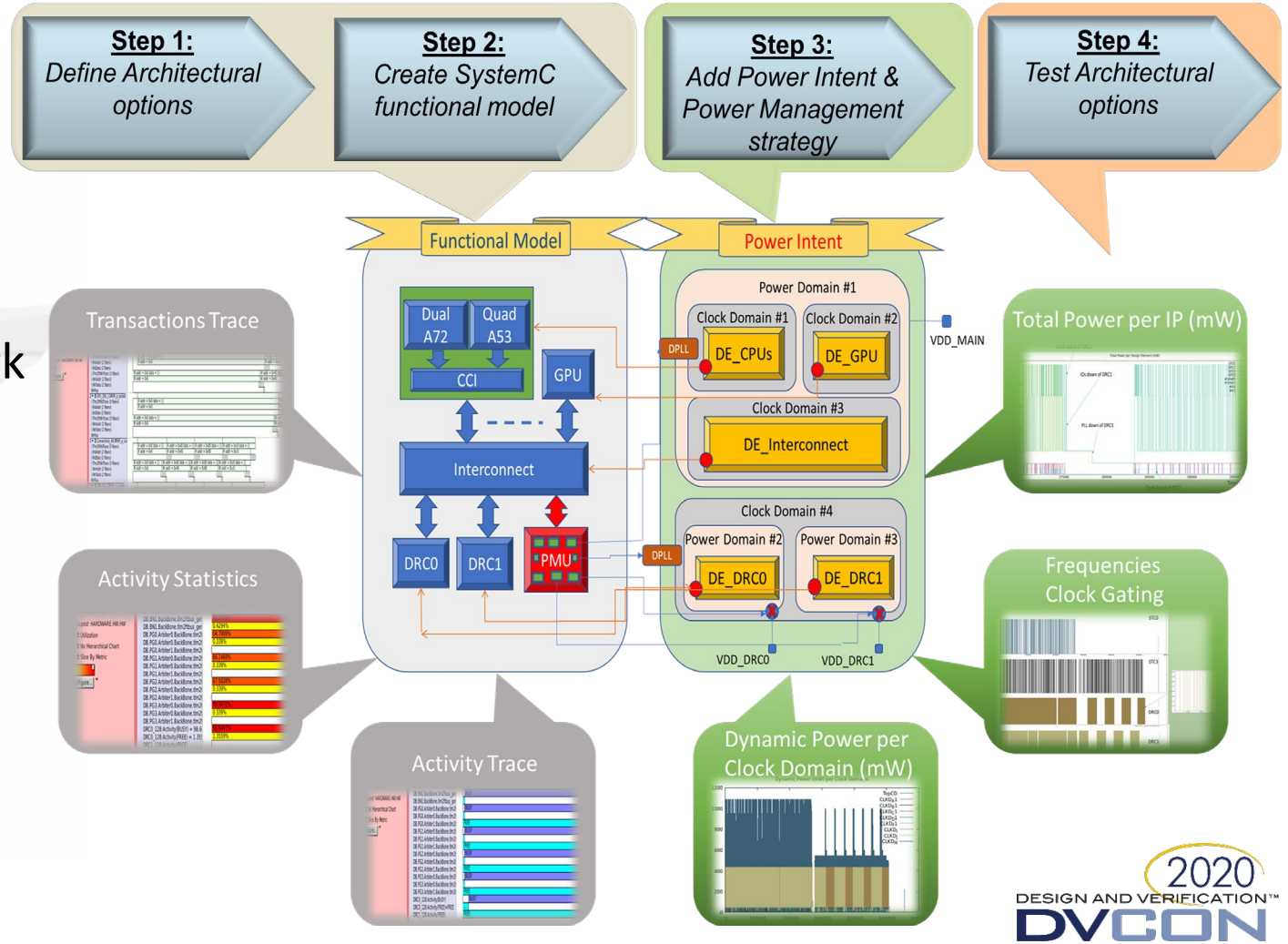
PwClkARCH - semantics

- C++ classes and SystemC/TLM modules
- UPF-based high-level approach
  - Design elements, power state table, power switches, supply nets
- Added clock tree description
  - External clocks, generated clocks, DPLLs, clock state table, clock managers
- Power and Clock domains
- Power management
  - OPP Table, Clock gating, Auto clock gating, Power gating, DVFS



PwClkARCH - power management and estimation

- **Advantages**:
  - Functional model / Power intent separation
  - Parallel DYNAMIC Co-simulation
  - Mixed Perf/Power estimation framework
  - Test power reduction technics **early in the flow –** (Power/Clock gating, DVFS)
- **Other existing solutions**
  - not easily applicable and they lack of precise power reduction technics mechanisms at high abstraction level.



Simple example

1

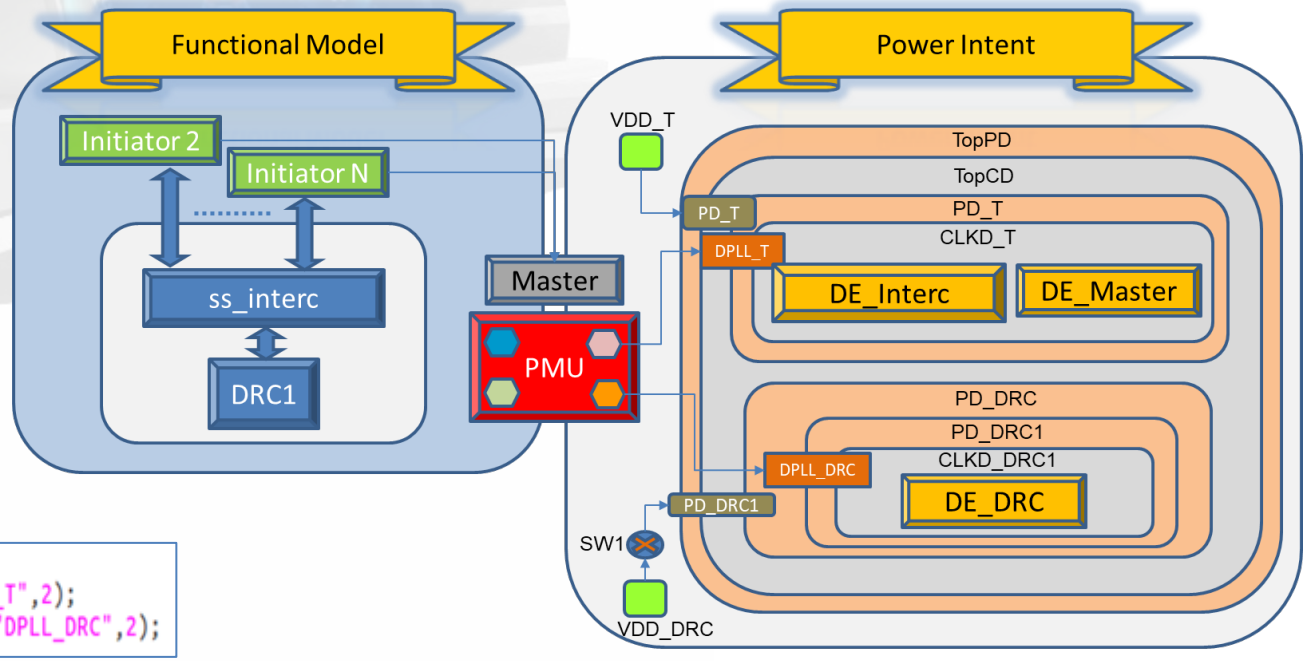
```
//Create Clock Domains
Clock_Domain* TopCD = new Clock_Domain(NULL,"TopCD","TOP");
Clock_Domain* CLKD_T = new Clock_Domain(TopCD,"CLKD_T","TOP/CLKD_T");
Clock_Domain* CLKD_DRC1 = new Clock_Domain(TopCD,"CLKD_DRC1","TOP/CLKD_DRC1");
```

2

```
//Create Power Domains
Power_Domain* TopPD = new Power_Domain(NULL,"TopPD","top");
Power_Domain* PD_T  = new Power_Domain(TopPD,"PD_T","top/T");
Power_Domain* PD_DRC  = new Power_Domain(TopPD,"PD_DRC","top/DRC");
Power_Domain* PD_DRC1 = new Power_Domain(PD_DRC,"PD_DRC1","top/DRC/DRC1");
```

3

```
//Design Elements
Design_elem* DE_Interc  = new Design_elem (CLKD_T,     PD_T,   (top->ss_interc),     INTERC_CAPACITANCE,     INIT_ACTIVITY,  INTERC_LEAKAGE_RESITANCE);
Design_elem* DE_Master  = new Design_elem (CLKD_T,     PD_T,   (top->master),        0*(std::pow(10,-12)),   0.0,            10e6                    );
Design_elem* DE_DRC     = new Design_elem (CLKD_DRC1,  PD_DRC, (top->ss_drc1),       DRC_CAPACITANCE,        INIT_ACTIVITY,  DRC_LEAKAGE_RESITANCE   );
```



4

```
//Create DPLLs
DPLL* DPLL_T = new DPLL (CLKD_T,"DPLL_T",2);
DPLL* DPLL_DRC = new DPLL (CLKD_DRC1,"DPLL_DRC",2);
```

5

```
//Power switches
Power_Switch* SW1 = new Power_Switch (PD_DRC1,"SW1",2);
(SW1->_input_supply_nets).push_back(VDD_DRC);
SW1->SetOutput_supply_net(VDD_DRC1);
```

Tables

```
//Power state table - PST
S1.create_pst   ("PST_top",TopPD,              "3"    ,"VDD_T",       "VDD_DRC",      "VDD_DRC1" );
S1.add_pst_state("PST_top","PST1-All_ON",      "3",    "ON_H",        "ON",           "ON");// #1
S1.add_pst_state("PST_top","PST3-DRC1_OFF",    "3",    "ON_L",        "ON",           "OFF");// #2

//Power states legal transitions
PSTrans* Tr = new PSTrans("PST_top","*","*");
```

State	VDD_T	VDD_DRC	VDD_DRC1
ALL_ON	ON_H	OFF	ON
DRC_OFF	ON_L	ON	OFF

```
//Create external clocks
Clock_Externe* Clk_T_R = new Clock_Externe("Clk_T_R","reference",DPLL_T, 24*(std::pow(10,6)));
Clock_Externe* Clk_T_B = new Clock_Externe("Clk_T_B","Bypass",DPLL_T, 32*(std::pow(10,3)));
Clock_Externe* Clk_DRC1_R = new Clock_Externe("Clk_DRC1_R","reference",DPLL_DRC1,24*(std::pow(10,6)));
Clock_Externe* Clk_DRC1_B = new Clock_Externe("Clk_DRC1_B","Bypass",DPLL_DRC1,32*(std::pow(10,3)));
```

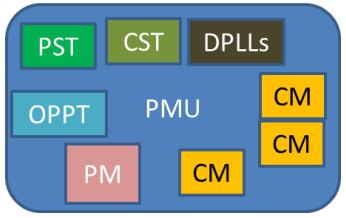
```
//Clock States Table - CST
S2.create_clkst("CLKST_top", TopCD,           "2"  ,"CK_CM_CLKD_T_DE_Interc", "CK_CM_CLKD_T_DE_Master", "CK_CM_CLKD_DRC1_DE_DRC1" );
S2.add_clkst_state("CLKST_top","CST1-All_ON",   "2",          "4",                    "4",                    "4"                 );// #1
S2.add_clkst_state("CLKST_top","CST2-DRC1_OFF", "2",          "4",                    "4",                    "0"                 );// #2
```

State	CLKD_divider	CLKD _Master_divider	CLKD_DRC _divider
ALL_ON	4	4	4
DRC_OFF	4	4	0

```
//OPP Table
S2.create_OPP_table     ("OPPtable", TopCD, TopPD,      "3",    "DPLL_T",       "DPLL_DRC",     "index");
S2.add_OPP_state        ("OPPtable",    "OPP1-All_ON",  "3",    "600,4",        "600,4",        "1,1"); // #1
S2.add_OPP_state        ("OPPtable",    "OPP2-DRC_OFF", "3",    "600,4",        "600,4",        "2,2"); // #2
```

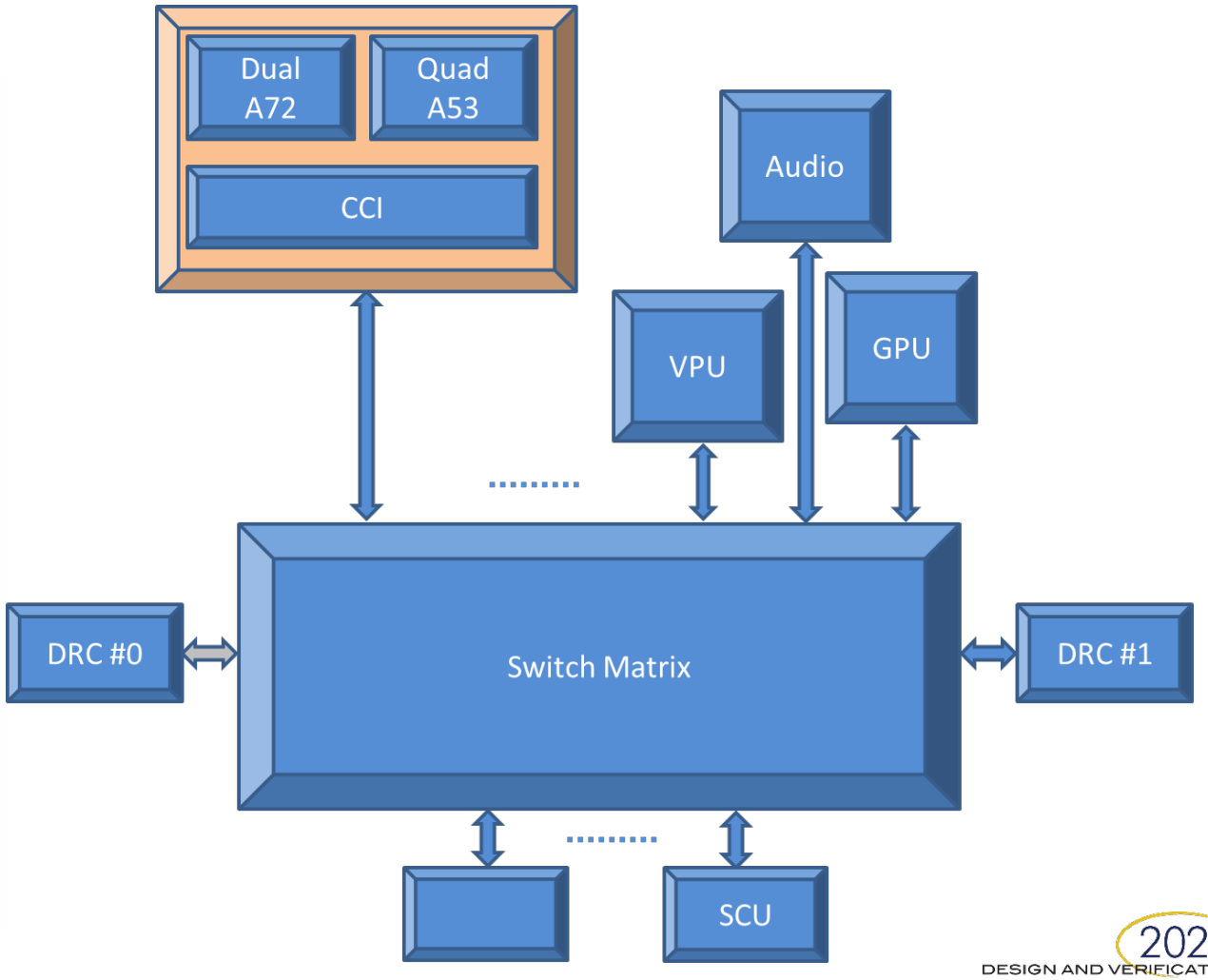
State	DPLL_T	DPLL_DRC	Index[PD:CD]
ALL_ON	600,4	600,4	1,1
DRC_OFF	600,4	600,4	2,2

```
// Create Power Management Unit (PMU)
ARK_IPs::PMU*   pmu = new ARK_IPs::PMU("PMU", TopPD->power_domains_list, pst, TopCD->clock_domains_list, clkst, DPLL_T->dpll_list, pOppTable);
```



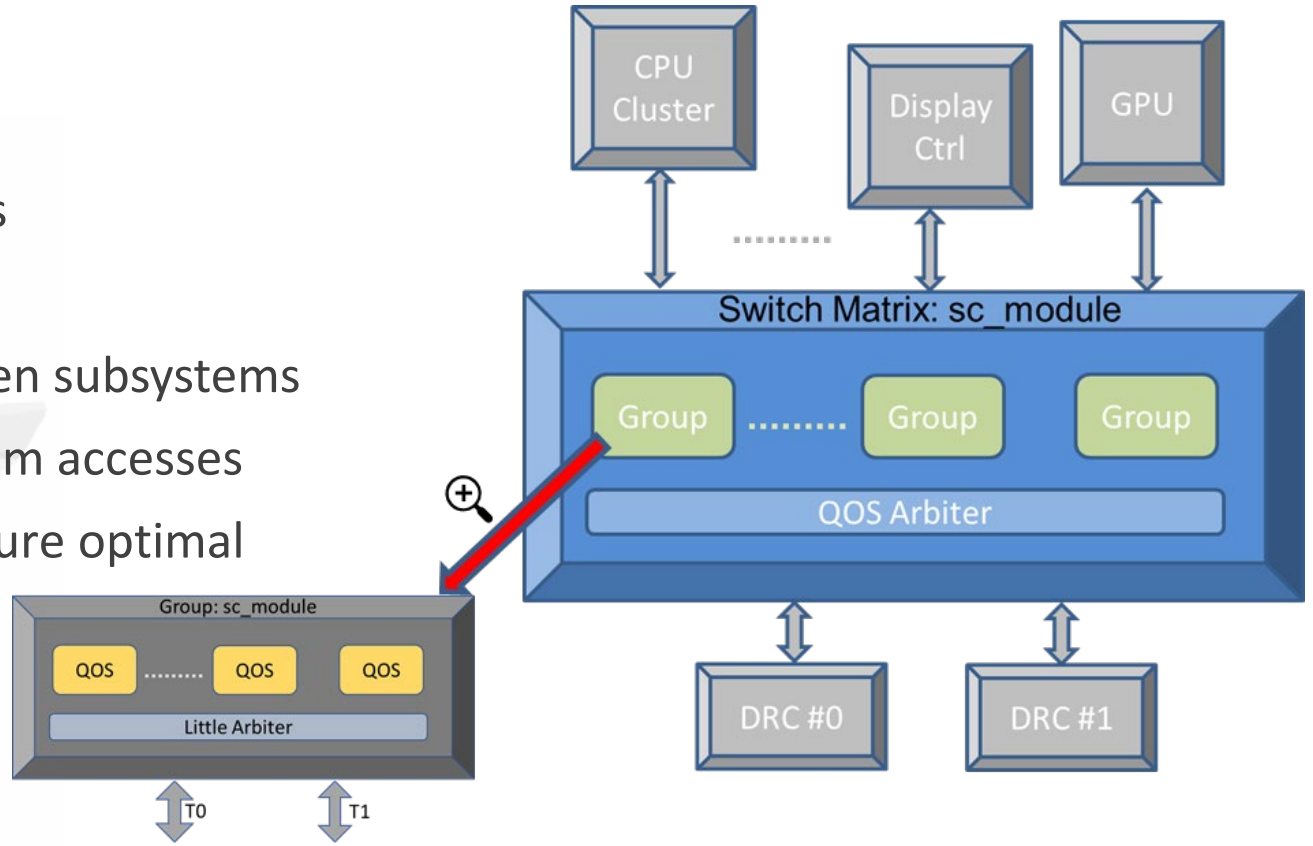
Evaluation - based on Interconnect subsystem

- Each device in i.MX8 family has:
  - 1x Switch matrix where all subsystems are plugged-in
    - Functional model is targeting both performance and power consumption
  - SCU (System Control Unit)
    - Handling reset, clock and power control
    - Those policies are modeled using PwClkARCH
  - 1x or 2x DRAM controller(s)
- All devices in i.MX8 family are following the same structure
  - Subsystems are scaled or replaced



Evaluation - based on Interconnect subsystem

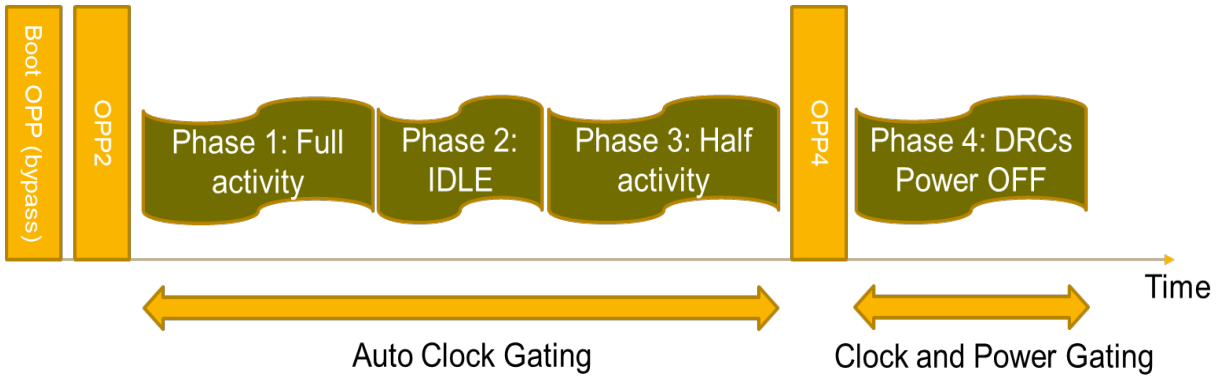
- Switch Matrix (SM)
  - Contains a large number of complex sub-blocks
  - Manages QoS of in-coming transactions
  - Apply Multi-level QoS based arbitration between subsystems
  - Handled interleaving to DRCs and routing system accesses
  - Executes multiple scheduling algorithms to assure optimal memory usage and performance



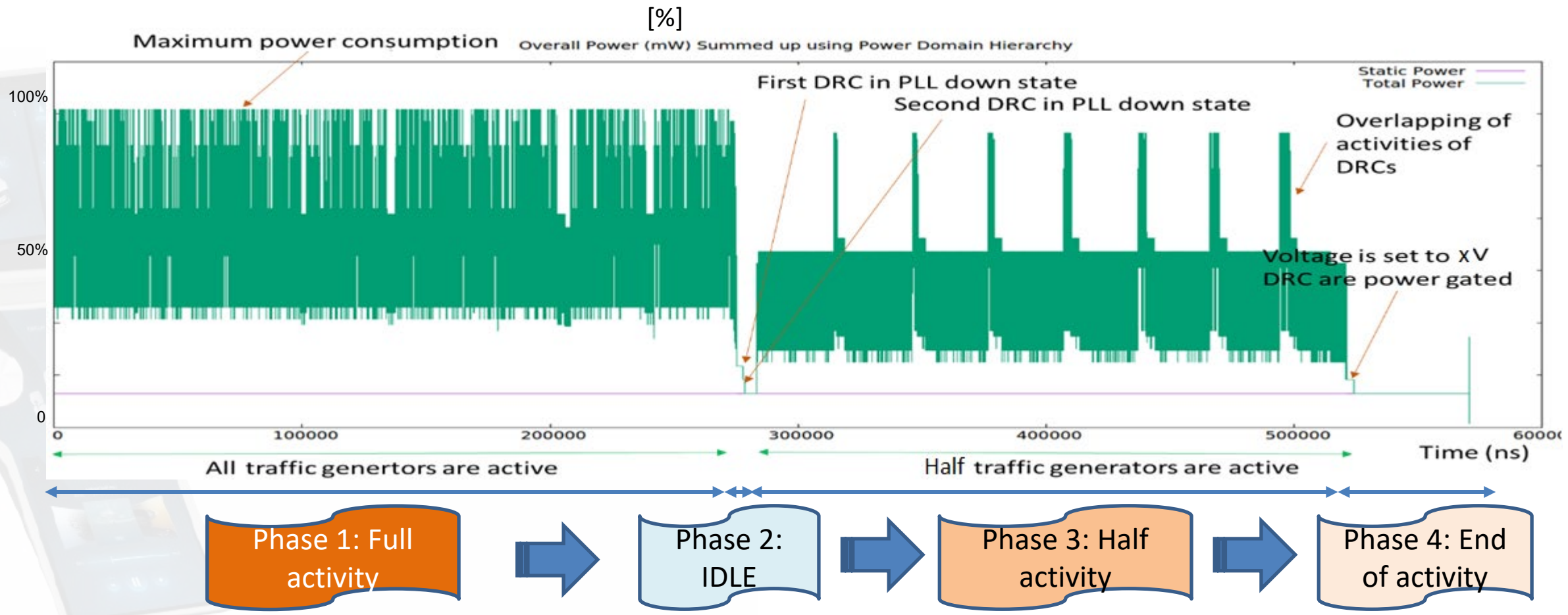
- = 1x voltage domain – low-power support
- ~ 5x power domain
- > 25 clock domains – HW auto clock gating

Simple multi-task use case - with power management

- **Full activity** – all Switch Matrix blocks and the 2 DRCs are active
- **IDLE** – no activity – clock gating (all clock domains in the Switch Matrix and those for DRCs)
- **Half activity** – half of the Switch Matrix is active and only 1 DRC is active at a time
- **Power OFF** – end of activity – Clock gating, Low-power mode for Switch Matrix and DRC power gating

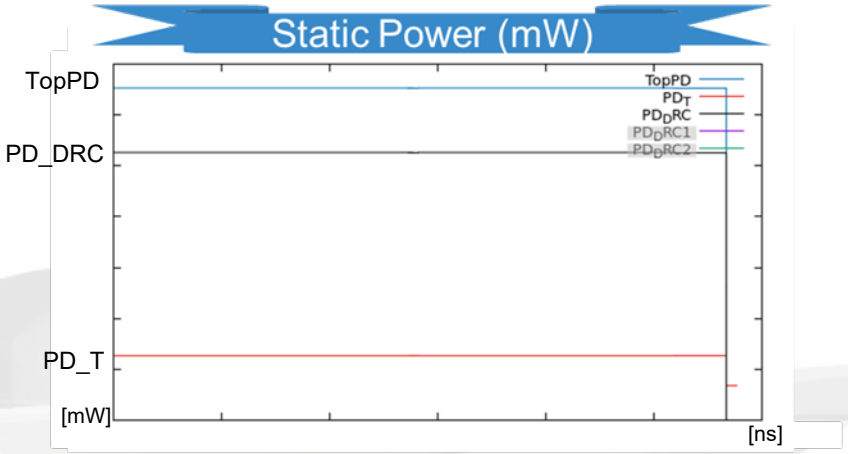


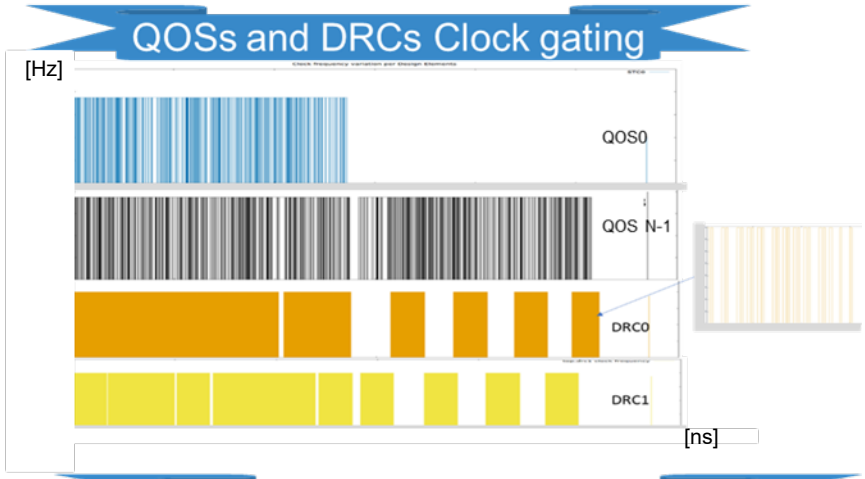
Results - Total Power

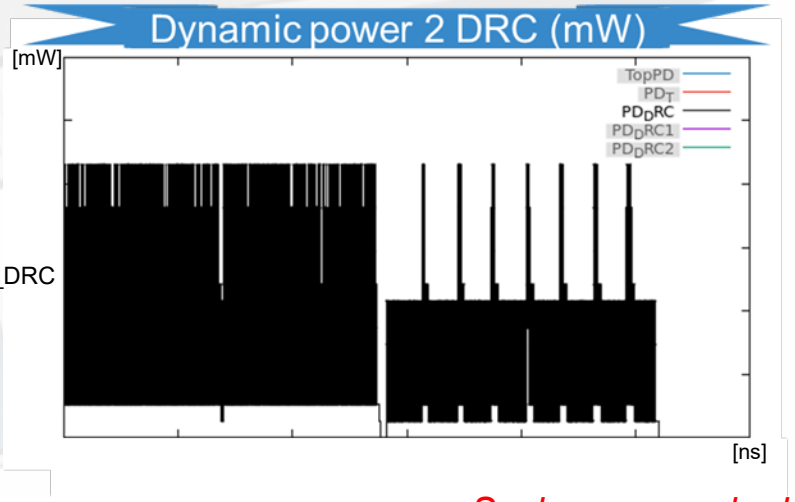


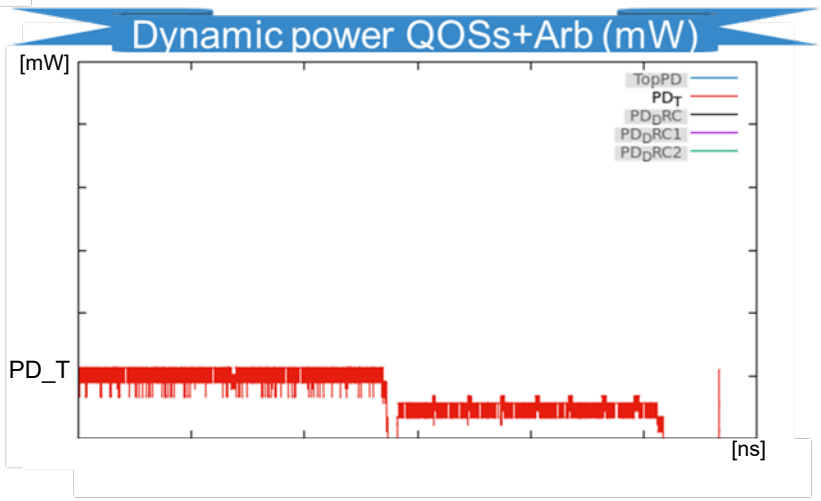
Scales are masked due to confidentiality restrictions

Results - Observations







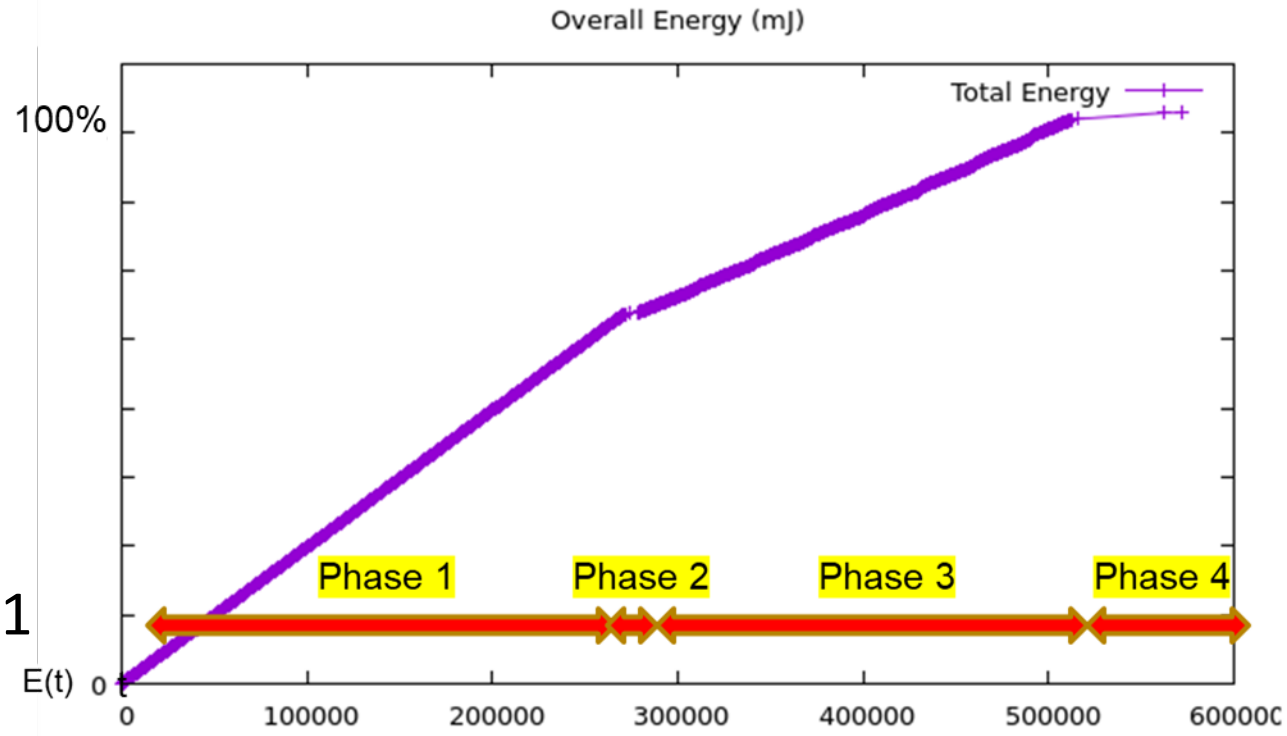


Scales are masked due to confidentiality restrictions

Results - Overall energy

- $E = \int P(t)dt$

- Observations
  - Phase 1 – max consumption
  - Phase 2 – absence of activity
  - Phase 3 –the slope is lower than in Phase 1



Scales are masked due to confidentiality restrictions

Results - Correlation

Subsystems power contribution	Simulation/Silicon power measurements correlation
Interconnect dynamic power	95%
Interconnect static power	97%
2 DRC dynamic power	95%
2 DRC static power	97%
Total power under 1.1V	95-97%

Values are masked due to confidentiality restrictions

Summary & Outlook

- Based on initial assessment, we are convinced by PwClkARCH technology and we continue to support and test it with different use cases and silicon measurements comparison.

- It would be very interesting to integrate this technology into an industrialized EDA.

- Our second DVCon2020 paper presents some additional use case simulations and methodology enhancements.
  - *"Timing-Aware high level power estimation of industrial interconnect module" - (presented by Amal Ben Ameur)*

Thank you!

Q&A