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Mixed-abstraction Modeling Approach with Fault Injection for Hardware-Firmware Co-design and Functional Co-verification of an Automotive Airbag System on Chip Product

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System Integration and Rapid Prototype

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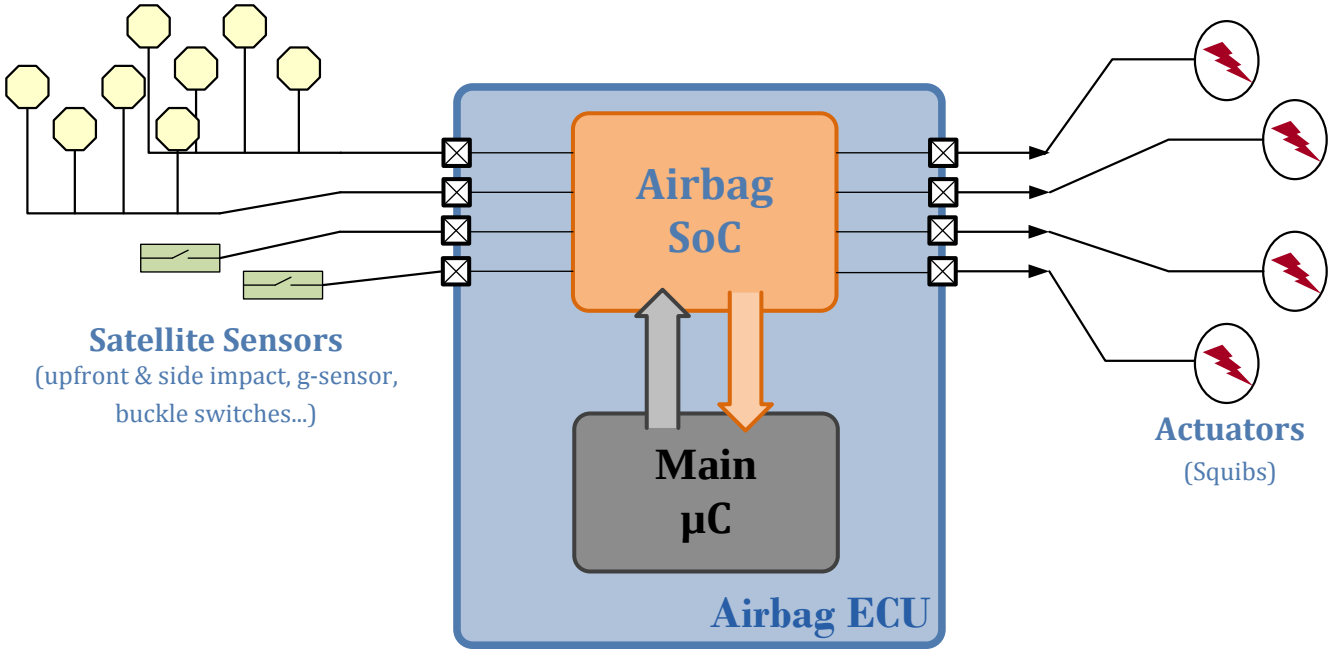
Agenda

- Automotive Airbag System Overview
- Challenges of Airbag SoC Design and Verification
- The Mixed-abstraction Modeling Approach
- Model Coverage Evaluation
- Fault Injection Simulation using Global Signaling Concept
- Summary of Results/Conclusions

Automotive Airbag System - I

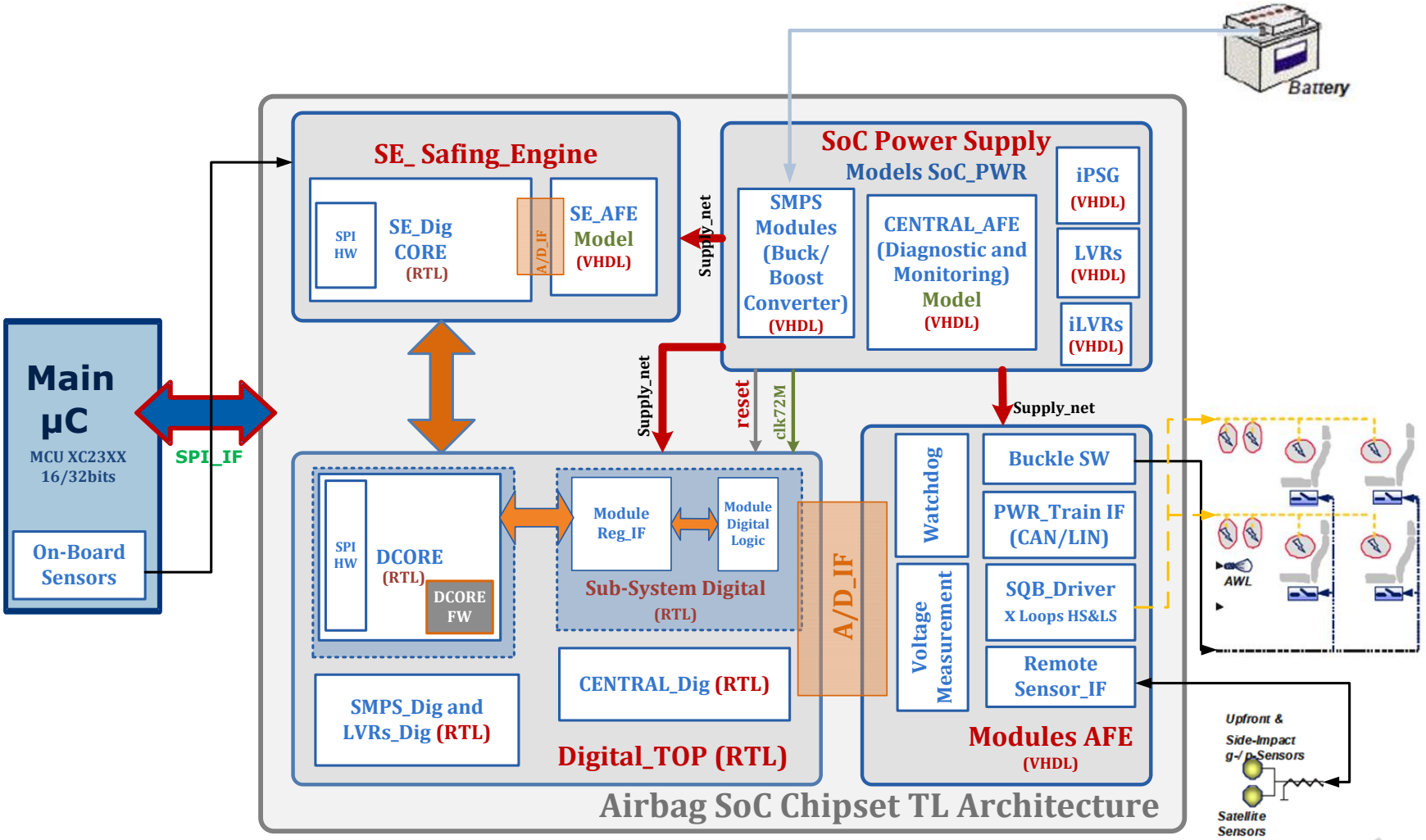


Airbag System Overview

(Sensors <--> Controller <--> Actuators)

...a typical airbag system from bird's eye view

Automotive Airbag System - II



Challenges of Airbag SoC Design

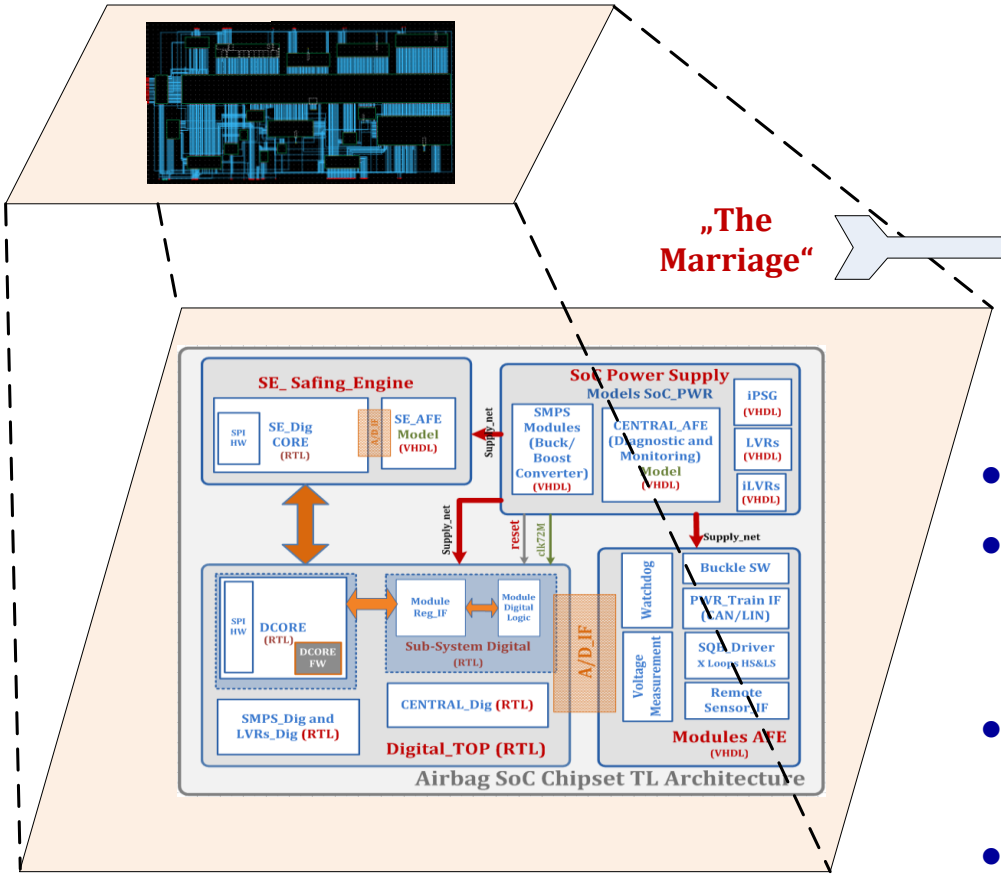
- Factors that drive design complexity:
  - Based on modern sub-micron logic and PWR technology
  - integration of high complexity digital circuits with high voltage power driving modules
    - → new architecture approach with distributed functionalities in D/A/_HW and embedded FW
  - Compliance to ISO 26262 safety standard
- The system covers real-time embedded mixed-signal domains with high number of modules
- Time-to-Market and first time right design

→ leads to verification challenges

Modeling Requirements & Analysis

- A complete airbag SoC chip model:
  - Top-level functional simulation = HW, FW, and co-verification
  - "Accuracy" vs. "Speed"
  - Interface consistency between analogue/digital and also with top-level schematic
- HW (A+D) behavior model for HW/FW co-verification at chip toplevel at early stage of the design phase.
- Effort vs. Time vs. Accuracy

The Mixed-abstraction Modeling Approach



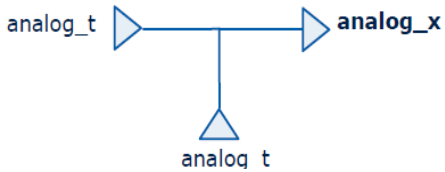
s1280a11_top TO Schematic VHDL Netlist

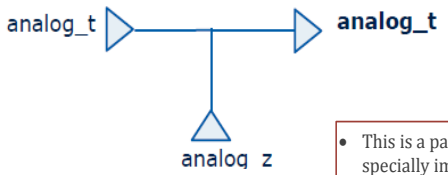
Reuse !

- Reuse of the chip digital RTL code
- Analogue circuit is modelled using VHDL with support of real value for the analog behavior
- Model integration using top-level tape-out schematic netlist Reuse !
- Firmware ROM Mask content is used directly with the digital RTL of the model Reuse !

Example of analogue circuit modeling

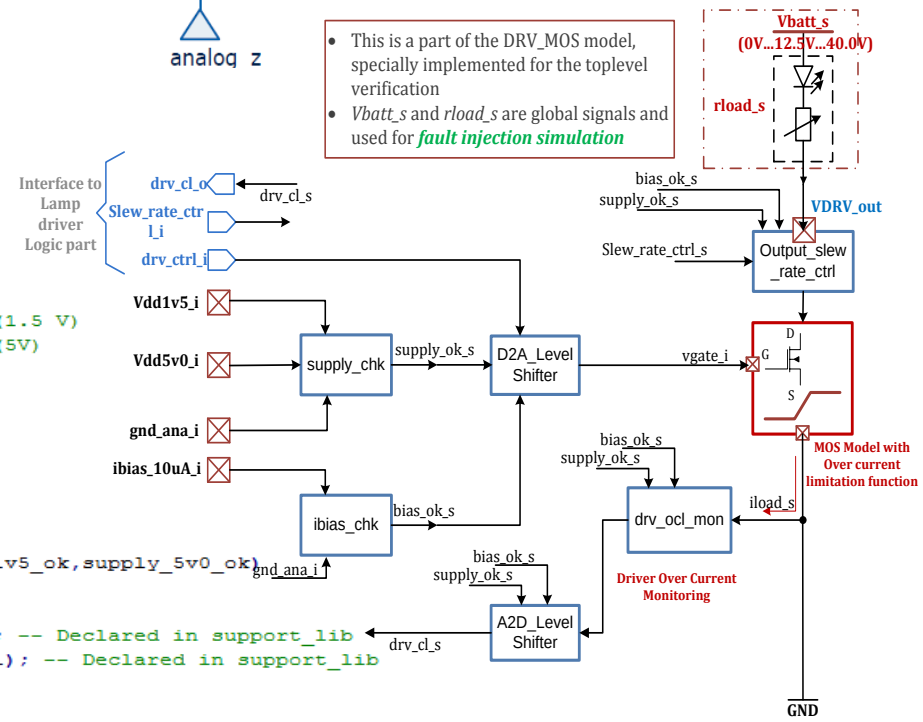
- Resolution function and example of supply_check module:





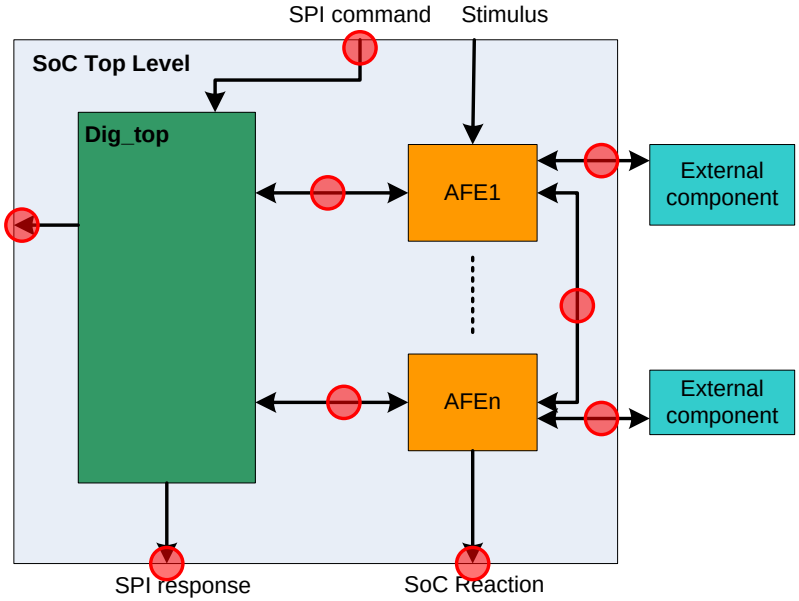

```
4   USE ieee.numeric_std.all;
5   --! Use IFX simple analog library.
6   LIBRARY work, analog_hw;
7   USE analog_hw.analog_pack.all; --! Use analog elements.
8   --! Supporting functionality for high-level behavioral models.
9   USE work.support_lib.all;
10
11  ENTITY lamp_drv_supply_check IS
12    PORT(
13      ana_gnd_i    : IN    analog_t;       --! Ground Pin
14      vdd1v5_i     : IN    analog_t;       --! Analog Supply Voltage (1.5 V)
15      vdd5v0_i     : IN    analog_t;       --! Analog Supply Voltage (5V)
16      supply_ok_o  : OUT   std_ulogic      --! supply ok signal
17    );
18  END lamp_drv_supply_check;
19
20  ARCHITECTURE behav OF lamp_drv_supply_check IS
21      signal supply_1v5_ok : std_ulogic := '0';
22      signal supply_5v0_ok : std_ulogic := '0';
23  BEGIN
24      supply_check: process (vdd1v5_a_i,vdd5v_ps_i,ana_gnd_i,supply_1v5_ok,supply_5v0_ok)
25      begin
26
27          supply_1v5_ok <= supply_test_1v5(vdd1v5_a_i,gpd_ana_gnd_i); -- Declared in support_lib
28          supply_5v0_ok <= supply_test_5v0ps(vdd5v_ps_i,gpd_ana_gnd_i); -- Declared in support_lib
29
30          if supply_1v5_ok = '1' and supply_5v0_ok ='1'  then
31              supply_ok_o <= '1';
32          else
33              supply_ok_o <= '0';
34          end if;
35      end process;
36  END behav;
```

- This is a part of the DRV_MOS model, specially implemented for the toplevel verification
- *Vbatt_s* and *rload_s* are global signals and used for ***fault injection simulation***



Model Coverage Evaluation

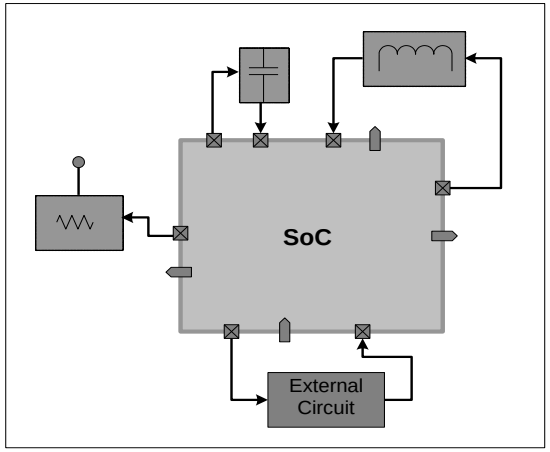
- Functional coverage:
  - Hardware (ANA + DIG) behavior
  - Firmware behavior
  - PWR → Chip Gobal functional
- Physical Impelmentation coverage:
  - Digital_Hardware (RTL)
  - ROM Mask
  - Interfaces between DIG and ANA hardware domain
  - Top-level LVS connectivities

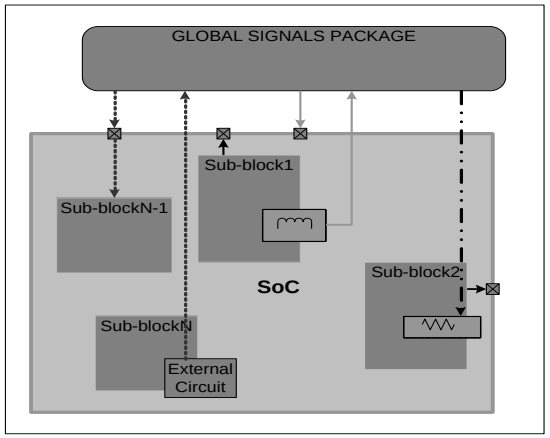


The Mixed-abstraction Modeling Approach – Advantages/Limitations

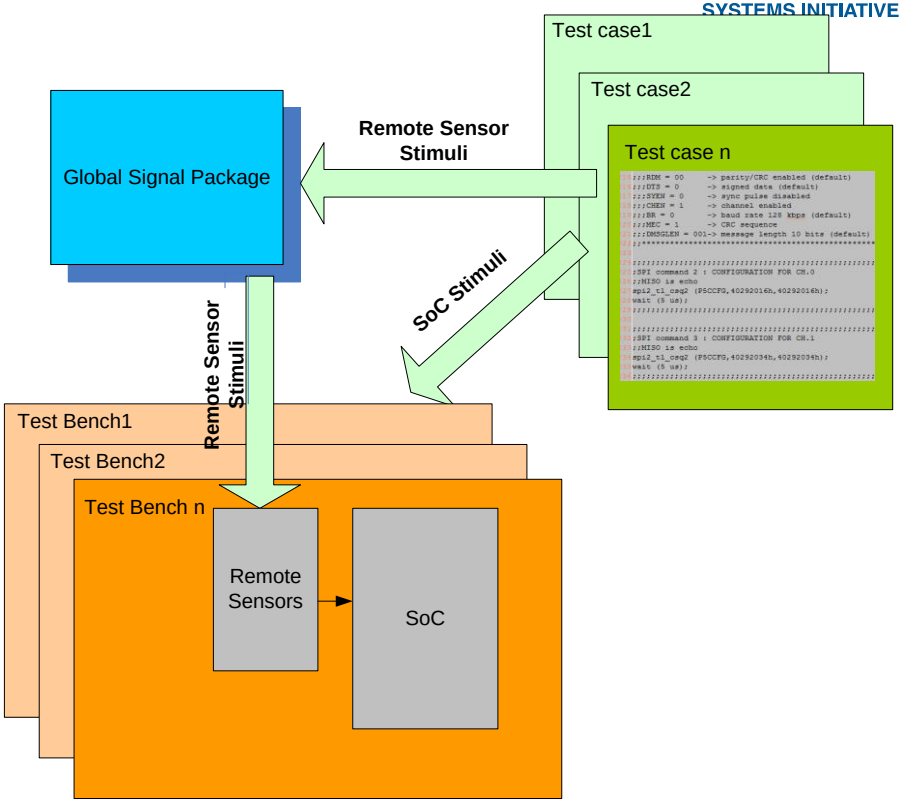
+ Event based simulation @ chip top-level:
  - significantly gain in speed complexity and clk rate)
  - et. Convergency
+ still guarantee the accuracy for functional verification purpose.
+ Effort (integration and maintenance) vs. Time (in a very short) vs. Accuracy (High)
- For chip TL model integration: it is strongly dependent on the DIG_TOP level
- Modeling of external load (capacitive and inductive) is limited → workaround: „Global Signalling Concept"

Global Signaling Concept





…for external load modeling



…for fault injection simulation

Summary of Results/Conclusions

- Virtual „prototype" of the airbag SoC product at an early phase for firmware develop. and verification
- Simulation performance: less than 1h (for a typical functional simulation run at chip top-level)
- Bridging the gap between "Speed" and "Accuracy"
- Project could significantly gain time-to-market and achieve design target