Metric Driven Mixed-Signal Verification Methodology and Practices for Complex Mixed-signal ASSPs

Frank Yang; Andy Sha; Morton Zhao

Analog Devices , Beijing, China

Yanping Sha

Cadence design Systems, Beijing, China

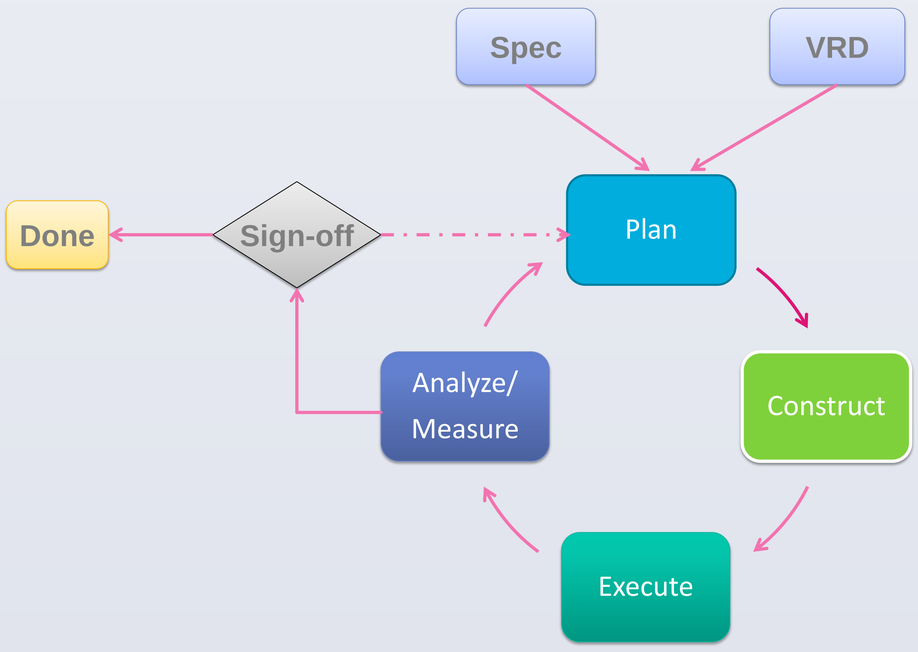
Abstract

Abstract - **Most ASSPs today are mixed-signal systems and this higher level of integration means the verification of these ASSPs is becoming more and more complex. For the 'digital only' SOCs there already exists advanced verification methodologies are widely used throughout the industry i.e. VMM, UVM, metric driven verification (MDV). The push in verification is now to extend these advanced verification methodologies to be used in analog/mixed-signal ASSP verification as well.**

A recent ASSP in ADI is an example of this trend. The ASSP was a true mixed signal development, incorporating a Cortex-M3 MCU with analog peripherals including, ADC, VDAC, IDAC and PLL etc. This paper will discuss how we implemented MDV for the mixed-signal ASSP, how we defined verification metrics for analog/mixed-signal blocks and how we built up the mixed-signal constrained random verification environment. Defining verification metrics for analog/mixed-signal blocks is a key common problem for mixed-signal MDV and a lot of the discussions will focus on this topic.

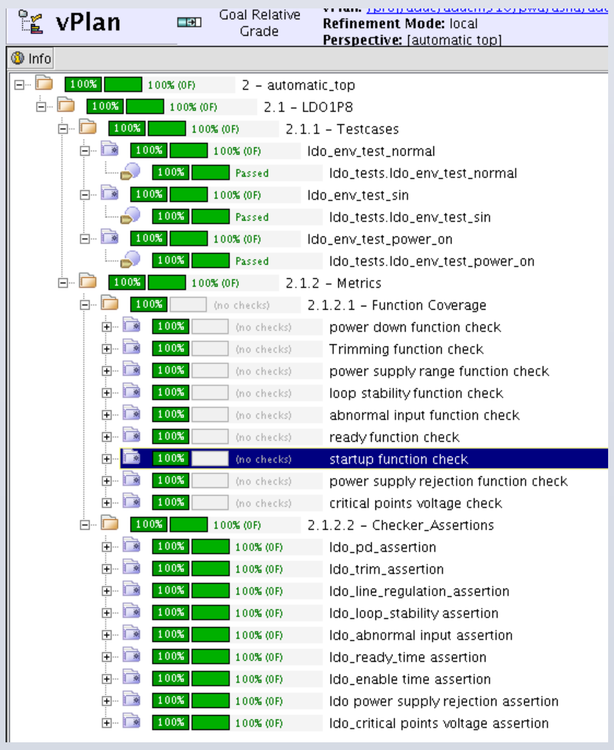
Metric Driven Verification Flow

The metric driven verification flow is shown as below.



Verification Plan

We used Eplanner as the verification plan tool. An example is shown as below.



UVM Verification Environment Build Up

Some simple real-life UVM code is shown as blow.

```
// Integration for UVM-compliant Program block

// Interfaces
`include "mstr_slv_intfs.incl"


module ldo_env_tb_mod; //integration module

import uvm_pkg::*;
`include "uvm_macros.svh"

// ENV+TEST
`include "ldo_env_env.sv"
`include "ldo_env_test.sv"

// All interfaces
   typedef virtual ldo_magt_if    v_if1;
   typedef virtual ldo_sagt_if    v_if2;
   typedef virtual analog_stim_if v_if3;

// Configure TB / Run Test
   initial begin
      uvm_config_db #(v_if1)::set(null,"","mst_if",u_ldo_tb_sv.mst_if);
      uvm_config_db #(v_if2)::set(null,"","slv_if",u_ldo_tb_sv.slv_if);
      uvm_config_db #(v_if3)::set(null,"*.x_analog_stim_agt0","analog_agt_if",
      u_ldo_tb_sv.x_analog_stim_if0);
      uvm_config_db #(v_if3)::set(null,"*.x_analog_stim_agt1","analog_agt_if",
      u_ldo_tb_sv.x_analog_stim_if1);
      run_test();
   end

endmodule: ldo_env_tb_mod
```

Analog/MS verification metric definition and implementation

We defined the following types of analog/mixed-signal verification metrics.

- ***Real number analog assertions***

The following table shows the features which are suitable to use real number analog assertions to define metrics.

Features	Detailed Features and Examples	
Timing	Settling time, none-overlap signals timing	
Digital controlled analog trimming	Voltage trimming	Reference/LDO/POR trip point trimming
	Current trimming	Bias current trimming
	Clock frequency trimming	VCO/Oscillator trimming
Digital assisted analog calibration	ADC offset/gain calibration	
	DAC offset/gain calibration	
Algorithm	ADC chop, average, redundant, dither…	
Critical signal monitors	Monitor power supply, reference and bias	

The following code shows a real number analog assertion example: LDO power supply rejection performance check.

```
// Real number analog assertion: LDO power supply rejection performance check
module psr_chk_db
 #(
 // LDO PSR spec: -50 db
   parameter psr_spec_db = -50.00,
 // Expected voltage output of the LDO: 1.8v
   parameter base_point = 1.8,
 // Amplitude of the sine wave noise: +/-50 mv
   parameter power_noise  = 0.05,
  // Calculated torerance
   parameter tolerance = ( power_noise* 10**(psr_spec_db/20.0))/base_point
  )
  (
    input real v1p8_a,       // the voltage output of the LDO
    input      ldo_pd,       // power down LDO
    input      sample_clk    // Sample clock
   );

v_checker
 #(.base_point(base_point),
   .tolerance(tolerance),
   .delay_check(0)
  )
 u_v_checker
 (.compare_value(v1p8_a),
  .sample_clk(sample_clk),
  .disable_check(ldo_pd),
  .compare_enable(1'b1)
  );

endmodule
```

- ***Real Number Functional Coverage***

The following table shows the features which are suitable to use real number function coverage to define metrics.

Features	Detailed Features and Examples
Voltage range	ADC input voltage range
	DAC output voltage range
	Voltage reference range
Current range	Bias current range
Clock frequency range	PLL VCO clock frequency range
	PLL input reference clock range

The system verilog real number functional coverage code for ADC input range is shown as below.

```
real ain_r;

covergroup real_bin_cg;
  option.per_instance = 1;
  adc_in_range : coverpoint ain_r {
    bins Zero          = {0};              // 0
    bins HalfScale     = {1.25};           // half scale input
    bins FullScale     = {2.5};            // full scale input
    bins OverFlow      = {2.75};           // over flow input
    bins ain_range1    = {[0.1  :0.25  ]}; // 0.1-0.25
    bins ain_range2    = {[0.25 :0.5   ]}; // 0.25-0.5
    bins ain_range3    = {[0.5  :0.75  ]}; // 0.5-0.75
    bins ain_range4    = {[0.75  :1.0  ]}; // 0.75-1.0
    bins ain_range5    = {[1.0  :1.25  ]}; // 1.0-1.25
    bins ain_range6    = {[1.25  :1.5  ]}; // 1.25-1.5
    bins ain_range7    = {[1.5  :1.75  ]}; // 1.5-1.75
    bins ain_range8    = {[1.75 :2.0   ]}; // 1.75-2.0
    bins ain_range9    = {[2.0  :2.25  ]}; // 2.0-2.25
    bins ain_range10   = {[2.25 :2.5   ]}; // 2.25-2.5
  }
endgroup : real_bin_cg
```

- ***Memery mapped register function coverage***

Function coverage of memory mapped register is defined to cover the function of each bit of memory mapped register.

- ***Toggle coverage of analog/digital interface signals***

The toggle coverage of analog/digital interface signals is defined to cover the different control sequences.

- ***Code coverage***

Code coverage of RTL in analog control blocks.

Conclusions

Implementing these advanced metric driven mixed-signal verification techniques on our recent ASSP development was a great success and resulted in first pass silicon success. The initial revision of silicon was successfully sampled to our customers.

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Contacts

We can be contacted by email Frank.Yang@analog.com and Andy.Sha@analog.com