Low Power Techniques in Emulation

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Need of Power Verification

- SoCs today are more complex due to increased performance and functionality

- This is leading to designs with increased power dissipations and driving the demand for low power consumption

- Power verification is equally important as functional verification
Power Management Techniques

- Isolation
- Retention
- Level shifter
- Clock gating
Definition of UPF

• Accellera standard – Unified Power Format
• To define power intent in design
• Written in formats like IEEE1801 UPF
• Enables low power design and verification from early RTL verification of the power management architecture through physical design and implementation
Power Aware Verification
Power Aware Simulation

- Power aware simulation mimics circuit behavior for power up/down events
- When block is powered off
  - Internals and outputs corrupted to “X”
- When block powered on
  - Start simulation as if @ time zero
Challenges in Simulation

- Complex design contains more power domains
- Longer runtime in Simulation due to complexity involved in SoCs
- Complete power verification is very time consuming on simulation due to its speed and longer runtime for bigger designs
- Trade-off between accuracy and speed
- Debug is difficult to replicate for a later time of a test
Need for Low Power Emulation

• Emulation – runs on hardware (FPGA/Processor based system)

• Many magnitudes faster than simulation

• Complete regression suite with complex power scenarios can be exercised in much faster way
Power Aware Emulation

• Power Simulation features:
  – Multiple power domains
  – Hierarchical power domain connections
  – Special power cells viz. isolation, retention, switches
  – X corruption of power domains

• Behavior
  – When supply is off
    • Internals and outputs corrupt to “X” – on waveform
  – When supply is on
    • Normal simulation
Simulation Challenge-1

- Longer Runtime in Simulation

**Problem:** Usually simulators are very low, so it is preferable to have a platform that runs the tests faster

**Solution:** The design was ported to the emulation platform and UPF techniques were applied for power verification
Design Overview
Simulation Challenge-2

• X-propagation in Simulation

_Problem:_ Simulation adds additional X for the power-down domains leading to functional bugs

_Solution:_ Emulation works on randomization, resulting in some unknown values to the internal nodes if they are not powered on, it provides a good coverage of overall Power-down behavior in real hardware
Simulation Challenge - 3

• Power Management is difficult in Simulation

Problem: Power management, including UPF and average and peak power calculations, is difficult in Simulation due to its nature of keeping a record of each and every net/reg behavior inside design.

Solution: Simulation can run for a few 10s/100s of thousand cycles which is not an ideal situation for most of current designs, Emulation is needed to run billion cycles to calculate the exact power behavior with better coverage of all applications running as a test.
Conclusion

• Due to the increased complexity, simulation is less viable approach for power verification

• The results of emulation are much closer to actual power consumption than simulated results and manual calculations

• Combination of Emulation + Power tools is a new way of doing efficient power verification
Questions