DESIGN & VERIFICATION DVCON 2014 CONFERENCE & EXHIBITION

Leveraging IP-XACT Standardized IP Interfaces for Rapid IP Integration

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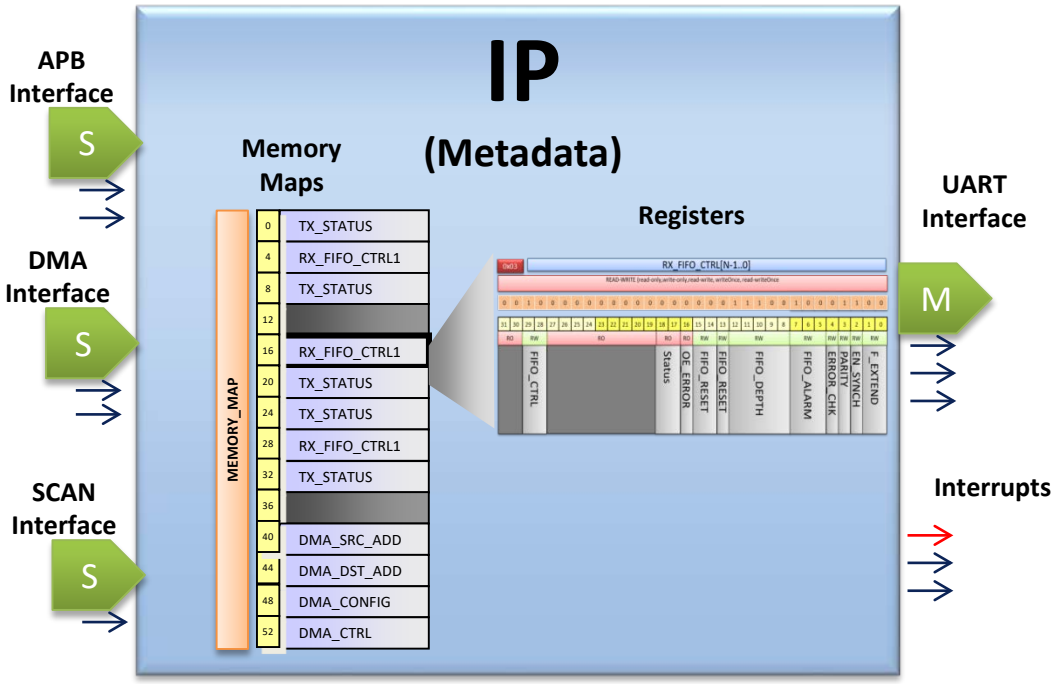
Overview

- What is Interface Standardization
- Why Standardize?
- Leveraging Standards
- IP-XACT as an interface standard
- Mechanics
- Flows
- Summary

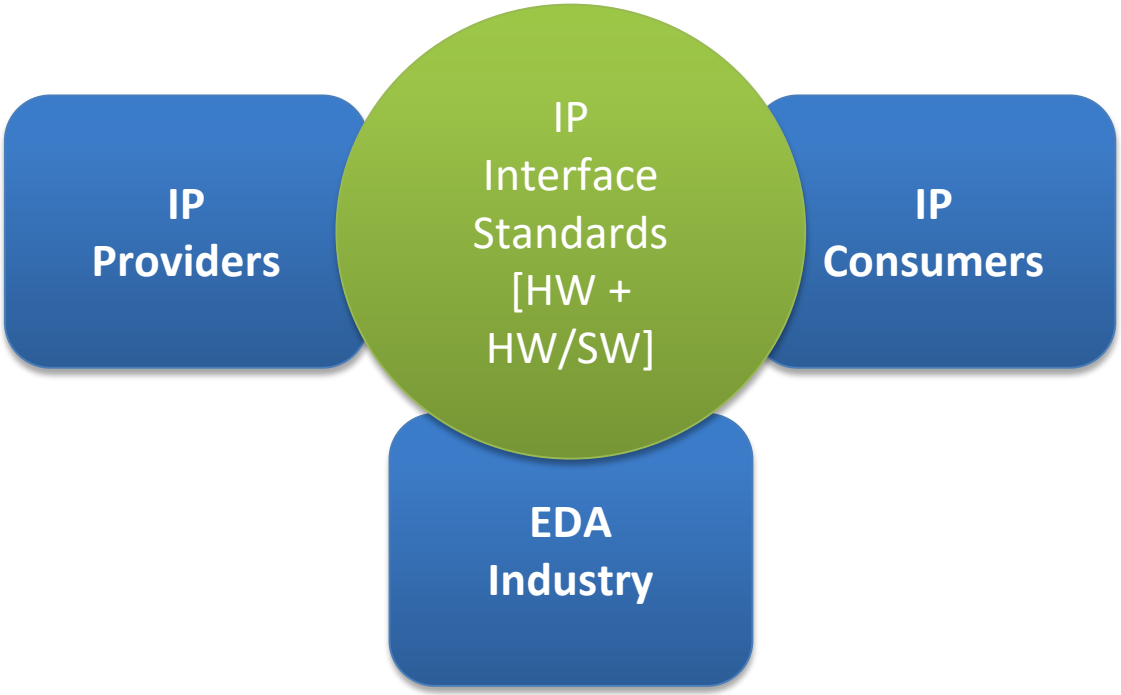
WHAT IS IP INTERFACE STANDARDIZATION?

- Standardization of
  - HW Interface
    - Ports
  - SW Interface
    - Memory Maps
    - Registers



Why Standardize

'INTEROPERABILITY'



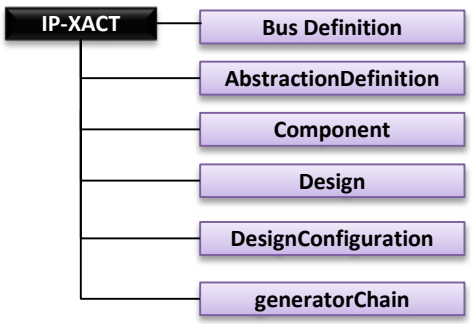
Leveraging Standards

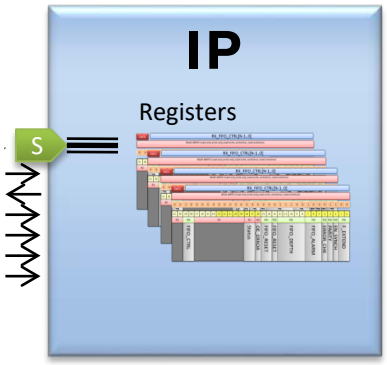
- Leveraging interface standards for IP Creators
  - Standards help utilise automation to create IP Collateral e.g. documentation, design implementations or verification environments.
- Leveraging standards for IP Consumers
  - Standards help to automate IP integration and verification. IP blocks with known good interfaces are easier to integrate both from the hardware and software side.
- Leveraging standards by EDA industry
  - Standards are not enough! They must be automatable and automated!
  - EDA Industry delivers value by providing automation of complex design and verification flows,

IP-XACT Standard

- IP-XACT is an XML schema that defines and describes electronic components and their designs.
- Goals
  - to ensure delivery of compatible component descriptions from multiple component vendors
  - to enable exchanging complex component libraries between EDA tools for SoC design
  - to describe configurable components using metadata
  - to enable the provision of EDA vendor-neutral scripts for component creation and configuration

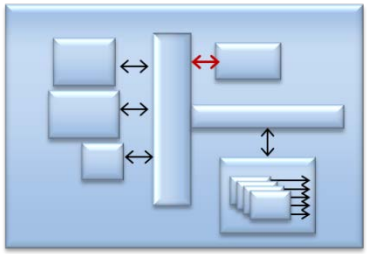
IP-XACT Content





IP Metadata
- Components
- Ports
- Bus Interfaces/Definitions
- Filesets/files
- Memorymaps/registers
- ComponentGenerators

SoC / Sub-system

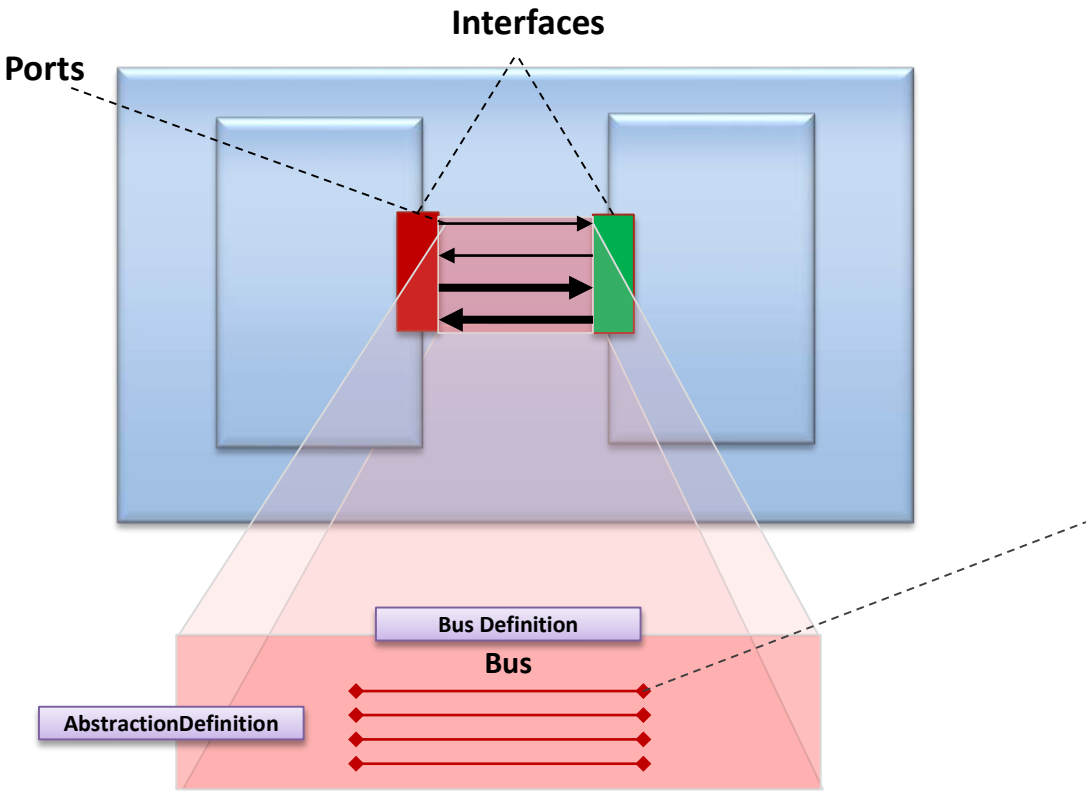


Design/Integration Metadata
- Component Instances
- Interface connections
- Port-level connections
- Design Configurations

Flows

Generators/Flows
- Component Generators
- Generator Chains

Bus Definitions



Port Definition		
Name		ADR
Description		Address
Type		Wire
Default		0
Qualifier		isAddress
On Master	Presence	Required
	Direction	out
	Width	
On Slave	Presence	Required
	Direction	In
	Width	
On System	Presence	illegal
	Direction	
	Width	

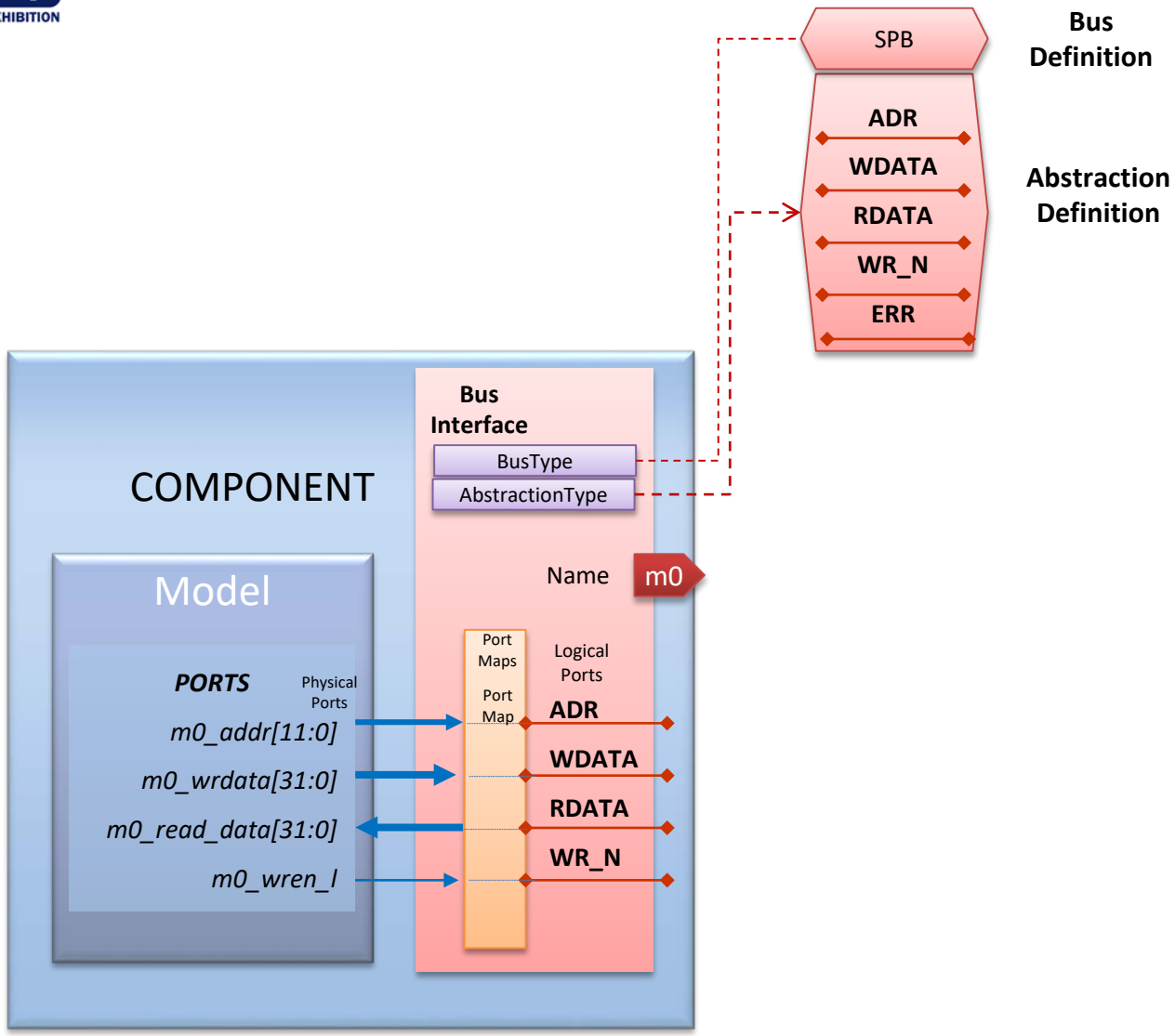
Defines how bus ports should appear on interfaces

Bus Abstraction

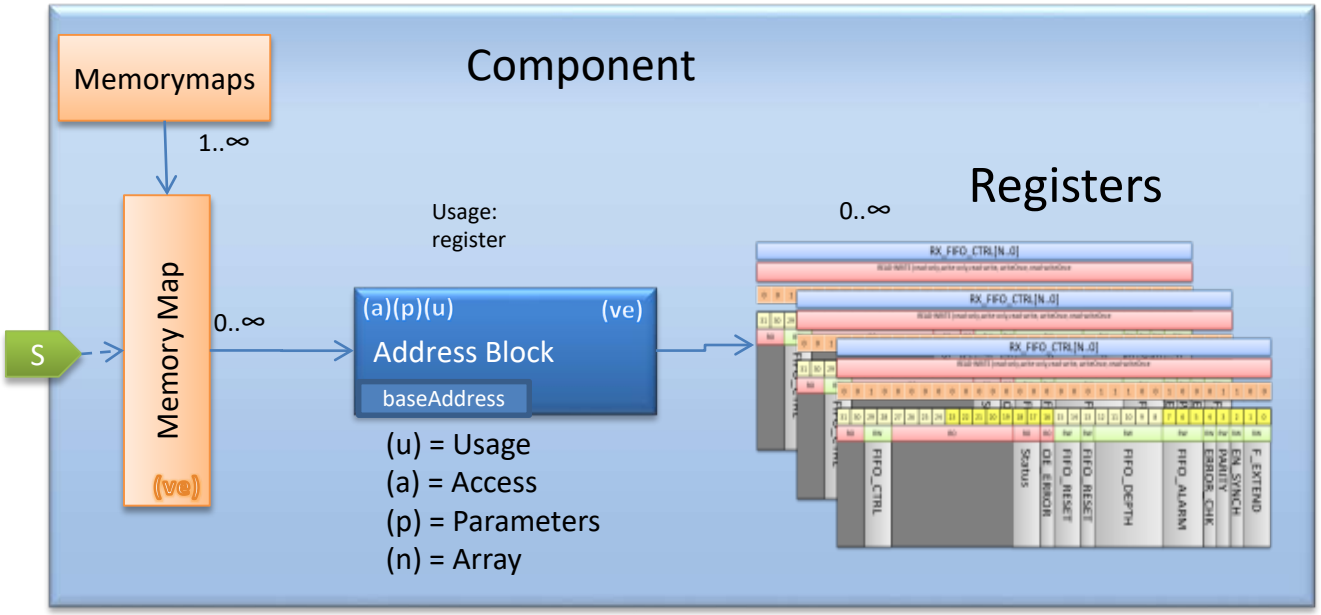
				On System			On Slave			On Master		
Name	Description	Type	Default	Presence	Direction	Width	Presence	Direction	Width	Presence	Direction	Width
ADR	Address	Wire	0	Illegal			Required	in		Required	out	
WDATA	WriteData	Wire	0	Illegal			Required	in	32	Required	out	32
RDATA	ReadData	Wire	0	Illegal			Required	out	32	Required	in	32
WR_N	Write Enable	Wire	1	Illegal			Required	out	1	Required	in	1
ERR	Error	Wire	0	Illegal			Optional	out	1	Optional	in	1

- Defines the main characteristics of an overall bus and how it should appear on an IP

Mapping Ports to Interfaces

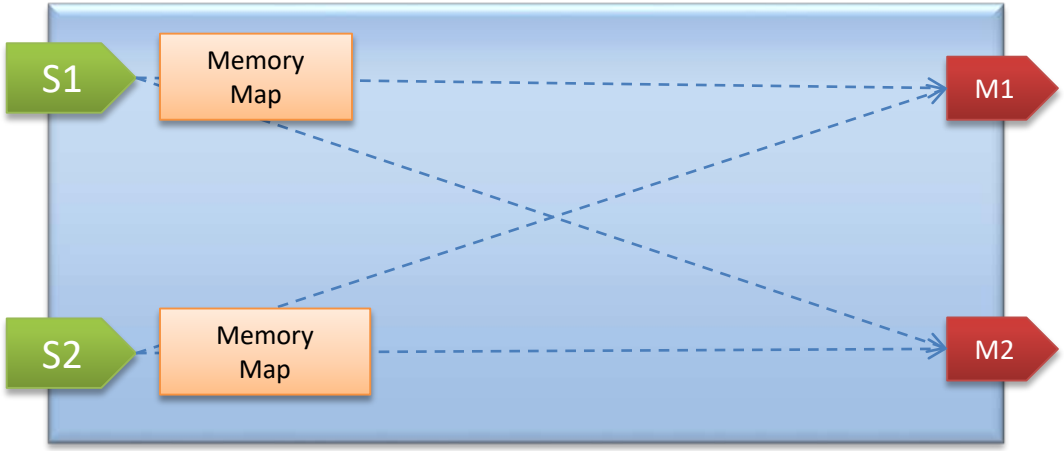


HW/SW Interface



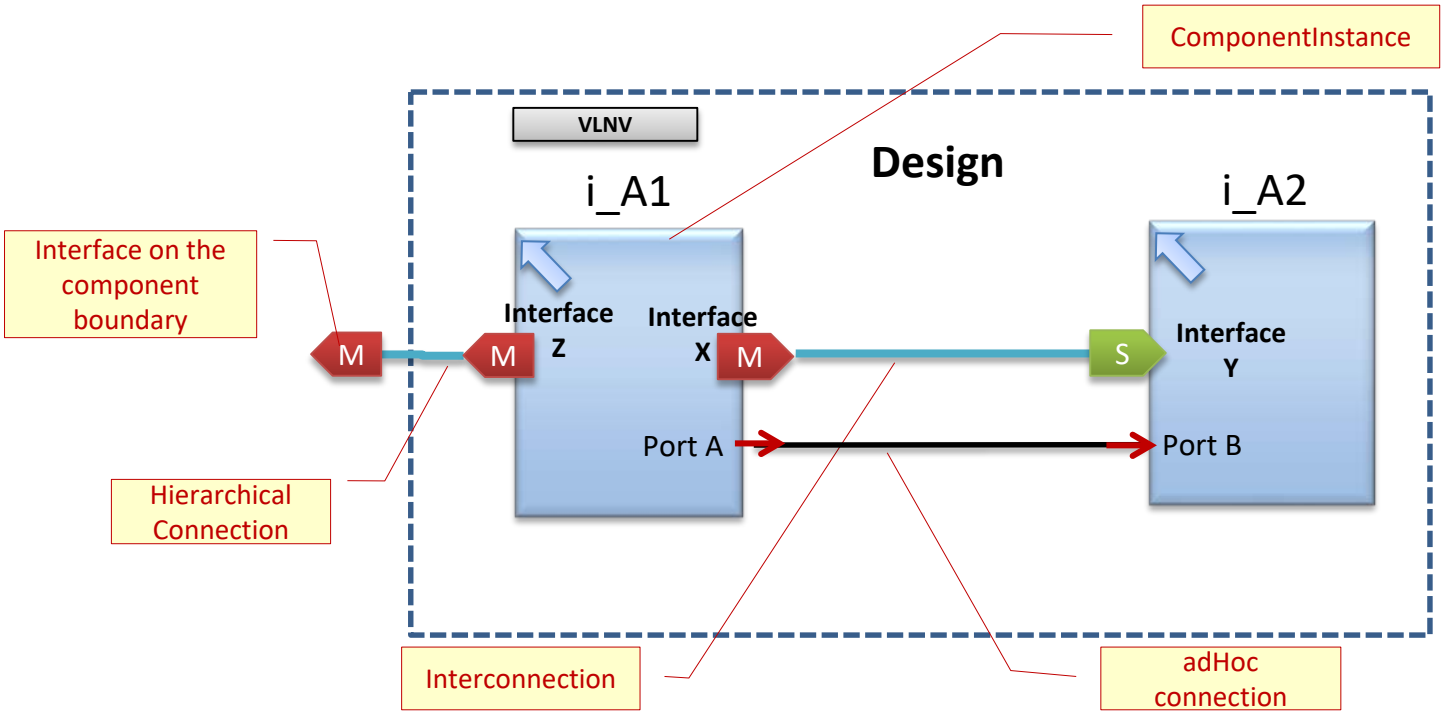
- Defines Memory maps and registers in an standard format

Interconnects/Bridges



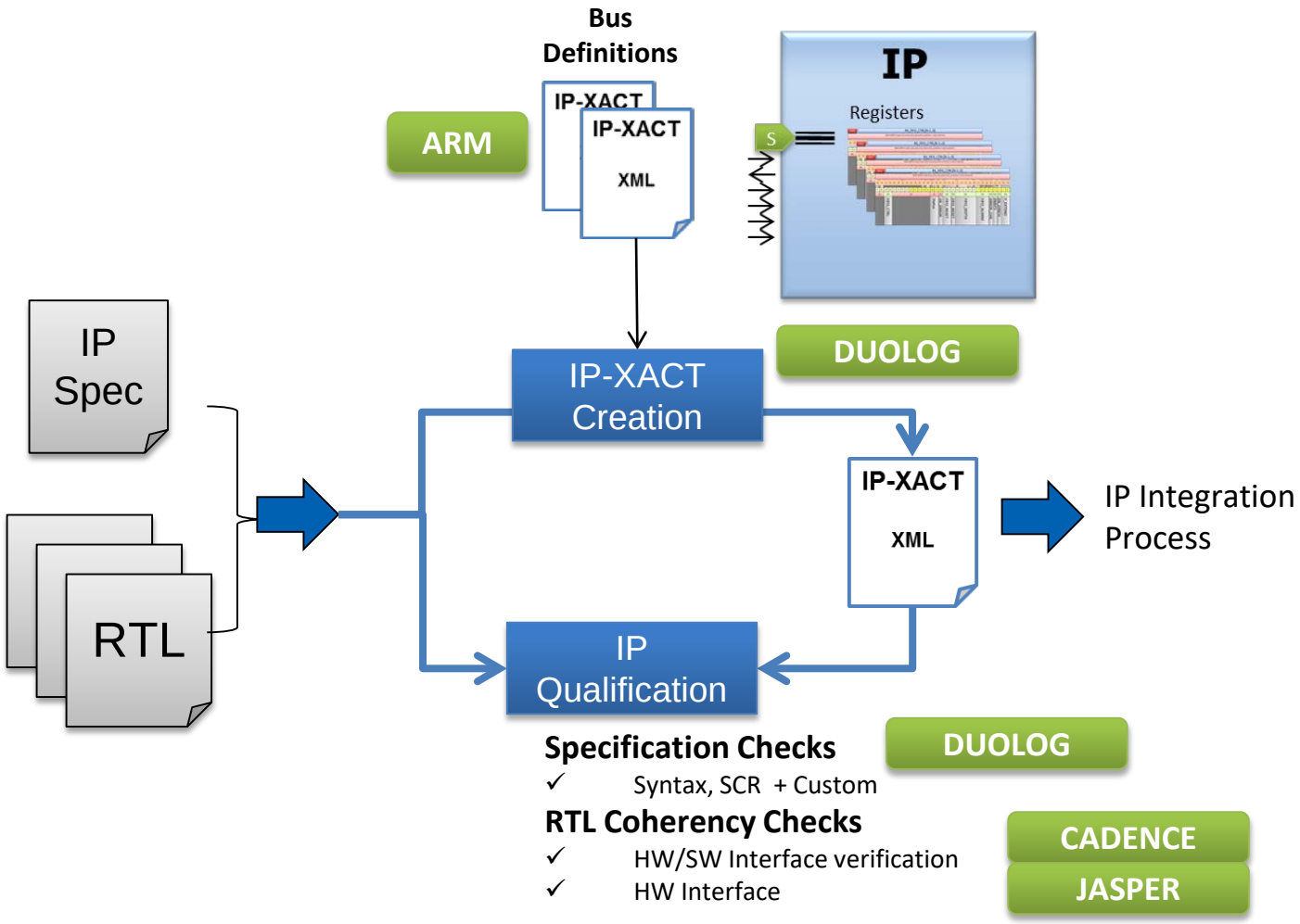
- Defines Bus interconnect structures and bridges

Defining Connected Systems

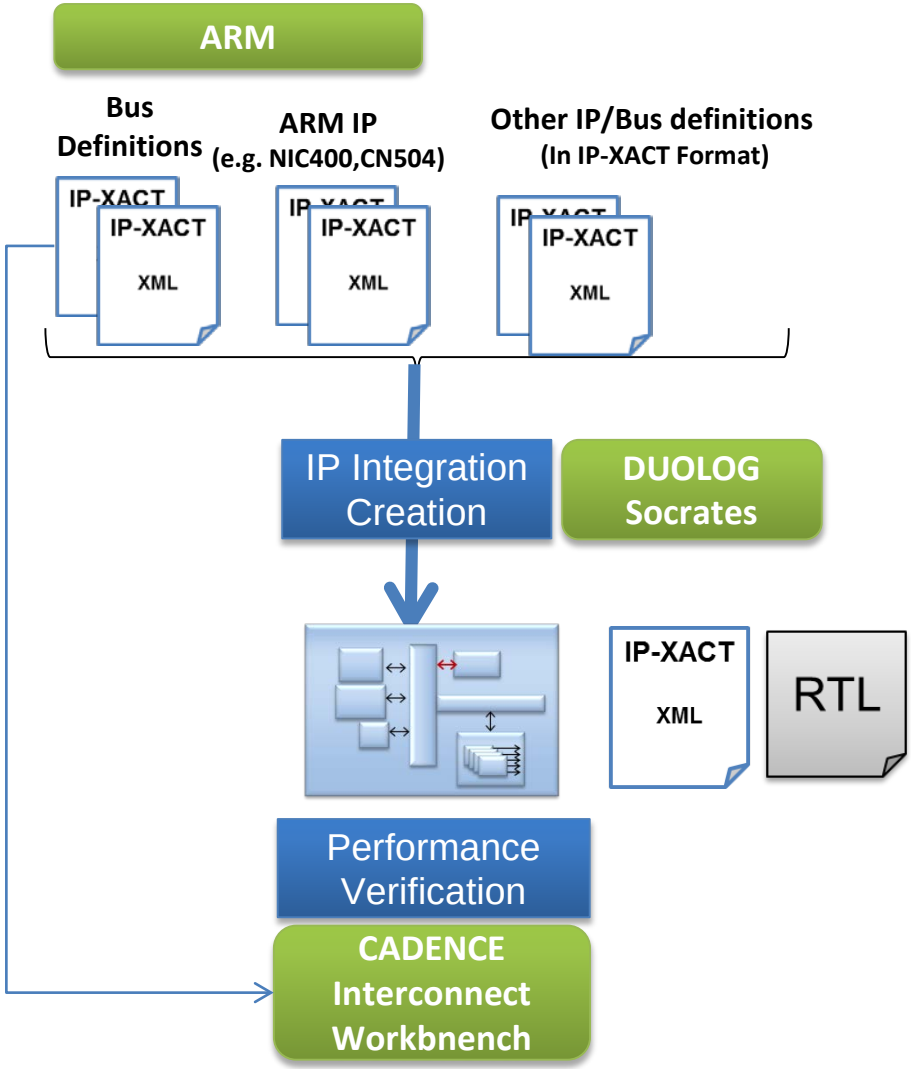


Utilizing the Standard

IP Qualification



IP Integration and Verification



Summary

- The growth of 3rd party IP usage and the lack of hardware and Hardware/Software interface standardization are causing a lot of integration issues which remain a key challenge of SoC design

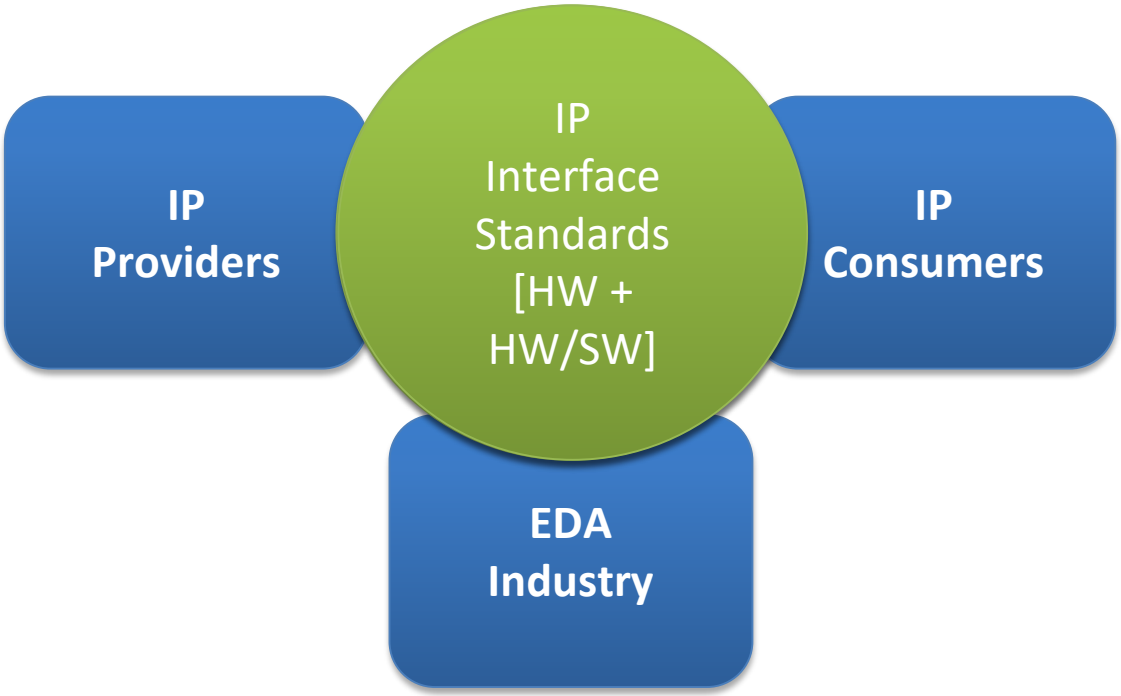
- IP-XACT has emerged as a clear leader for the IP interface specification standards
  - It has comprehensive capabilities when it comes to defining the intricacies of RTL port interfaces
  - Possible Hardware/Software elements such as registers and memory maps.

- The standardization of IP interface helps
  - To improve IP quality and automation
  - To streamline IP integration and verification

- IP-XACT adoption in the industry has led to high-value multi-vendor, interoperable flows that provide integration ready-IP, accelerate IP integration and enable high levels of verification automation.

Acknowledgements

ONE BIG HAPPY FAMILY



Thanks our industry partners who have collaborated with us in the past number of years to make these highly interoperable IP-XACT Flows.

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Questions!

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Thank You !