JESD204B Deterministic Latency Verification with UVM Constrained Random Approaches

Girish Nadiger
Analog Devices, Inc.
Bangalore, India – 560016
girish.nadiger@analog.com

Ashok Chandran
Analog Devices, Inc.
Bangalore, India – 560016
ashok.chandran@analog.com

***Abstract* - As the high speed converter market growing more and more designs started using JESD204B converter interface standard. Verifications of JESD204B designs and that of deterministic latency feature in subclass 1 is very critical. Traditionally, deterministic latency is verified manually by analyzing the waveform which is tedious and error prone. This paper proposes a simple yet scalable approach to verify deterministic latency using impulse characterization in a JESD204B DAC system.**

I. INTRODUCTION

As the demand for high speed converters is growing, transmitting data to/from these high speed converters pose a big design challenge as the existing IO technologies don't scale very well in terms of speed, power and number of IO pins. Large number of IO pins on the product makes system level PCB design very complex and also increase the power consumption.

These challenges led to the development of a scalable high speed serial interface standard which would have lesser number of IO pins and would be more flexible.

This paper focuses on verifying deterministic latency feature in JESD204B Rx system in subclass 1. In most of the cases deterministic latency is verified by visually checking the waveform. This is very tedious and error prone. We propose a simple approach for the verification of the same.

II. Overview

A. *Introduction to JESD204B*

JESD204B is a JEDEC standard for serial data interfacing. The standard defines a multi gigabit link between a converter device and a logic device such as FPGA or ASIC.

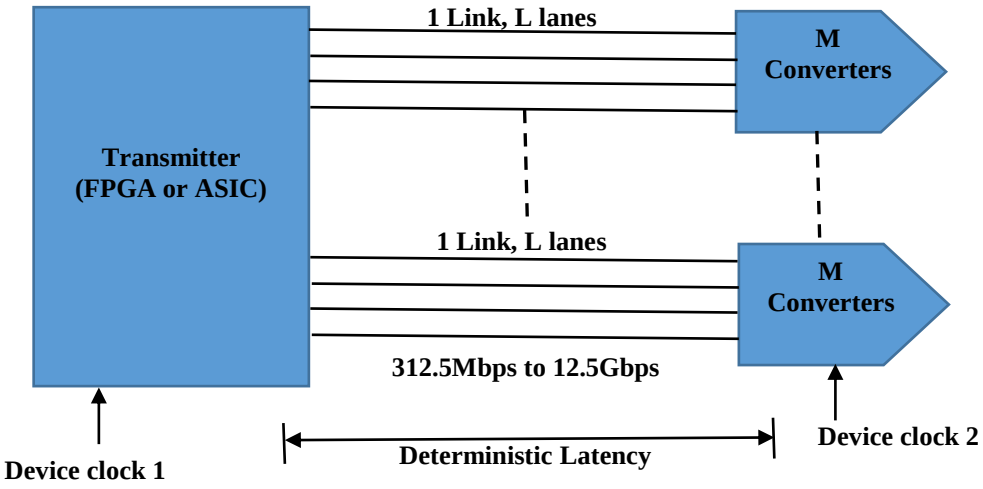

Figure 1. JESD204B DAC system [1]

In Figure 1, there are M converters driven by L physical lanes. Each lane is a serial differential pair of interconnects utilizing current mode logic (CML) drivers and receivers. Each lanes can support up to 12.5Gbps data rate. The link shown is the serialized data link established between the logic device and the converters.

JESD204B interface defines three layers as shown in figure 2 namely,

a. Physical layer

Physical layer consists of L differential pairs of current mode logic (CML) drivers and receivers where L is the number of lanes in a link. Each lanes support data rates between 312.5Mbps to 12.5Gbps. Physical layer recovers clocks from the 8B10B encoded data and parallelizes the input bit stream.

Let us see some of the important signals of interest to us.

i. Device clock: Each converter and transmitter receives their respective device clock from a clock generator circuit which is responsible for generating all device clocks from a common source.

ii. SYNCB : it is a return path from receiver to the transmitter synchronous to receiver internal clocks. SYNCB signal is used to indicate receiver synchronization and also used for error reporting to the transmitter.

iii. SYSREF : SYSREF is the global timing reference for all the components in the system. This signal is used to align all the clocks and also aligns jesd frames in each of the transmitters and converters. This helps in to ensure deterministic latency through the system. SYSREF can be one shot, periodic or gapped periodic.

b. Data link layer

Data link layer is responsible for establishing the link, initial lane alignment and monitoring the link alignment. There is an 8B/10B encoder/decoder which helps in clock recovery at the receiver and also helps in maintaining DC balance. There is also a scrambler/descrambler block which helps in reducing spectral peaks when same data repeats.

c. Transport layer

For receivers, transport layer takes 8B10B decoded octets and maps them back to converter samples.

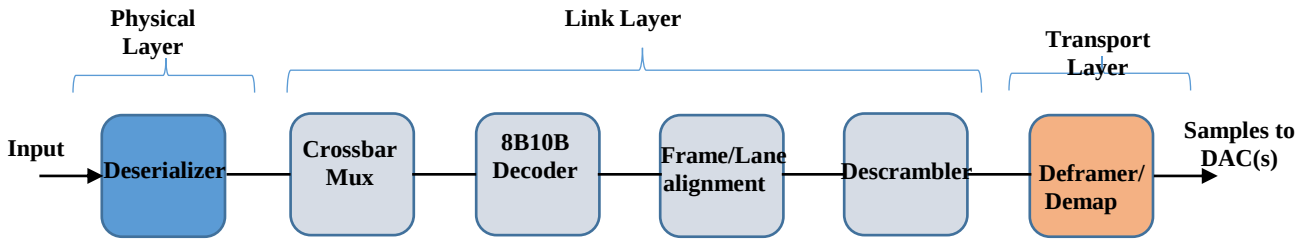

Figure 2. JESD204B layer (Receiver)[2]

B. Deterministic Latency

Matching the latency variation of all converters in the system for application that use array of converters is a big concern. Any mismatch in latency can degrade the system performance. For systems that use interleaved samples also require the latency to be matched. Systems that use digital pre distortion (DPD) loops require latency to be deterministic.

JESD204B addresses these challenges by providing mechanisms to establish deterministic latency for all converters in the system. Deterministic latency is defined as the time it takes for the parallel input data to propagate from transmitter input to parallel data output at the receiver. This time is measured in frame clocks or device clocks. This latency is expected to be constant over power cycles and link resynchronization events and also the latency should be programmable.

Since SYSREF aligns all clocks in each of the converters and logic devices and the frame boundaries are communicated to the receiver by some control characters, each receivers can decode the placement of the transmitter frame relative to its own clocks and also relative to all transmitters. This enables the receiver to de-skew the data on different links with different delays using delay buffers [4] and the de-skewed data is sent out on the next frame boundary. This helps synchronize array of converters.

Since deterministic latency involve multiple modules like SYSREF sampling, clock generation, JESD Rx etc, verification of this feature is very critical and challenging. Traditionally, this is verified by visually checking the waveform. This method is not scalable, tedious – especially when you have lot of JESD operational modes- and error prone.

III. PROPOSED SOLUTION

We propose a simple UVM score boarding method for verifying JESD204B deterministic latency requirements. System latency from JESD TX parallel data input to dac output is characterized by using impulses. An impulse is sent on one of the randomly chosen channels. The time taken for the impulse to propagate through JESD TX, JESD RX, and data path and appear at the dac output is the latency of the system as illustrated in the figure 3. Same procedure conducted multiple times. Hardware reset is asserted between each iterations and also link is re synchronized between the iterations.

Clocks are gated for some random time before sending the impulse just to make sure clocks phase alignment is proper and clock gating has no impact on latency.

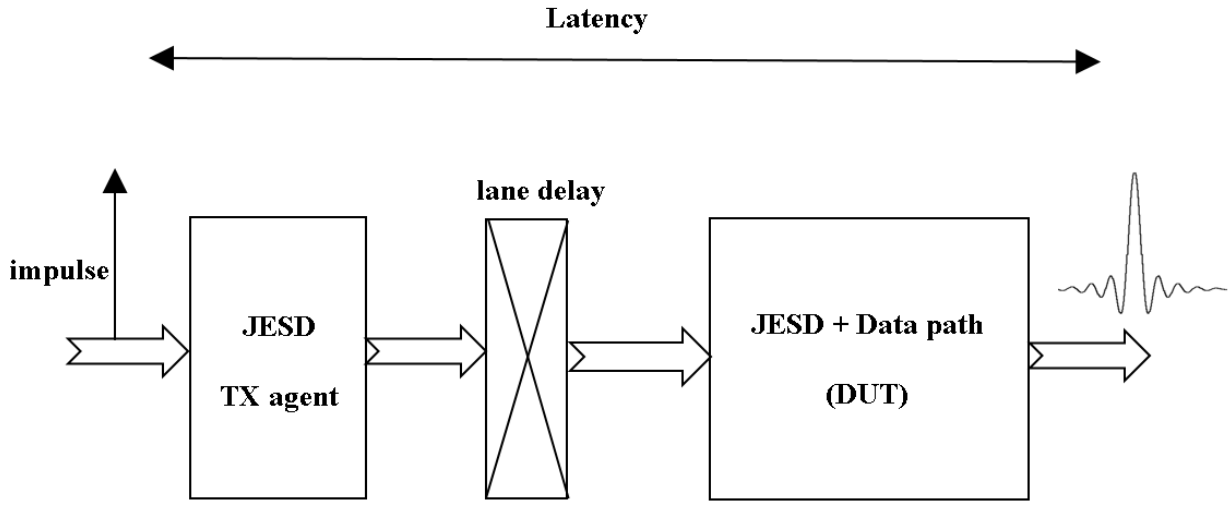

Figure 3. Latency measurement

As the impulse propagates through the up-sampling filters in the data path impulse becomes a sinc function since there are up sampling (low pass) filters in the data path, as shown in the figure 4.

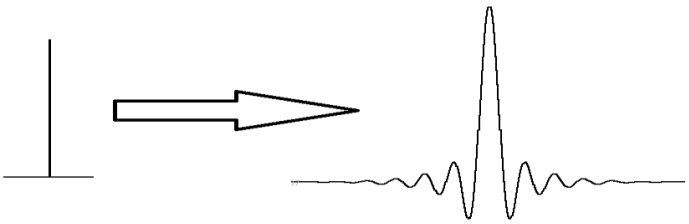

Figure 4. When an impulse is transmitted, it appears as sinc at dac output

The verification flow diagram is shown in figure 5,

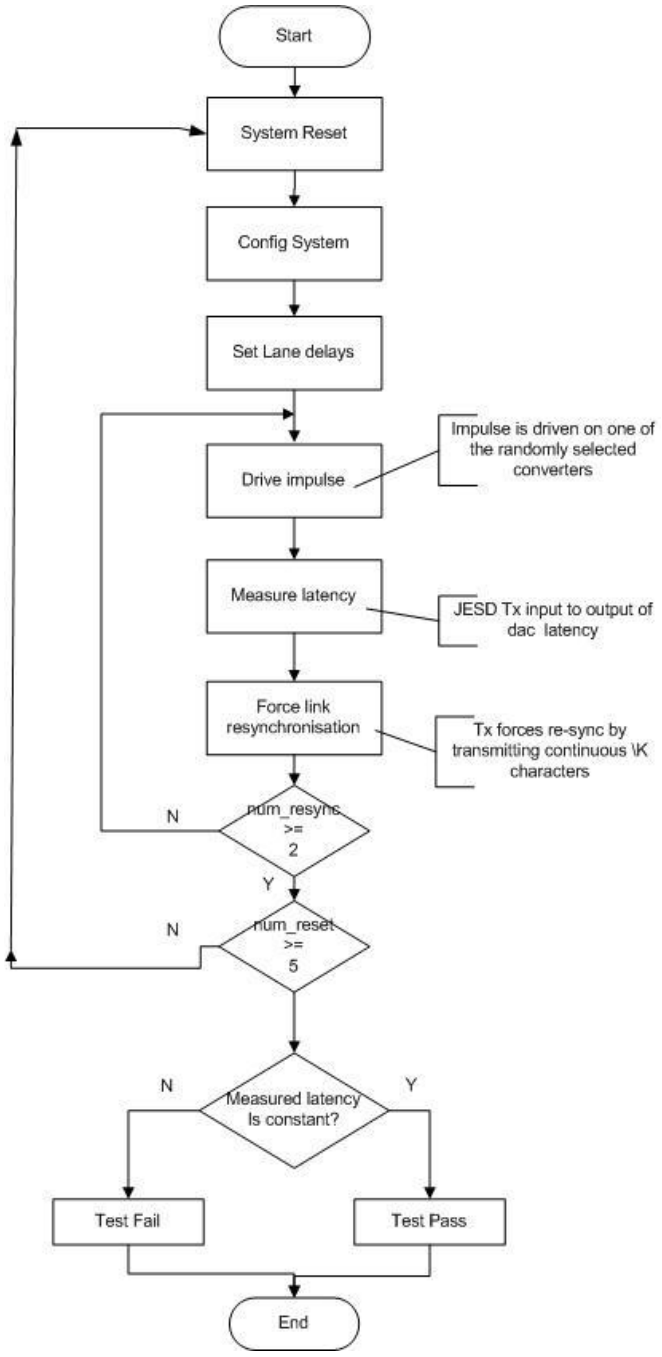

Figure 5. Verification Flow diagram

IV. VERIFICATION ENVIRONMENT

Figure 6 shows the system level verification environment.

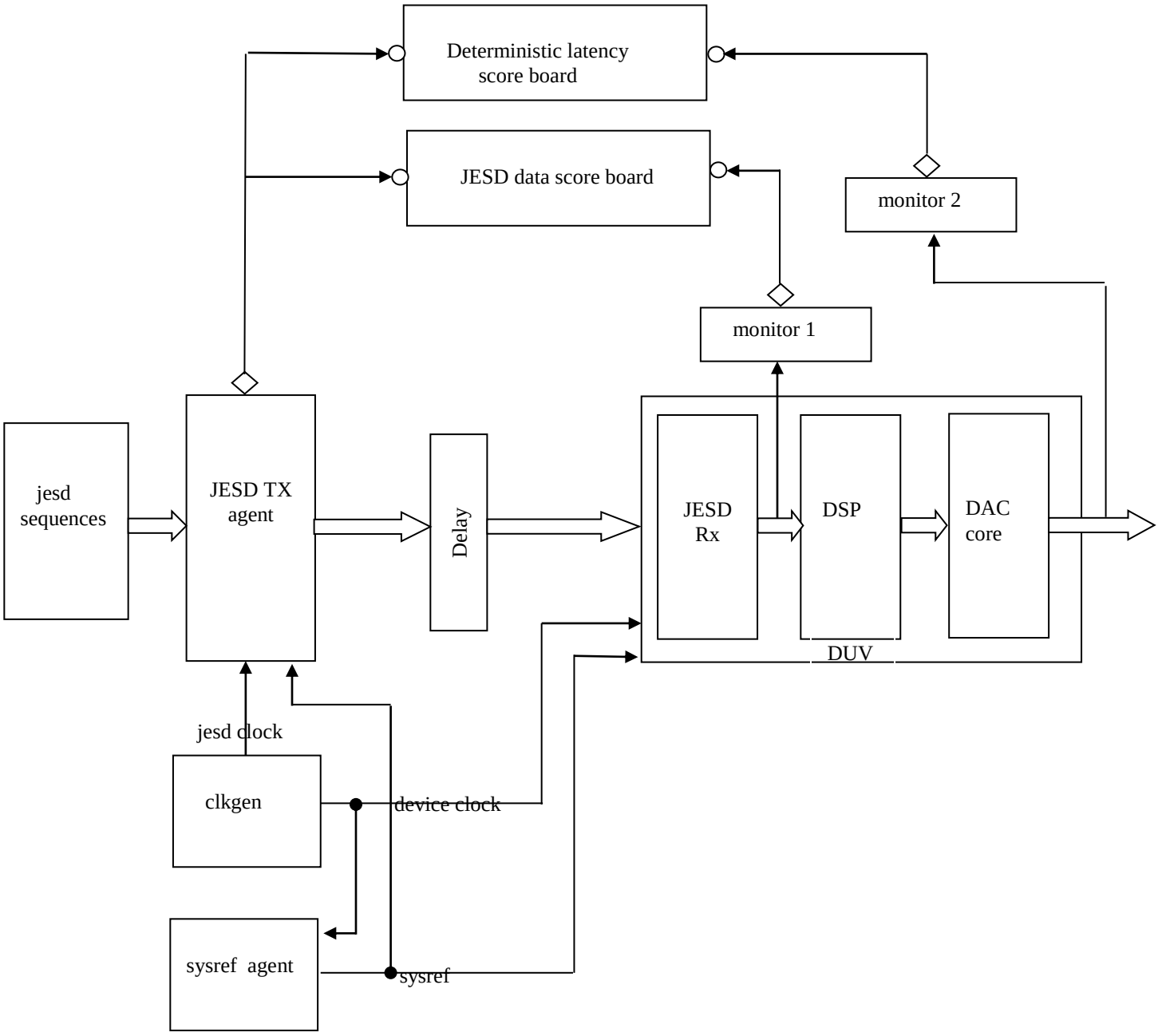

Figure 6. Verification environment

a. **JESD TX agent**: JESD TX agent contains a JESD driver and a JESD sequencers. Driver handle all JESD204B protocol related stuff. It implements all 3 layers of the JESD204B namely transport layer, data link layer and physical layer. Initially the driver keeps sending link initialization sequence. JESD RX indicates the link synchronization through SYNCB signal. After the link is synchronized the driver

sends lane alignment sequence - which helps in aligning all the lanes – as per JESD204B specification. Driver then starts taking user data and maps it to JESD frames and drives on the respective lanes.
Whenever there is a SYSREF pulse JESD TX agent aligns its internal clocks and aligns jesd frames to SYSREF pulse.
This is a fully configurable UVC. All the jesd parameters are configured at the start depending on the design mode.

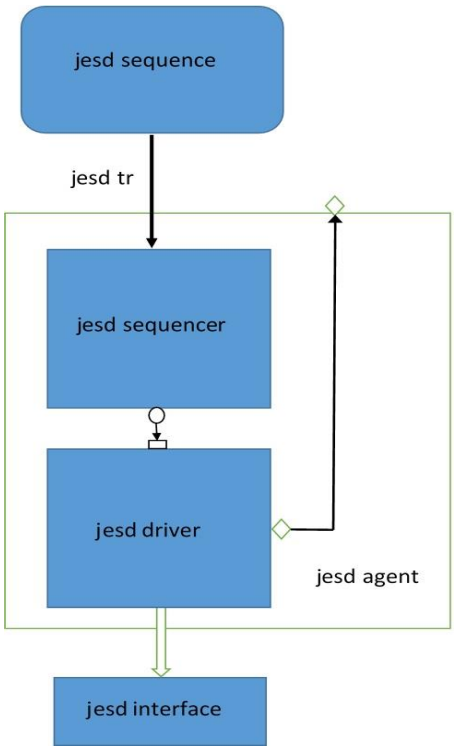

Figure 7. JESD Tx agent

b. **Lane delay modelling:** Delay block models delays on different lane. The delays may be due different wire lengths, SERDES uncertainties – different serdes may start parallelizing data from different reference point, clock phasing related uncertainties, clock domain crossing uncertainties etc. There are up to 8 lanes depending on the mode. The delay values are randomized within permissible range every time the system is powered up. Randomization also takes care of the skew among the lanes.

There are lot of protocols that are tolerant to lane delays within a permissible range. Same logic can be used for modelling lane delays in such protocols as well.

```
constraint c_lane_delay{
    // lane2lane skew is 5 pclks
    foreach(lane_delay[i]){
        lane_delay[i] < (40 * max_lane_delay);
        lane_delay[i] >= 0;

    }
    // link2link skew is upto 10 pclks
    foreach(link_delay[i]){
        link_delay[i] >= 0;

        if(multiple_links)
            link_delay[i] < max_link_delay;
        else
            link_delay[i] == 0;

    }
}
```

Figure 8. lane delay constraints

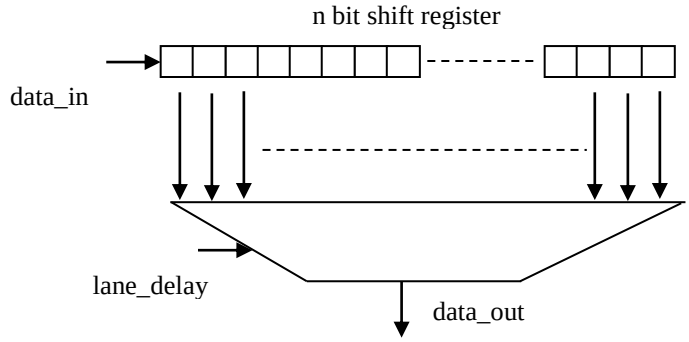

Figure 9. Introducing variable delay

c. **SYSREF agent:** SYSREF agent is responsible for generating the sysref pulses. The period, width and SYSREF mode (i.e. one shot, periodic and gapped periodic) are randomized based on the design modes. The agent generates SYSREF pulses using these random values.

d. **JESD data scoreboard**: There is a data scoreboard at the JESD receiver output. This compares received user data against transmitted user data which helps in verifying data integrity and data ordering. Since this scoreboard is after the transport layer, it doesn't compare/handle protocol related data. This helps in debugging and isolated pre-JESD and post JESD issues.

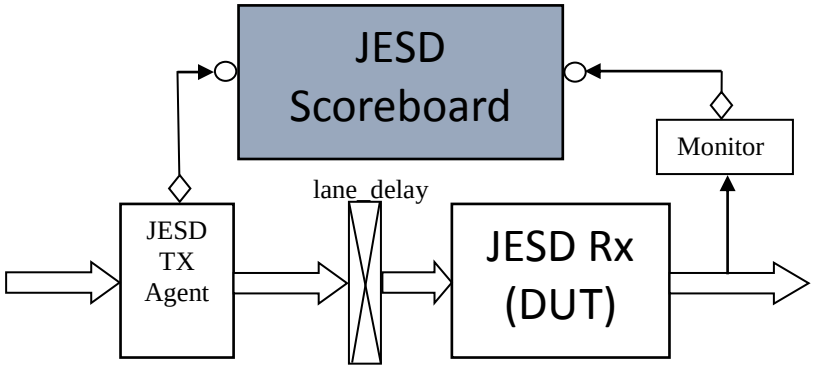

Figure 10. JESD data scoreboard

e. **Deterministic latency scoreboard**: This is used for measuring the latency from JESD transmitter input to dac output. Whenever an impulse is seen on the scoreboard input, it starts a counter. At the dac output it keeps on looking for a sinc waveform. Whenever a sinc waveform peak is detected, it stops the counter. This count value is the latency from JESD TX input to dac output. This scoreboard also supports measuring latencies from JESD TX input to JESD RX parallel output.

III. RESULTS AND CONCLUSION

JESD204B interface now features in a variety of convertor devices. Standardized verification solutions for common issues in such a protocol is a definite advantage. Traditional approaches of manual verification of JESD204B Subclass1 deterministic latency does not scale for larger complexity designs and poses huge risk. The new approach is highly scalable and can be reused across multiple products and on JESD transmitter Designs as well (i.e. for ADCs as well). With this scoreboard approach we were able to find many JESD204B receiver data integrity RTL bugs early in the design cycle with less debug effort. Deterministic latency checker coupled with exhaustive coverage of design modes helped us find critical clocking related issues very easily which could have been missed with visual/directed verification.

This paper demonstrates an approach for the verification of deterministic latency systems. This scheme can be easily extended for the board level testing of deterministic latency. In general, any system/protocol that is invariant to lane delays can use this approach for the verification. Same approach can be used for latency characterization. In our system, we use this scheme to characterize delay variation for different design modes.

REFERENCES

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[4] Demystify Deterministic Latency Within JESD204B converters by Ian Beavers, Applications Engineer, Analog Devices, Inc.