JESD204B Deterministic Latency Verification with UVM Constrained Random Approaches

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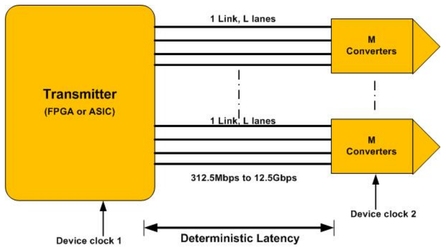
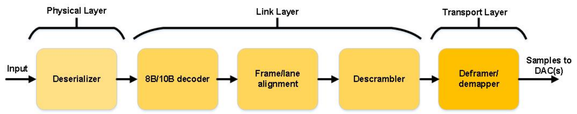
What is JESD204B ?

JESD204B is a JEDEC standard for serial data interfacing. The standard defines a multi gigabit link between a converter device and a logic device such as FPGA or ASIC



JESD204B interface defines three layers,



Phy Layer	Link layer	Transport layer
Physical layer consists of L differential pairs of current mode logic (CML) drivers and receivers. Each lanes support data rates between 312.5Mbps to 12.5Gbps. Physical layer recovers clocks from the 8B10B encoded data and parallelizes the input bit stream.	Data link layer is responsible for establishing the link, initial lane alignment and monitoring the link alignment. There is an 8B/10B encoder/decoder which helps in clock recovery at the receiver and also helps in maintaining DC balance. There is also a scrambler/descrambler block which helps in reducing spectral peaks when same data repeats.	For receivers, transport layer takes 8B10B decoded octets and maps them back to converter samples.

Some of the important signals of interest to us are:

i. **Device clock**: Each converter and transmitter receives their respective device clock from a clock generator circuit which is responsible for generating all device clocks from a common source.

ii. **SYNCB** : it is a return path from receiver to the transmitter synchronous to receiver internal clocks. SYNCB signal is used to indicate receiver synchronization and also used for error reporting to the transmitter.

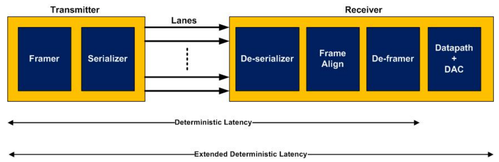
iii. **SYSREF** : SYSREF is the global timing reference for all the components in the system. This signal is used to align all the clocks and also aligns jesd frames in each of the transmitters and converters. This helps in to ensure deterministic latency through the system. SYSREF can be one shot, periodic or gapped periodic.

Deterministic Latency

In a JESD204B system, data is converted to serial and transmitted on the corresponding lanes. Clock relationship between the lanes can be random and each lane can have different delays. Also, there are various data processing elements distributed across different clock domains. These factors contribute to non repeatable latencies across the link from power up to power up cycles and link resynchronization.

Matching the latency variation of all converters in the system for application that use array of converters is a big concern. Any mismatch in latency can degrade the system performance. For systems that use interleaved samples also require the latency to be matched. Systems that use digital pre-distortion (DPD) loops require latency to be deterministic.

JESD204B provides mechanisms to establish deterministic latency for all converters in the system. Deterministic latency is defined as the time it takes for the parallel input data to propagate from transmitter input to parallel data output at the receiver. This time is measured in frame clocks or device clocks.



This latency is expected to be constant over power cycles and link resynchronization events and also the latency should be programmable.

SYSREF aligns all clocks in each of the converters and logic devices and the frame boundaries are communicated to the receiver by control characters. Each receiver can decode the placement of the transmitter frame relative to its own clocks and also relative to all transmitters. This enables the receiver to de-skew the data on different links with different delays using delay buffers and the de-skewed data is sent out on the next frame boundary.

Verification Challenge

Since deterministic latency involve multiple modules like SYSREF sampling, clock generation, JESD Rx etc, verification of this feature is very critical and challenging.

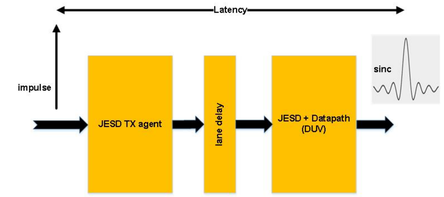
Multi channel data path with multi phased clocking and clock gating, requires one to ensure latency is constant from Tx parallel input to DAC output across power cycles (i.e. **extended deterministic latency**)

Traditionally, this is verified by visually checking the waveform. This method is not scalable, tedious (especially when you have lot of JESD operational modes) and error prone.

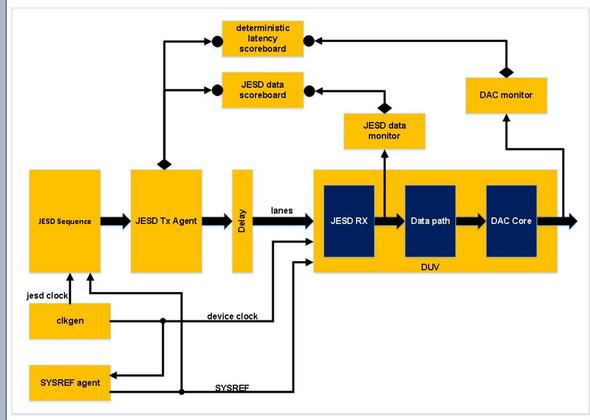
Proposed Solution

System latency from JESD TX parallel data input to DAC output is characterized by using impulses. An impulse is sent on one of the randomly chosen channels. The time taken for the impulse to propagate through JESD TX, JESD RX, and data path and appear at the DAC output is the latency of the system. Same procedure is repeated couple of times. Hardware reset is asserted between each iterations and also link is re synchronized between the iterations.

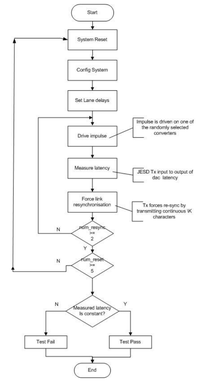
As the impulse propagates through the up-sampling filters in the data path, impulse becomes a sinc function since there are up sampling (low pass) filters in the data path.



Verification Environment



Verification Flow



Verification Environment (contd)

i. **Lane delay modelling**: Delay block models delays on different lane. The delays may be due different wire lengths, SERDES uncertainties, different SERDES may start parallelizing data from different reference point, clock phasing related uncertainties, clock domain crossing uncertainties etc. The delay values are randomized within permissible range every time the system is reset. Randomization also takes care of the skew among the lanes.

ii. **Deterministic latency scoreboard**: Used for measuring the latency from JESD transmitter input to DAC output. Whenever an impulse is seen on the scoreboard input, it starts a counter. At the DAC output, it looks for a sinc waveform. Whenever a sinc waveform peak is detected, counter is stopped. This count value is the latency from JESD TX input to DAC output. This scoreboard also supports measuring latencies from JESD TX input to JESD RX parallel output.

iii. **JESD data scoreboard**: There is a data scoreboard at the JESD receiver output. This compares received user data against transmitted user data which helps in verifying data integrity and data ordering. This helps in debugging and localizing errors.

iv. **SYSREF agent**: SYSREF agent is responsible for generating the SYSREF pulses. The period, width and SYSREF mode (i.e. one shot, periodic and gapped periodic) are randomized based on the design modes. The agent generates SYSREF pulses using these random values.

v. **JESD TX agent**: JESD TX agent contains a JESD driver and a JESD sequencers. Driver handle all JESD204B protocol related stuff. It implements all 3 layers of the JESD204B namely transport layer, data link layer and physical layer.

Results

i. Traditional approaches of manual verification of JESD204B Subclass1 deterministic latency does not scale for larger complexity designs and poses huge risk. The new approach is highly scalable and can be reused across multiple products and on JESD transmitter Designs as well

ii. With this scoreboard approach we were able to find many JESD204B receiver data integrity RTL bugs early in the design cycle with less debug effort.

iii. Deterministic latency scoreboard coupled with exhaustive coverage of design modes helped us find critical clocking related issues very easily which could have been missed with visual/directed verification.

Conclusion

i. Demonstrates an approach for the verification of deterministic latency systems.

ii. This scheme can be easily extended for the board level testing of deterministic latency.

iii. Any system/protocol that is invariant to lane delays can use this approach for the verification.

iv. Same approach can be used for latency characterization. In our system, we use this scheme to characterize delay variation for different design modes.