DESIGN & VERIFICATION DVCON 2014 CONFERENCE & EXHIBITION

Interpreting UPF for a Mixed-Signal Design Under Test

Mentor Graphics®

30 Sec Intro to UPF

- UPF is a format for specifying the power topology of an HDL description in a manner independent of the functional description
- What new problems arise for the AMS extension?

Two New Problems

1. A-D boundaries must be sensitive to drivers and receivers

2. UPF power sources and power control must take in to account the analog power sources and sinks of AMS elements

These problems do not arise in homogeneous digital or homogeneous electrical design hierarchies

Assumptions/Constraints

- AMS models are never *implicit*: they always have power ports, and the connection is *explicit* or *automatic*
- Communication is through the UPF *supply_net_type* digital type
- AMS blocks are always leaf-level elements
- They appear in the guise of digital blocks from the instantiating context

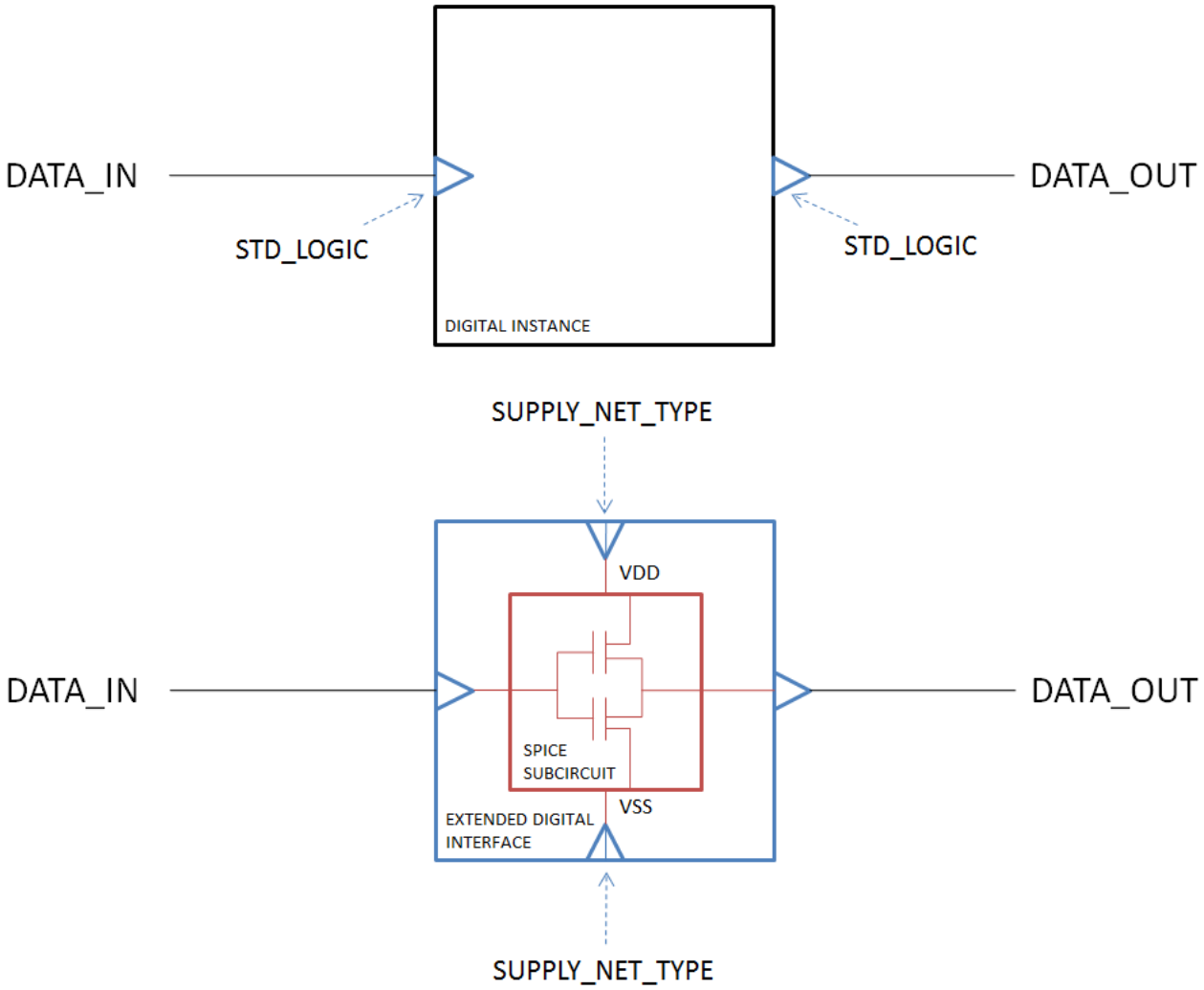
Use Model

- Given an existing power-aware design described by a homogeneous digital hierarchy and an accompanying UPF file….
- Substitute an AMS model instance with electrical ports.
- The AMS model has electrical ports that correspond one-for-one to the ports of the replaced digital instance

Use Model (continued)

- The AMS model will have electrical ports are power ports
- They can supply power to the analog sub-circuit within the model
- They can be supply sources for a UPF power net

Replacement of the Digital Component



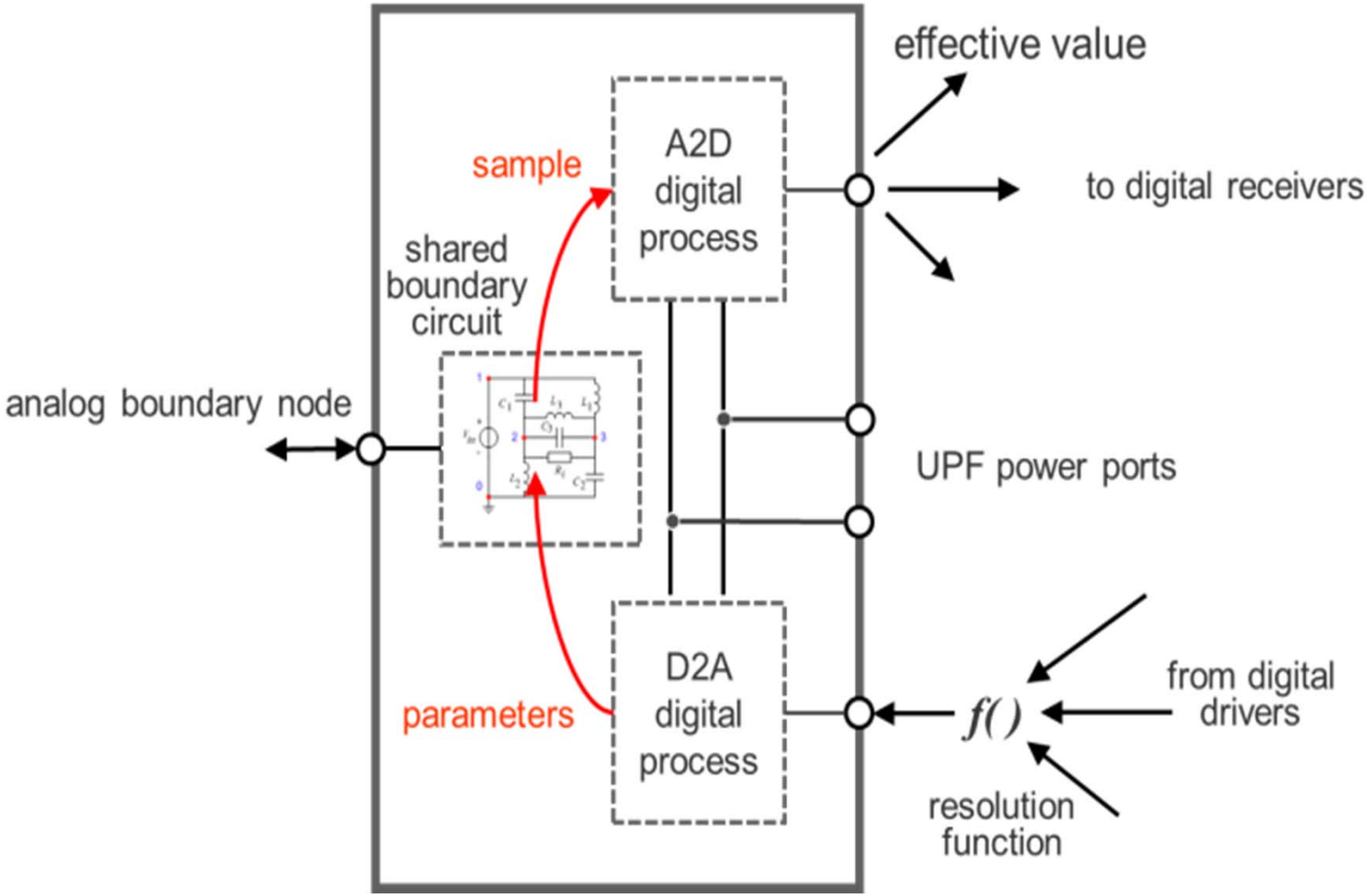
Digital Interface

```
Library IEEE;
use ieee.upf.all, IEEE.Std_logic_1164.all;
entity inv is
   PORT (inp : in Std_logic;
         outp : out Std_logic;
         VDD : in supply_net_type;
         VSS : in supply_net_type);
   attribute UPF_pg_type of
      VDD : signal is "primary_power";
   attribute UPF_pg_type of
      VSS : signal is "primary_ground";
end;
```

The Power-Sensitive Signal Boundary Element

- Interpretation of analog voltage as a logic value
- Interpretation of logic state as a voltage source
- Both must take into account the power state of the digital side of the connection

General Model of a Power-Sensitive Signal Boundary Element



Power Pins and Power Boundary Elements

- An element of an AMS hierarchy may have analog power pins
- In the RTL context, there are no explicit power nets that correspond

Power to Electrical Boundary Element

- If the instance needs power, power supplies must be created and connected
- We interpose a *power-to-electrical boundary element* (P2E)

```
entity P2E is
  generic (Voff  : Real := 0.0;
           Vund  : Real := 0.0;
           trise : Real := 50.0e-12;
           tfall : Real := 50.0e-12);
  port (signal upfin : in supply_net_type;
        terminal vdd  : electrical;
        terminal vss  : electrical);
end entity P2E;
```

Electrical to Power Boundary Element

- If the instance is a *supply driver*, power information must be encoded in UPF format
- We interpose an *electrical-to-power boundary element* (E2P)

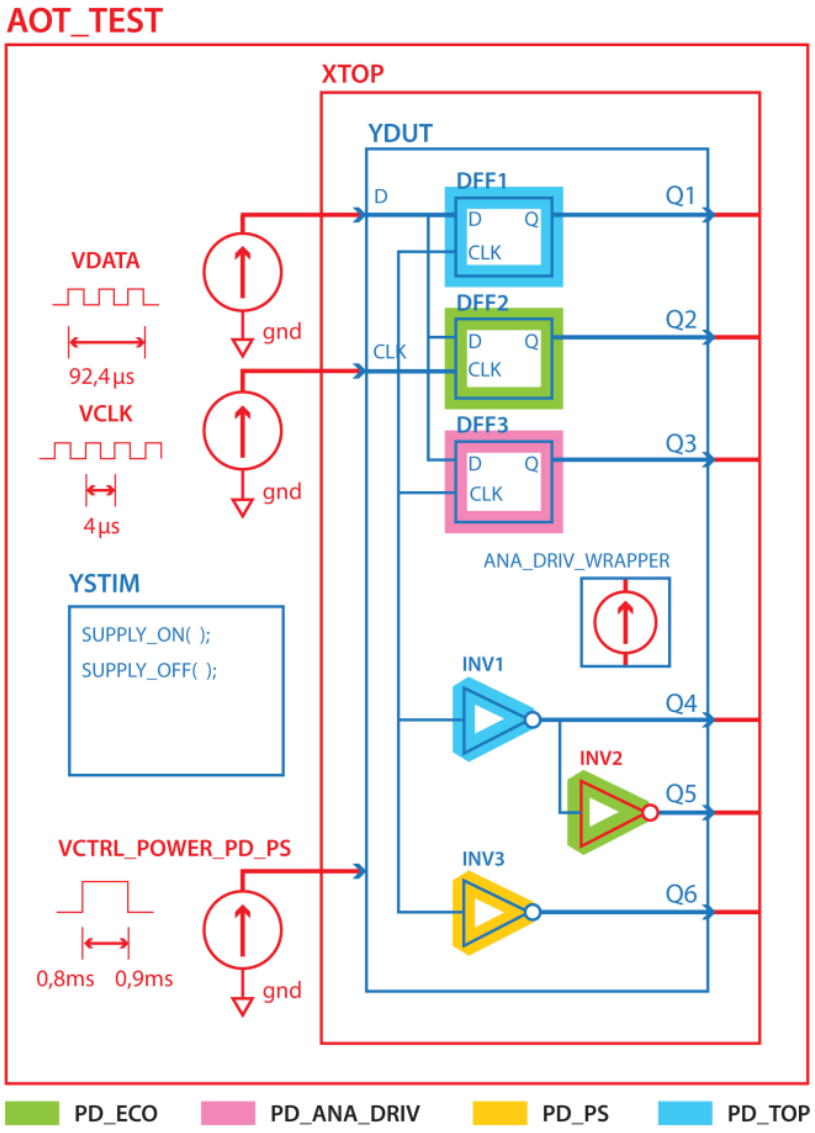
```
entity E2P is
  generic (voff : real := 0.2;
           von  : real := 0.5;
           eps  : real := 1.0e-3);

  port (signal upfout : out supply_net_type;
        terminal vdd : electrical;
        terminal vss : electrical);
end entity E2P;
```

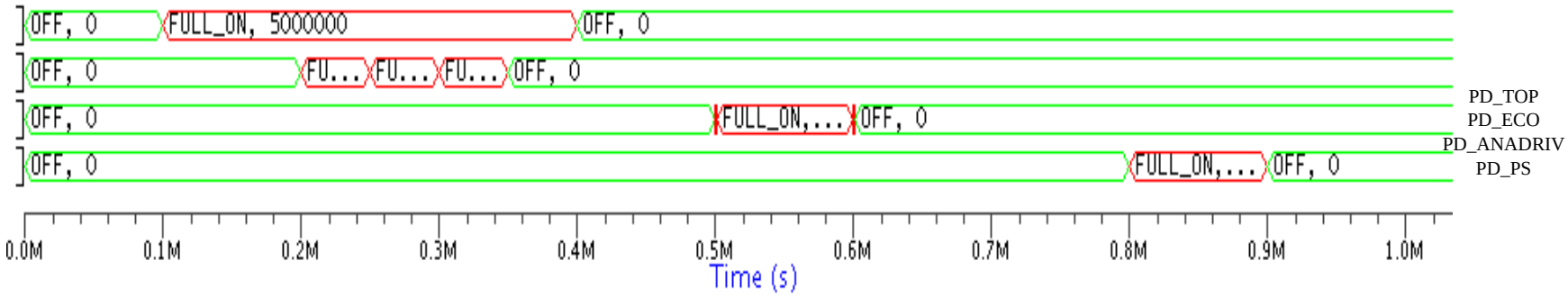
The Design Under Test

Structure - Default

Instance	Design unit	Design unit ty
aot_test	Top SPICE	Model
vclk	-	Device
vdata	-	Device
vctrl_power_pd_ps	-	Device
xtop	top_subckt	Subckt
ydut	top	Module
dff1	dff	Module
dff2	dff	Module
dff3	dff	Module
inv1	inv	Module
inv2	inv	Subckt
inv3	inv	Module
ana_driv_wra...	ana_driv	Subckt
ystim	Stim	Module
#ublk#371453...	Stim	Statement

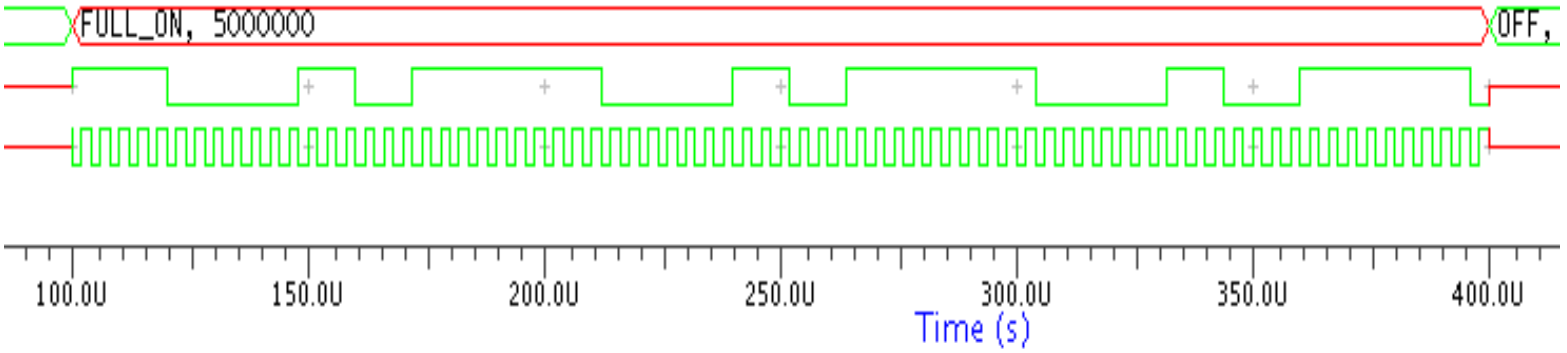


Power Regime



Chronogram of the switching regime for the power domains

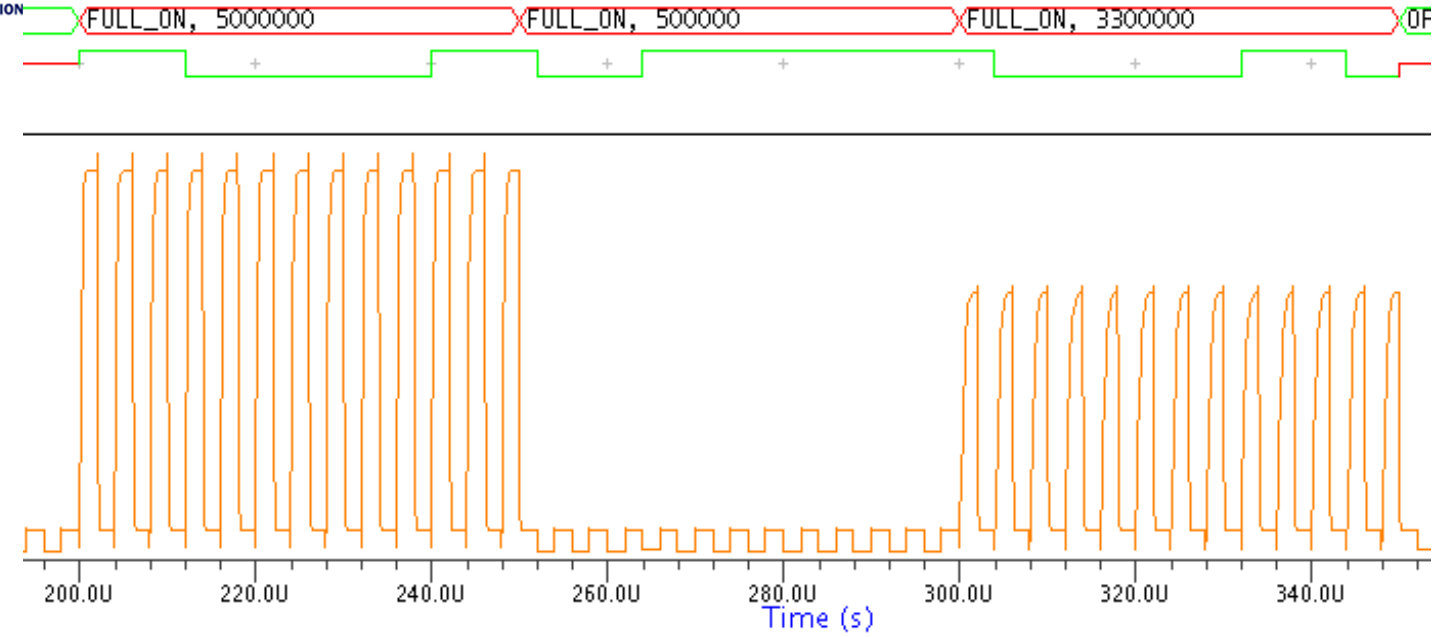
Test 1



At 100 µs power domain *pd_top* turns on and the outputs of *dff1* and *inv1* become valid.

Both *dff1* and *inv1* are digital modules governed by normal UPF implicit rules.

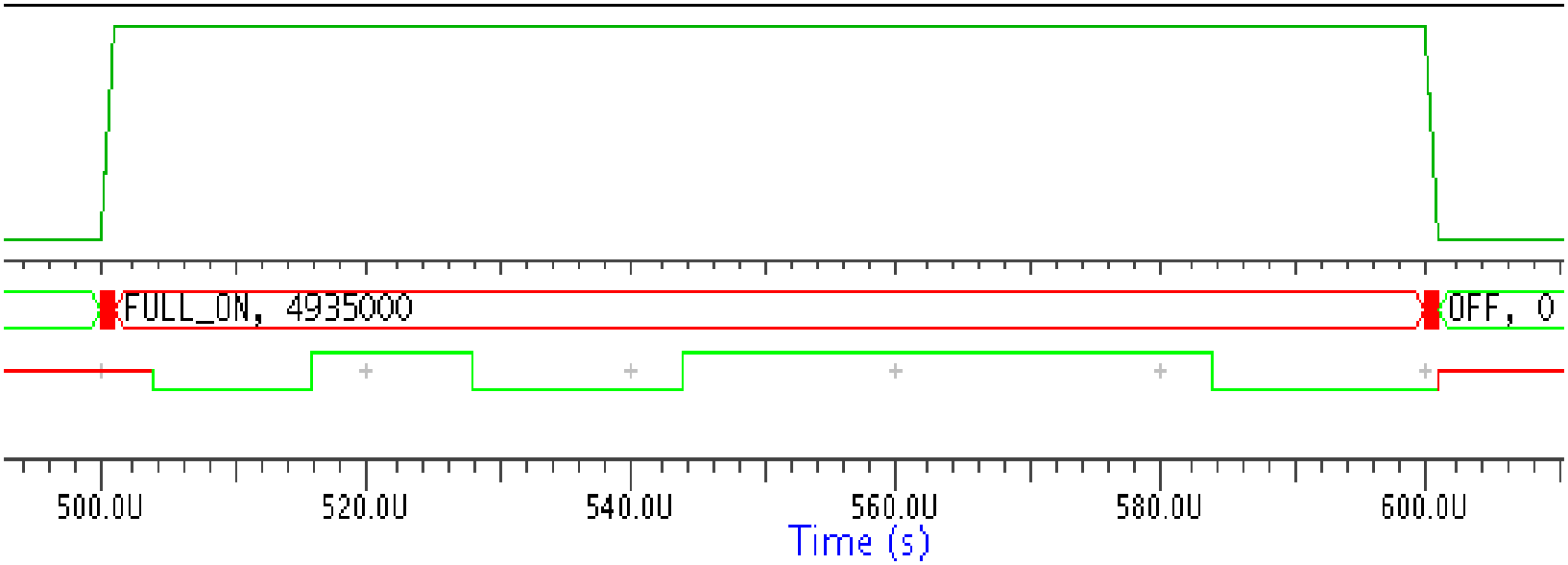
Test 2



Test 2 modulates primary power in PD_ECO, which contains DFF2 and INV2

INV2 uses power supplied by P2E boundary elements inserted at elaboration time

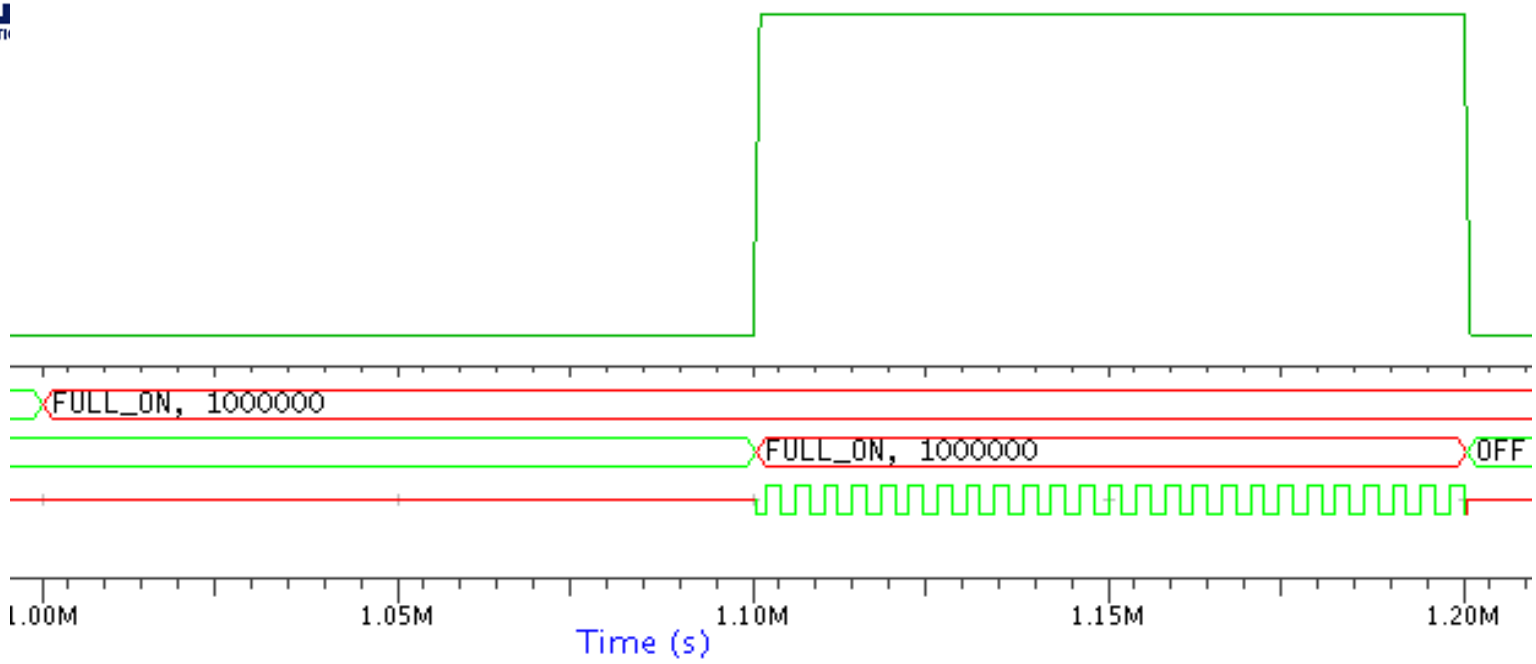
Test 3



A SPICE sub-circuit *ana_driv* provides primary power to domain PD_ANADRIV

Digital module DFF3 is in PD_ANADRIV

Test 4



The power domain PD_PS is governed by the output of a UPF switch

Summing Up

- An interpretation of UPF for mixed-signal
- Two important extensions :
  - A method for providing UPF-controlled, SPICE-level power to those AMS instances that require it
  - A method for defining signal connect elements (connect modules) that are sensitive to the power state of the enclosing UPF power domain