Integrating a Virtual Platform Framework for Smart Devices

V. Guarnieri[1], F. Stefanni[1], F.Fummi[1]

M. Grosso[2], D. Lena[2]

A. Ciccazzo[3], G. Gangemi[3], S. Rinaudo[3]

1

2

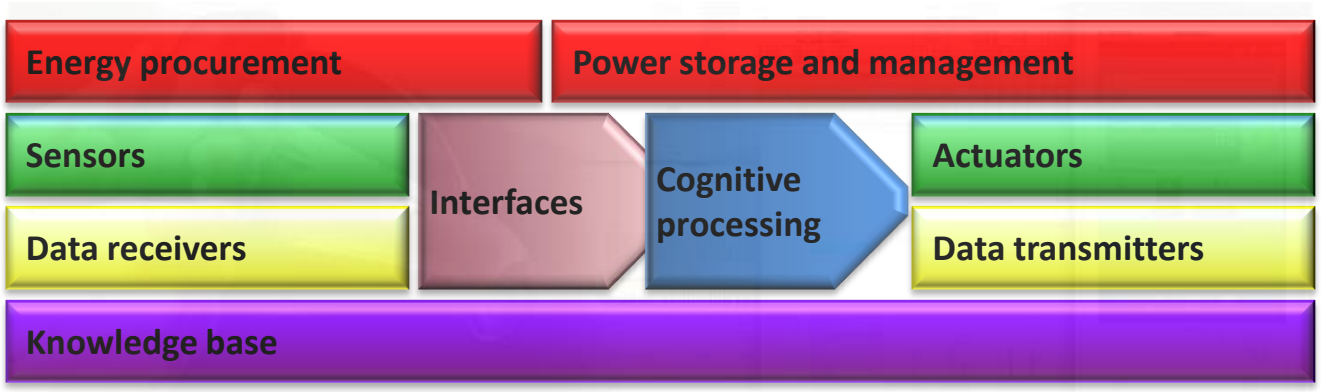
3

Outline

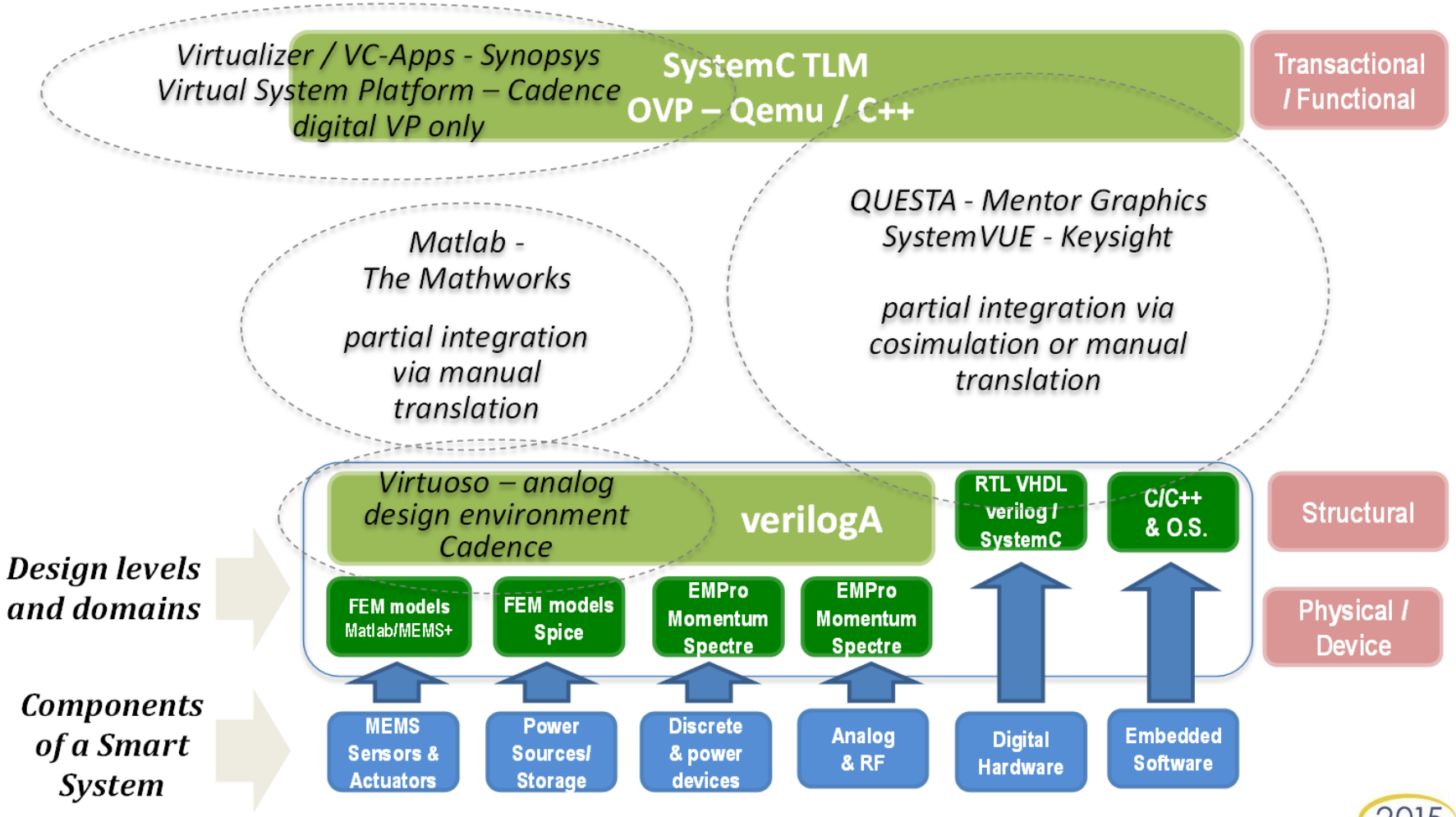
- Introduction
- HIFSuite
- Testcases
- Abstraction results
- Conclusion

What is a smart system?

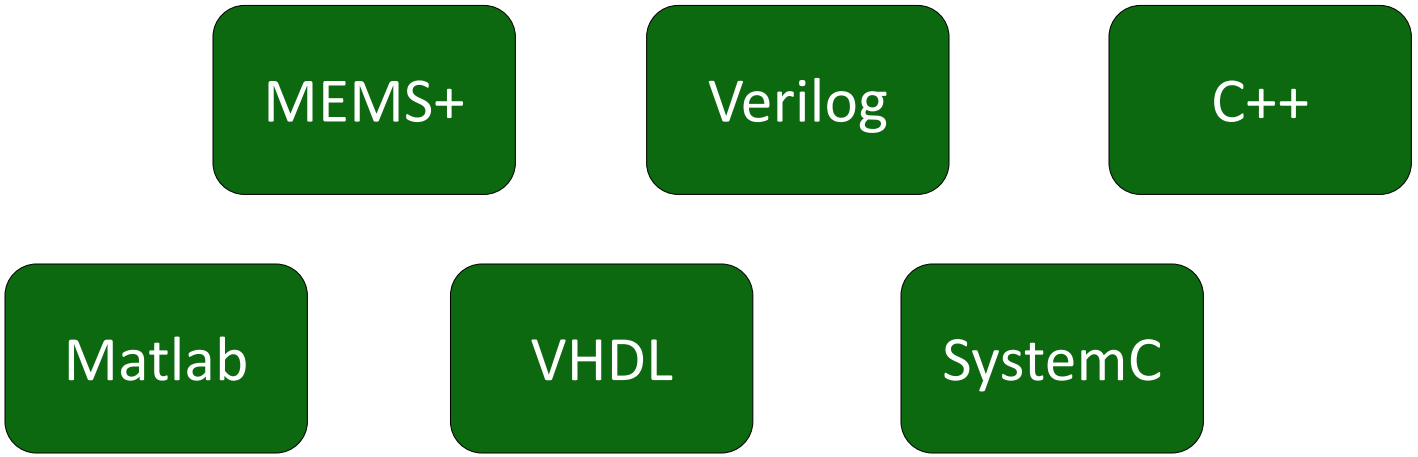
- Miniaturized self-sufficient device
  - incorporating functions of sensing, actuation and control
  - able to describe and analyze a situation
  - able to decide according to available data
  - Energy-autonomous and ubiquitously connected



Smart system design

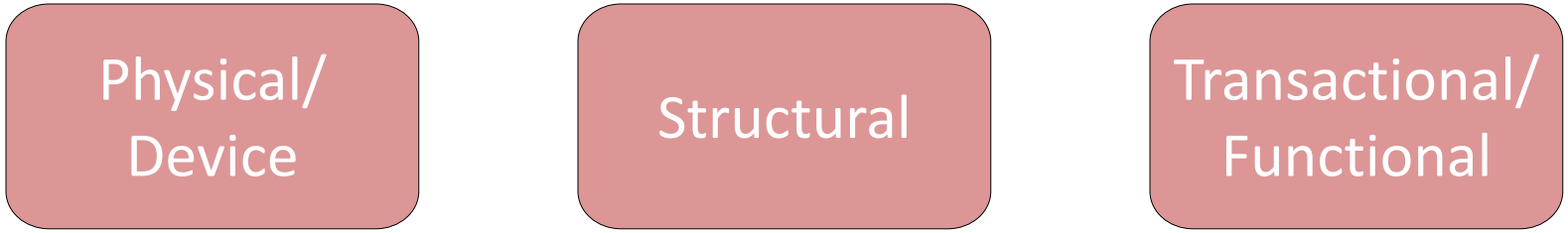


Issues in smart system design (I)



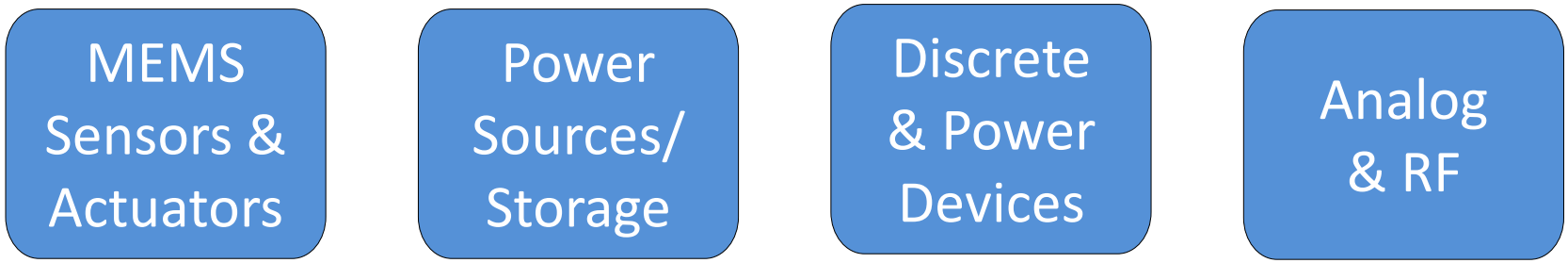
- Extremely heterogeneous representations for the various components → co-simulation
  - Poor simulation performance
  - Manual translation required

Issues in smart system design (II)



- Too low design level to provide a global view of the entire system
  - Typical design levels: physical/device, structural
  - Global view should be at least functional or transactional
  - Manual abstraction required

Issues in smart system design (III)



- Analog and mixed-signal components
  - Difficult to integrate into higher-level systems, but …
  - Absolutely required in smart systems
  - Multi-dimensional circuit sizing and verification problems → circuit analysis and automated optimization algorithms required

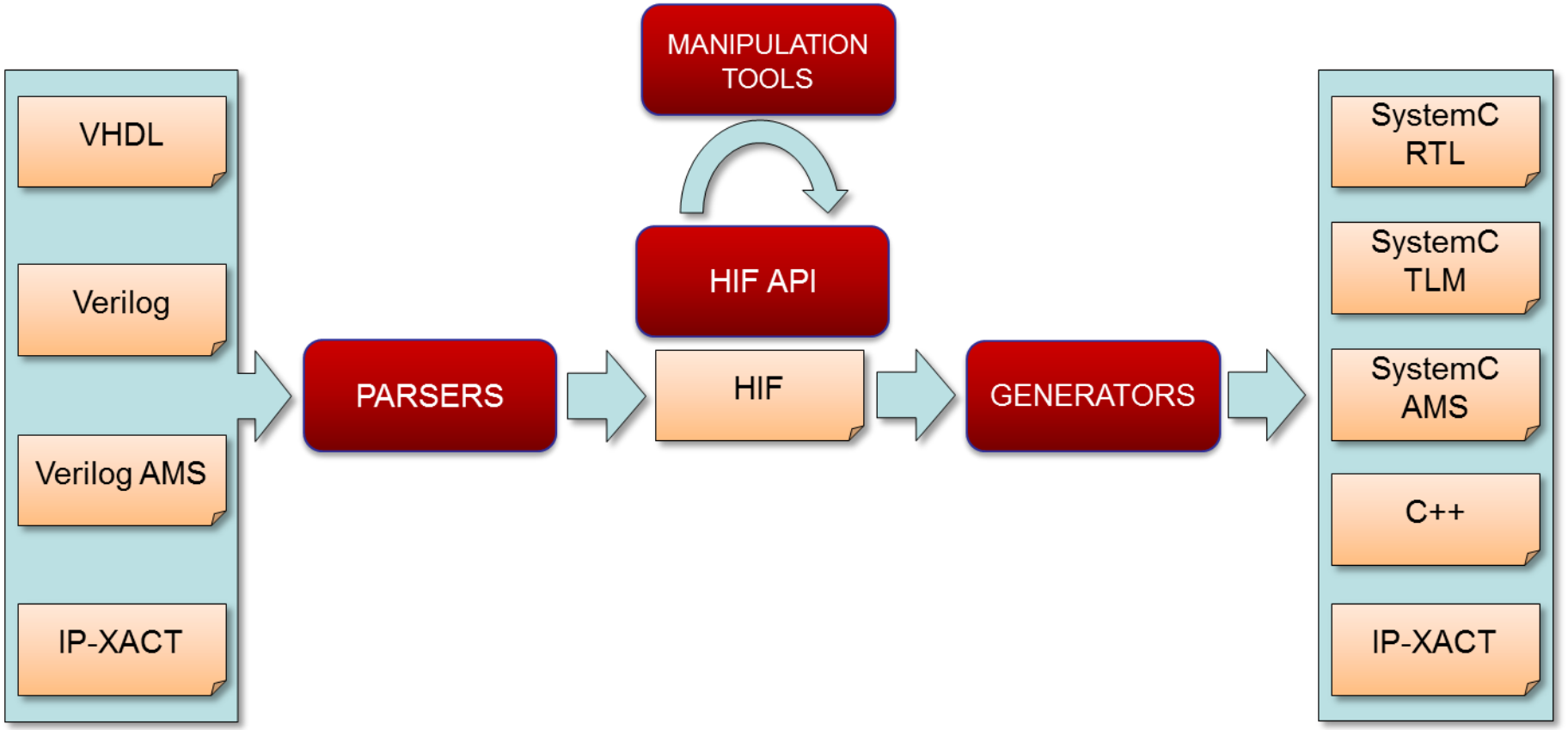
Possible solutions

- Heterogeneity of smart systems → homogeneous models
- Co-simulation techniques → simulation techniques
- Enhancing reuse through abstraction and systems aggregators
- Concurrent simulation of functional and extra-functional properties

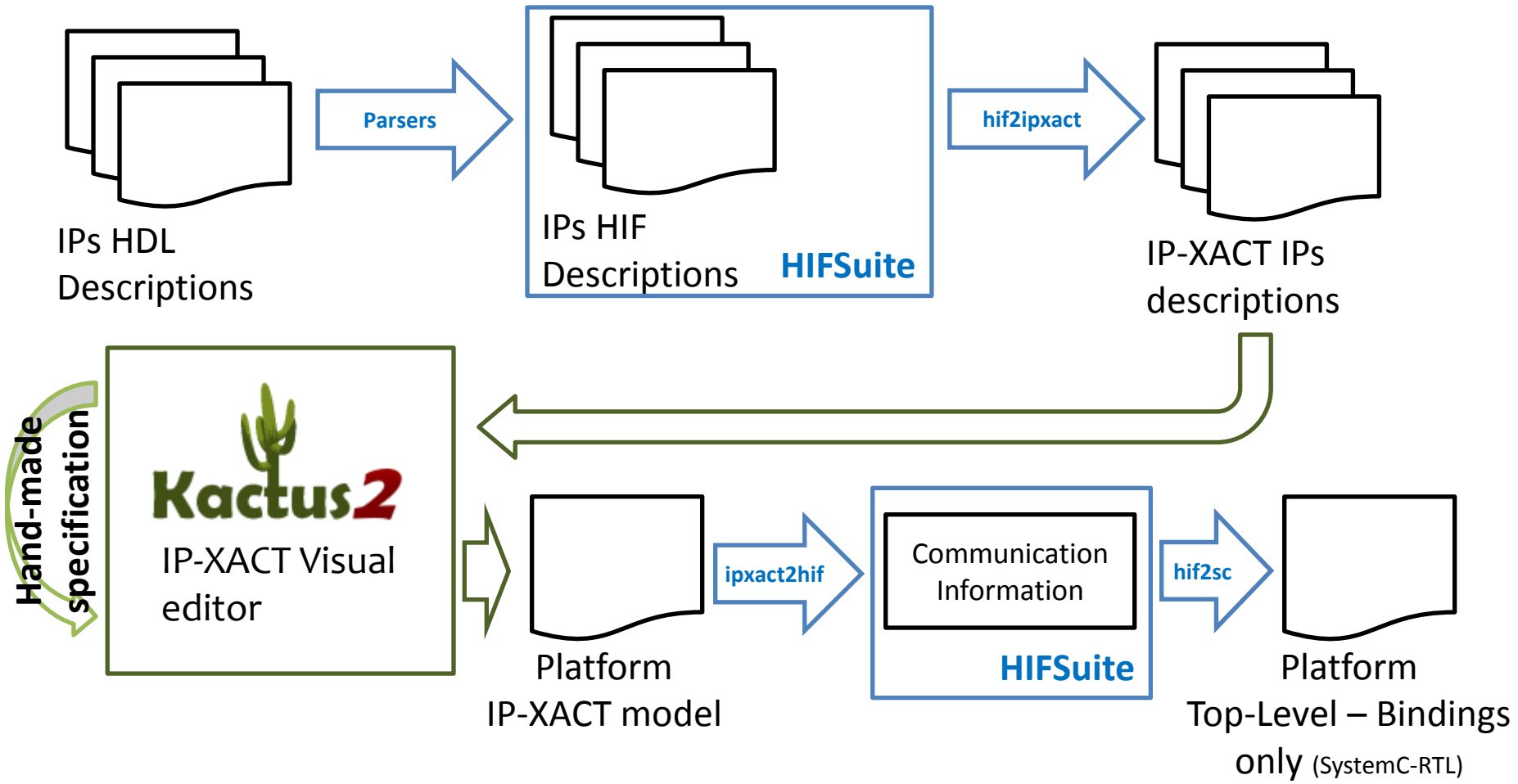
Proposed solution

- Integration of heterogeneous components into a homogeneous virtual platform
  - Components written in different languages and belonging to different domains
- Optimization of the homogeneous description for simulation
  - Towards a full C++ model
- Design of each component with the most suited tool
  - Homogeneous platform to evaluate functional and extra-functional properties

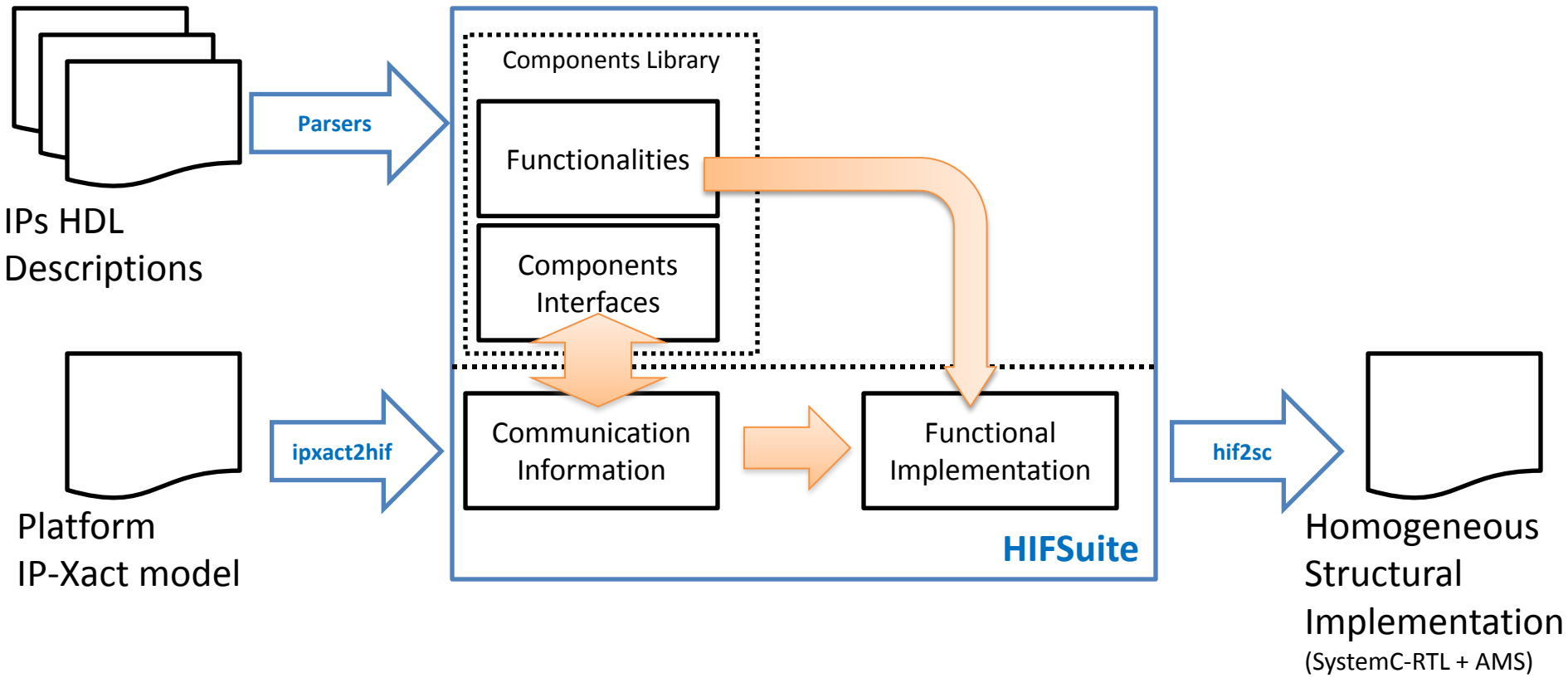
HIFSuite



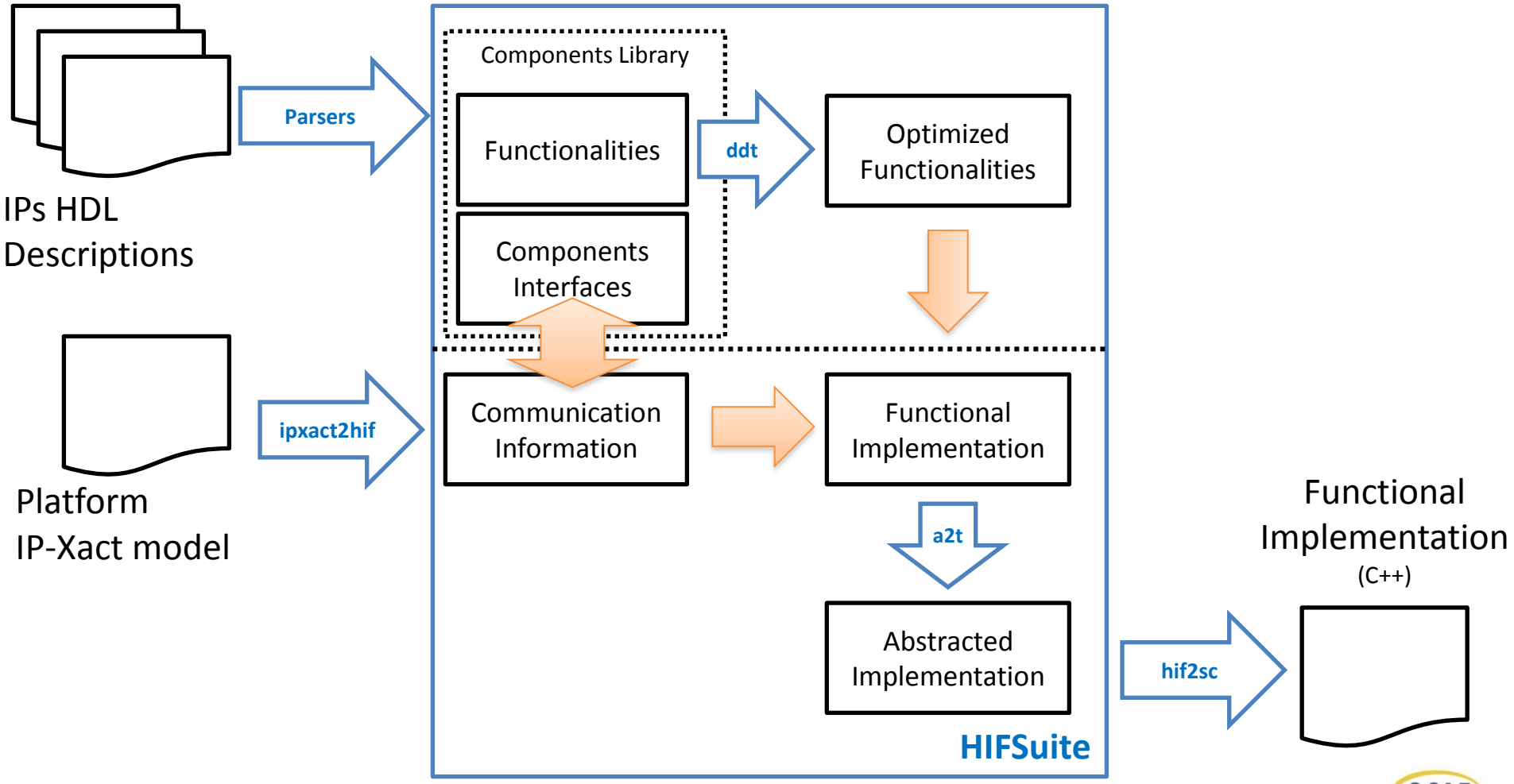
Step 1



Step 2



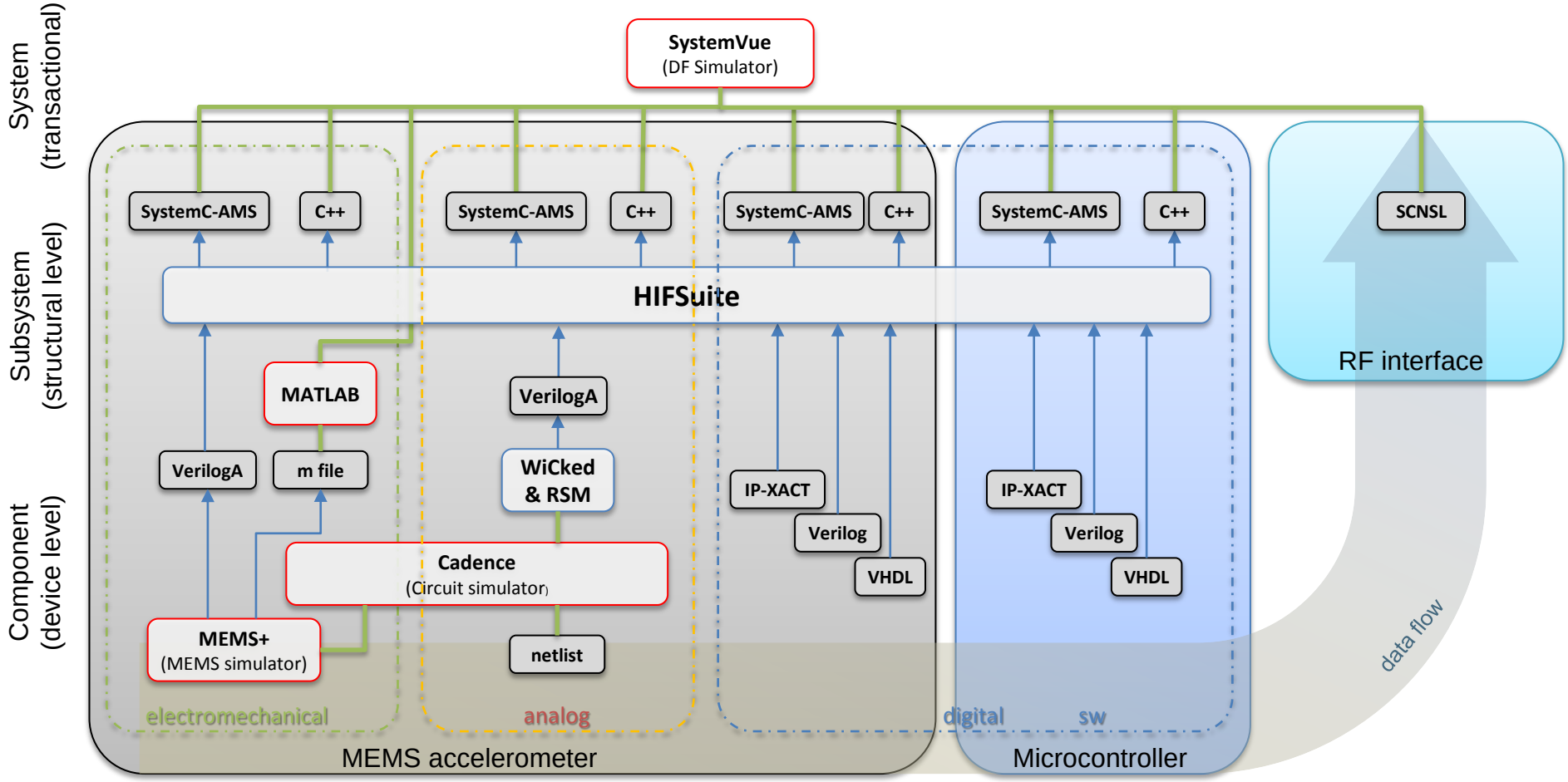
Step 3


IPs HDL Descriptions
Parsers
Components Library
Functionalities
Components Interfaces
ddt
Optimized Functionalities
Platform IP-Xact model
ipxact2hif
Communication Information
Functional Implementation
a2t
Abstracted Implementation
HIFSuite
hif2sc
Functional Implementation
(C++)

Testcases

- Two testcases provided by ST
  - Modular sensor node: monitoring of human gestures or movement
  - Enhanced LED driver engine: implementation of smart lightning modules
- Working prototypes, not marketed products
- Typical EDA challenges in
  - System-level design
  - MEMS-design
  - Analog-mixed signal-design

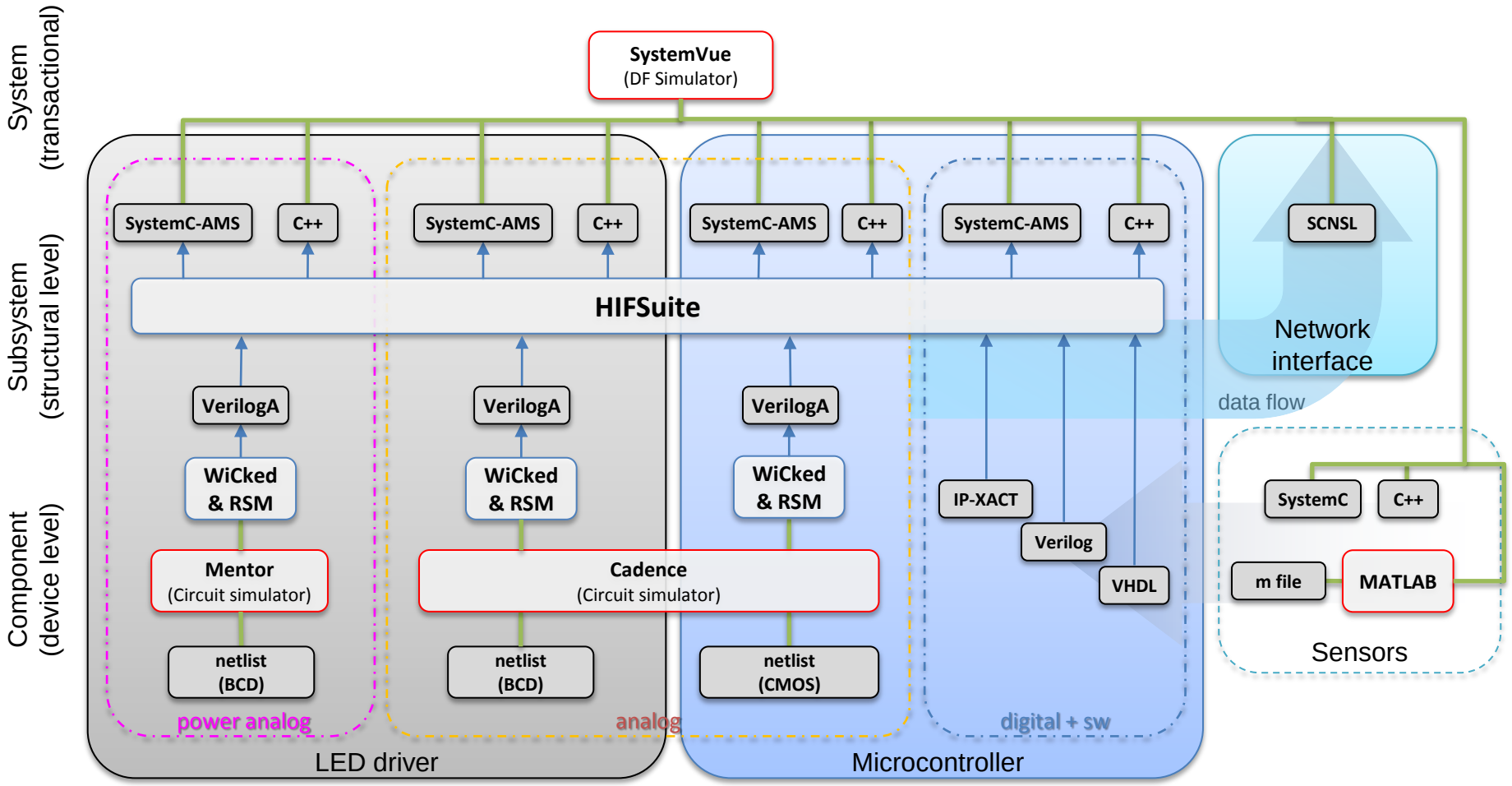
Modular sensor node (I)



Modular sensor node (II)

- Analog design domain
  - HIFSuite: VerilogA → SystemC-AMS
    - SystemC-AMS description to be used in system-level simulation
    - Avoiding co-simulation
- Digital design domain
  - HIFSuite: RTL → SystemC TLM or C++
    - Mitigating bottlenecks in system-level simulation due to complexity
- System-level model advantages
  - Performance evaluation under realistic workloads

Enhanced LED driver engine (I)



Enhanced LED driver engine (II)

- Full-system simulation advantages
  - Better understanding of sub-systems interactions
  - Deep investigation of the microcontroller capabilities and peripherals usage
    - Early addressing performance issues and firmware optimization
  - Optimization of power modes
  - Correct interoperability between sub-systems
  - Anticipation of issues during design phase → reduction of development costs

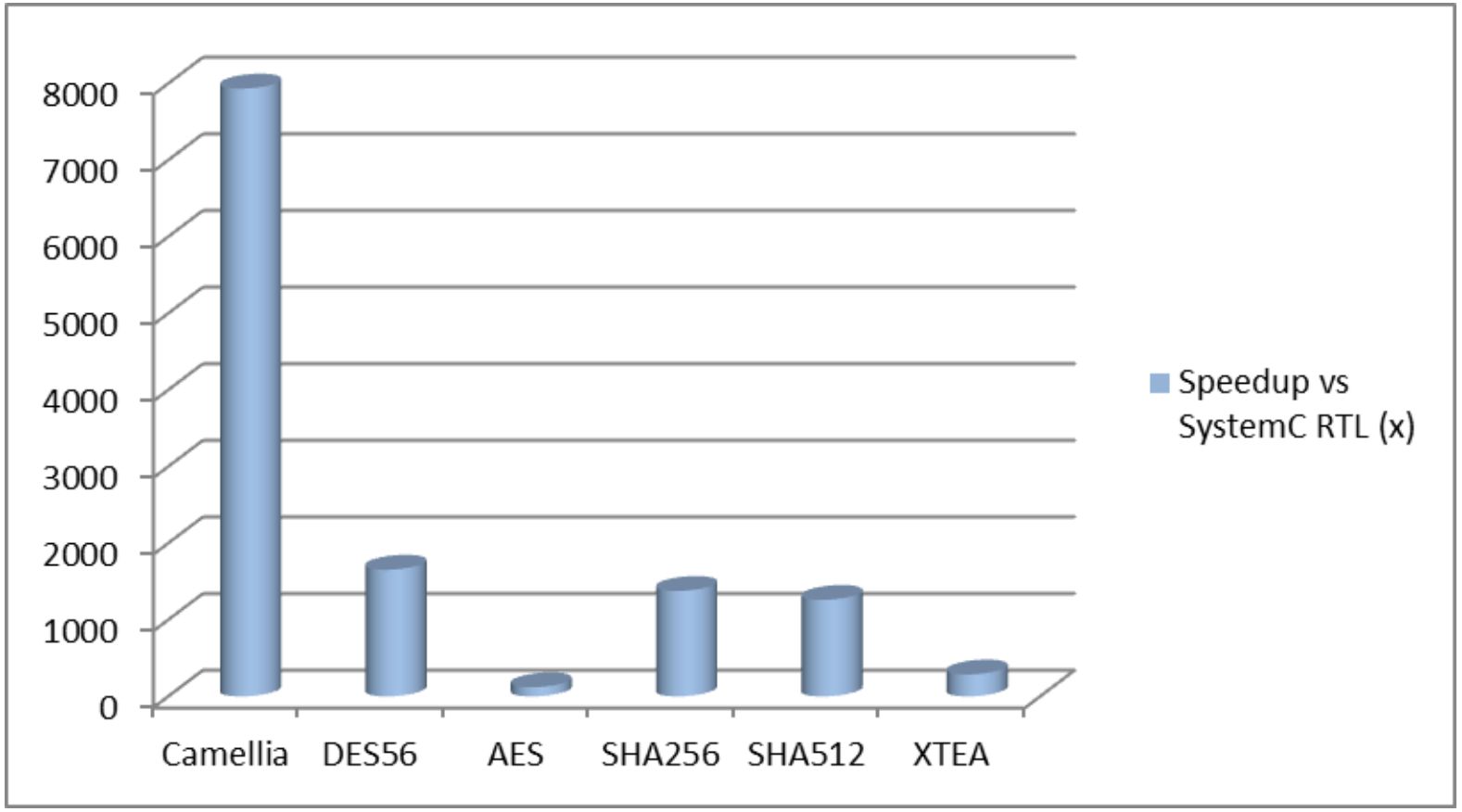
Abstraction

- Process scheduler
  - Classical HDL process scheduler → more performing process scheduler
- Data types
  - Original HDL data types → C++ built-in data types
- Interface
  - RTL interface → TLM or C++ interface

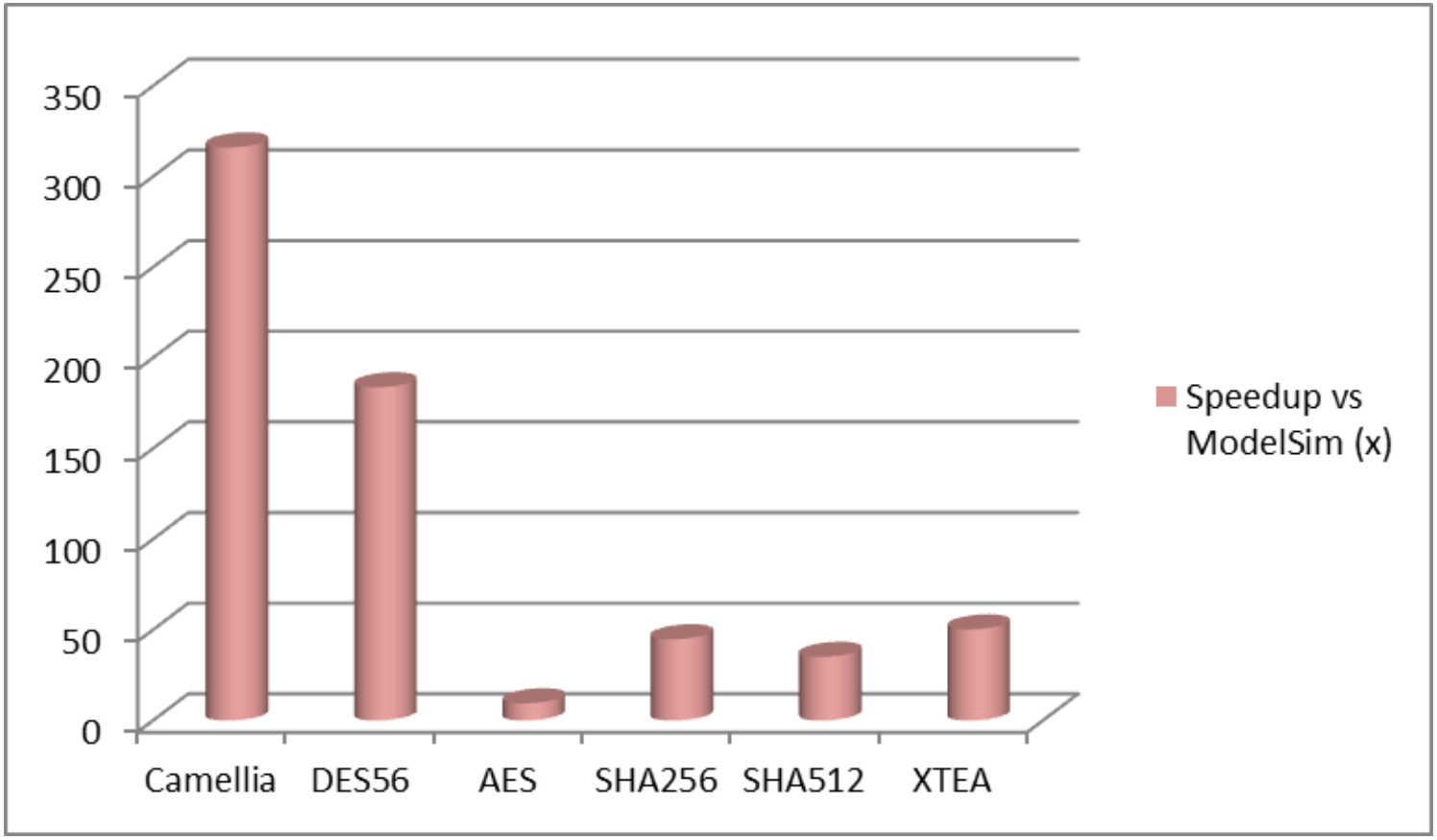
Abstraction results (I)

Design	SystemC RTL (s)	ModelSim (s)	Abstracted C++ (s)	Speedup vs SystemC RTL (x)	Speedup vs ModelSim (x)
Camellia	26,974.8	1,074.7	3.4	7,933.8	316.1
DES56	7,112.2	790.4	4.3	1654.0	183.8
AES	850.9	67.5	7.1	119.8	9.5
SHA256	4,682.5	152.4	3.4	1,377.2	44.8
SHA512	6,302.1	175.6	5.0	1,260.4	35.1
XTEA	975.2	170.9	3.4	286.8	50.3

Abstraction results (II)



Abstraction results (III)



Conclusions

- HIFSuite assists designers of smart devices
  - Translation of heterogeneous descriptions of components into homogeneous SystemC description
    - No need for co-simulation
  - Abstraction to C++ to enhance simulation performance
  - Reuse of existing IPs and integration into virtual platforms
    - Design space exploration
    - Design validation
    - Performance evaluation
  - Reduction of time to market

Thanks for your attention!

Questions?

accellera SYSTEMS INITIATIVE

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE