2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

IEEE 1801 Assisted Custom IP Development and Low Power Checks Using Cadence Virtuoso Power Manager

Dr. Matthias Steffen, Infineon Technologies, Munich, Germany (*matthias.steffen@infineon.com*)

Amit Chopra, Cadence Design Systems Inc., San Jose, United States (achopra@cadence.com)

Sonal Singh, Cadence Design Systems (I) Pvt. Ltd., Noida, India (sonals@cadence.com)

***Abstract*— Defining and verifying power requirements across analog and digital boundaries involves manual task. The power intent defined at concept level must be considered for development at the IP block level, no matter if these are analog or digital blocks. This makes defining and checking of power intent across these analog and digital hierarchies complicated. Also, the power related checks stop at the analog block boundaries. In order to ease the design process, we applied a new methodology for defining and checking of power intent through nested analog and digital hierarchies. The approach depends on the IEEE 1801 format to define the power intent for both analog and digital sub-blocks.**

Keywords—Low-power; analog/mixed-signal design; IEEE 1801; UPF(Unified Power Format); VPM(Virtuoso Power Manager)

I. INTRODUCTION

Today, mixed-signal IPs can be complex subsystems consisting of multiple analog and digital IP blocks with deep hierarchy. These design types can cause various problems in the implementation and verification process. In a top-down design approach, the power requirements are usually defined at conceptual level. These requirements are considered for development at IP block level, regardless of whether the IP blocks are analog or digital blocks.

Complex mixed-signal IPs can have multiple internal power domains powered by internal voltage regulators. The presence of these power domains in the mixed-signal context have been discussed by Mandal et al. in [1]. These domains have added another level of complexity in the implementation. The designer needs to consider requirements that have been defined at conceptual level and implement them in sub-blocks with corresponding power supply architecture.

The general need for low power verification is discussed in [2]. In this paper, the author already points out that the available standard to specify the power intent did not take the analog/mixed-signal design methodology into account. Low power verification is usually being done in the SoC projects. The methodology described in [3] is widely used in digital design flows targeting the SoC level. The authors explain the challenges of the low power verification at SoC level that includes analog IPs. Still the power intent of mixed-signal IPs is not verified using the methodology mentioned in [3] although these IPs can have complex power architectures, too.

In this paper, the focus is on the power supply system of mixed-signal IPs having several internal power domains. The main objectives of this paper are:

- To propose a new methodology and flow for the creation of supply connectivity in the schematic designs
- To describe how the existing low power verification approach can be extended in a way that it works for hierarchical analog IPs or mixed-signal subsystems with the new method

Both methodologies, to create and verify the power intent are based on power formats written in UPF 2.0 (IEEE 1801-2009). The focus of the methodology aims at hierarchical designs consisting of sub-block instances and the supply connections, above the stop level within the design hierarchy. This stop level is defined by the cell interface definition, written as Liberty model.

II. BASIC ELEMENTS AND TERMINOLOGY OF IEEE 1801 FORMAT

The power supply system or power architecture can be expressed by using the IEEE 1801 format as a modeling language. While the behavior of a circuit is modeled as schematic diagrams or RTL code, the corresponding power intent is written in IEEE 1801 [4]. The IEEE 1801 format brings a unified way to describe the structure of the power supply system as well as low power requirements in the design process of IPs or complete SoCs [5]. Therefore, this format is also known as UPF. It is readable by many EDA tools. This makes it possible to pass the power specification through the tool chain.

Most relevant specifications and terms in IEEE 1801 are:

- Power Domain (PD): a power domain groups the design elements with the same power supply requirements like different standard cell supply voltages and shut-off conditions. A power domain belongs to a part of the logic hierarchy, called scope.
- Supply ports and nets: representation of the actual power supply lines and pins. The supply nets are grouped in supply sets and get assigned to a power domain.
- Supply set: pairs of supply nets that belong together
- Port attribute: defines to which supply a port is connected to
- Isolation rule: describes how a signal has to react when the corresponding block is powered off. The rule requests isolation cells to be implemented at the power domain boundaries.
- Level shifter rule: describes a transition of a signal voltage when the driver or receiver cells run at different supply voltages. The rule requests level shifter cells to be implemented at the power domain boundaries.
- Power switch rule: describes how the internal switchable supply is generated from the input power supply based on the enable condition.
- Power state, power state table (PST): valid combination of voltages. Power states are grouped together in a power state table.

The details for the above, are captured in 1801 Export in Figure 7.

III. MIXED-SIGNAL BLOCK DEVELOPMENT WITH POWER INTENT

A. Motivation for Importing the Power Intent by Using IEEE 1801

When working with a top-down approach, IP blocks are developed based on the specification. The power supply system may be specified as a block diagram whereas the driver voltages of ports are often captured in spread sheets. To implement the power supply system for a mixed-signal block, the designer takes the appropriate supply definitions from the diagram and spread sheets and creates the supply domains and connections in the schematic. This is a manual task and can take a couple of iterations and reviews until all errors in the supply connectivity are fixed. In addition, the more complex the design is, the more challenging it is to propagate power connectivity in an accurate and optimized way.

In order to make the design entry process more reliable, we propose a new method for the creation of supply connectivity in the schematic designs. This may speed up the design entry as the power connectivity in the schematic is being generated according to the power specification.

B. Methodology of Importing Power Intent during Design Entry

Formats for expressing power intent have been available for some time now. However, there seems to be a lack of mixed-signal specific methodologies for the use of those formats.

The method makes IEEE 1801 power requirements applicable in the full-custom design process. It supports:

- Module-based development of full-custom IP blocks.
- Complex hard IPs like PLLs or LDOs with their own UPF design models
- Hierarchical design approach
- Existing full-custom design environment

The UPF import starts from a usual hierarchical schematic without supply connectivity, where the leaf cells have the power definition. An example is shown in Figure 1.

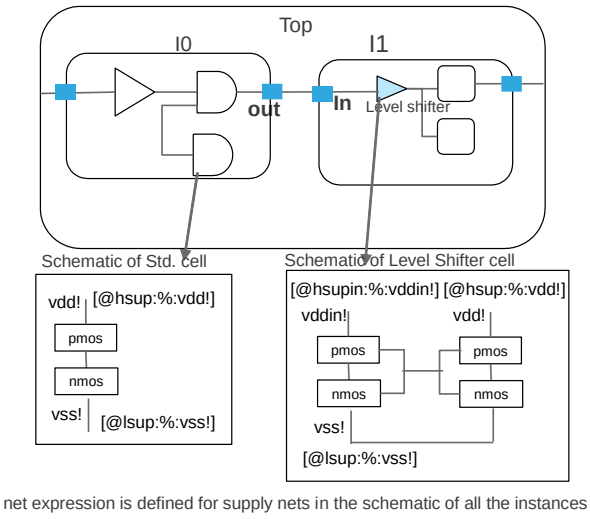


Figure 1: Schematic Design without supply connectivity

The power requirements have to be applied on the schematic. As the analog/mixed-signal design tools did not offer features for importing UPF, we developed the Virtuoso Power Manager (VPM). As shown in Figure 2, it provides an interface to import power requirements specified in IEEE 1801 and apply them on a hierarchical schematic.

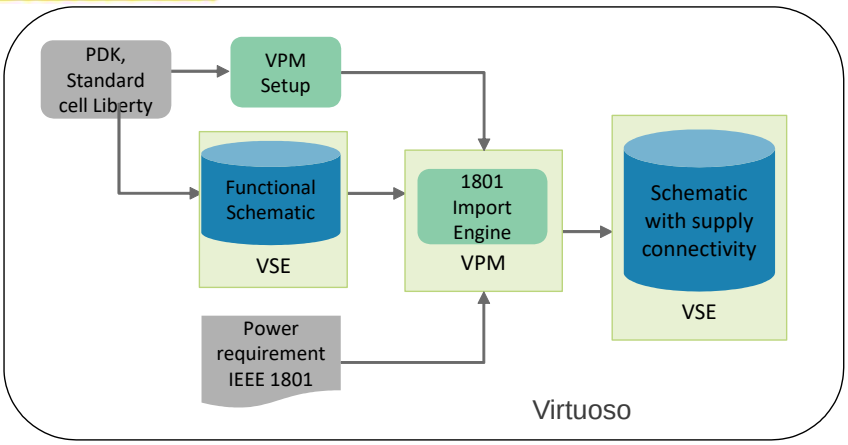


Figure 2: Creating power supply connections by importing IEEE 1801

The import interface must be configured using a separate setup file. It generates connectivity for the instances according to UPF definitions by using "inherited connections". This is a connectivity model which requires the property (aka net-expressions in Virtuoso) on the net, to be specified within leaf cells and/or blocks, and up in the hierarchy it can be connected to different value (aka netSet properties in Virtuoso) [7]. It is generally used for supply connectivity to avoid creating extra terminals on the symbol, thus reduced physical connections. Figure 3 illustrates the supply connectivity after 1801 import, using inherited connections. The instances in the schematic are connected to the power supplies according to the definitions in the UPF.

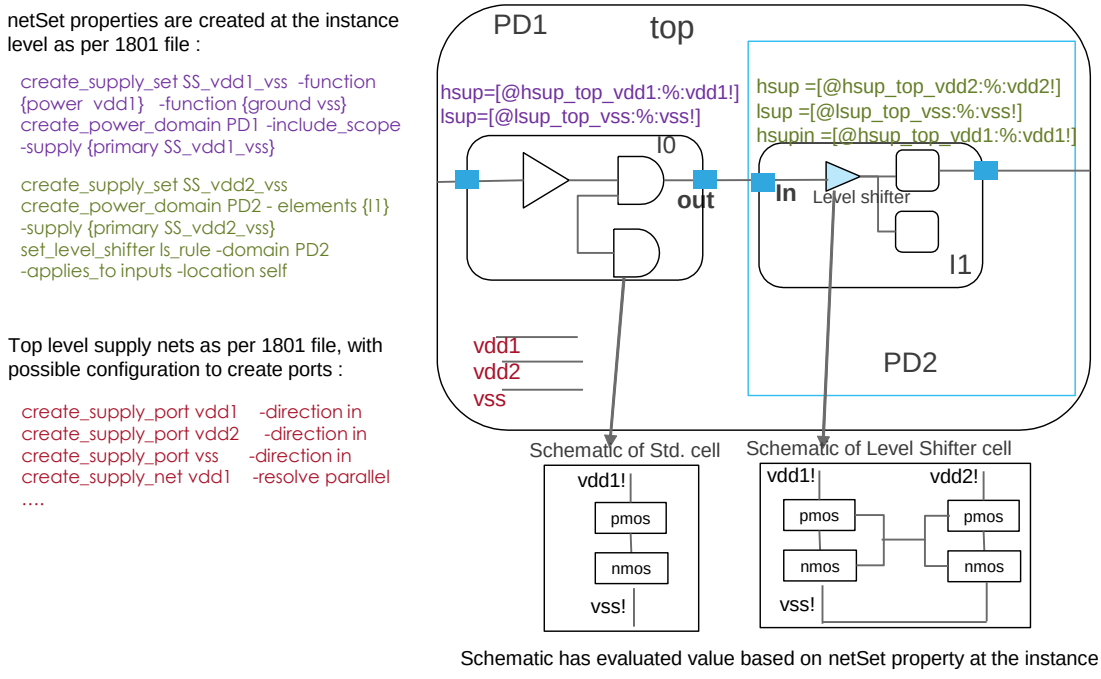


Figure 3: Supply connections in the schematic after IEEE 1801 Import

The approach worked successfully for our designs created using different methodologies, including the ones that are created using the top-down design methodology. The VPM Import interface creates optimal number of netSet properties that is very difficult to be implemented manually given the complexities of our designs.

C. Verifying power intent with design connectivity using IEEE 1801 Export

Once the schematic is finally implemented and available it needs to be checked for issues that can occur when a design has multiple power domains, like missing level shifters. Static check of the complete design against the power intent is essential to detect errors at power domain boundaries or in the power connectivity and avoids iterations in the design process. These checks are used in digital designs for many years. So far checks were also

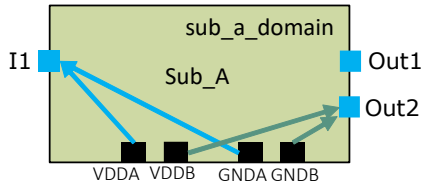


Figure 4: Example of block interface: UPF interface model with supply relations

performed on our custom analog, mixed-signal designs as part of the digital low-power verification, after the IP blocks were integrated. However, the checks only worked with limited UPF interface models. An example of block

```
create_power_domain sub_a_domain
create_supply_port VDDA -direction in
create_supply_port VDDB -direction in
create_supply_port GNDA -direction in
create_supply_port GNDB -direction in
create_supply_net VDDA -domain sub_a_domain
create_supply_net VDDB -domain sub_a_domain
create_supply_net GNDA -domain sub_a_domain
create_supply_net GNDB -domain sub_a_domain
connect_supply_net VDDA -ports VDDA
connect_supply_net VDDB -ports VDDB
connect_supply_net GNDA -ports GNDA
connect_supply_net GNDB -ports GNDB
set_port_attributes -ports {I1} \
   -related_ground_port "GNDA" -related_power_port "VDDA"
set_port_attributes -ports {Out1} \
   -related_ground_port "GNDA" -related_power_port "VDDA"
set_port_attributes -ports {Out2} \
    -related_ground_port "GNDB" -related_power_port "VDDB"
```

Figure 5: Example of UPF interface model

interface is shown in Figure 4. The IP block has two supplies, the input and output pins are related to these supplies. The corresponding UPF interface model of the block is shown in Figure 5. It contains the domain definition, supply ports, nets, and supply relations. The internal details of the block, however, are not considered.

To extend the mixed-signal verification methods, we propose to use an IEEE 1801 Design model which covers more IP relevant details of the power architecture like internal level shifters or power states. A comprehensive discussion of this modeling approach can be found in [6]. The goal is to apply the checks to mixed-signal IP blocks. The method is illustrated in Figure 6. The approach is based on VPM and extracts power intent out of the schematic designs and then, export it in IEEE 1801 (UPF 2.0) format. The UPF models are then checked before integration at SoC level. In contrast to the approach described above, the VPM extractor is able to cope with various power saving techniques and is able to produce IEEE 1801 model that fully describes the block interface as well as internal power structures. The exported design model includes all the specifications that are captured in section II.

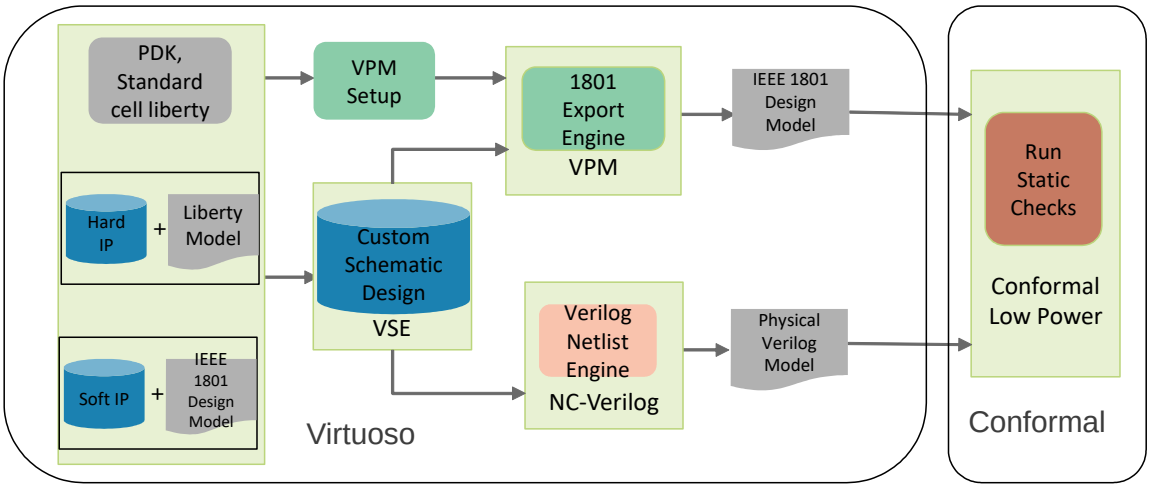
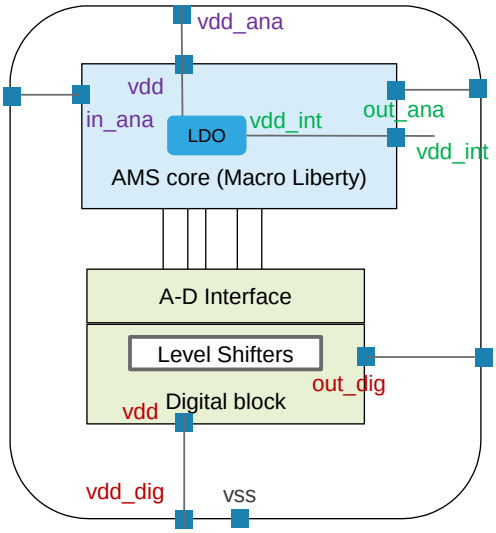


Figure 6: Verifying the power intent by exporting IEEE 1801

Using this detailed IEEE 1801 design model from a schematic design, it becomes possible to do a comprehensive low power static verification.

We consider the new method to be successful, if not only the IP interface is checked but also the internal structure and power domain crossings. The example below illustrates how this requirement is met. The IP block has an internal interface at which level shifters transform the signals between the analog and digital sub block. There is internal power generated in AMS block and drives the boundary port, which is also captured in 1801 file with the required commands. The corresponding UPF design model extracted from the schematic is shown in Figure 7.



Power state tables :

```
create_pst   top_pst -supplies [vdd_ana  vdd_dig vss
ams/vdd_int ]
add_pst_state state_1 -pst top_pst -state { V110 V130  OFF
V110 }
#PST are gen. for other port states as well #
```

Primary power domain of AMS core :

```
create_supply_net vdd_ana
create_supply_port vdd_ana –direction inout
connect_supply_net vdd_ana –ports vdd_ana
create_supply_set SS_analog –function {power vdd_ana}
-function {ground vss}
 create_power_domain pd_ana –elements {ams} –supply
{primary SS_analog}
set_port_attributes -ports in_ana –receiver_supply SS_ana
add_port_state vdd_ana  -state { V110 1.1 }  -state { OFF off }
```

Internal power of AMS core :

```
create_supply_net vdd_int
connect_Supply_net vdd_int –ports ams/vdd_int
create_supply_set SS_int –function {power vdd_int}
-function {ground vss}
set_port_attributes -ports out_ana –driver_supply SS_int
add_port_state ams/vdd_int  -state { V110 1.1 }  -state { OFF
off }
```

Primary power domain of Digital block :

```
……
create_power_domain pd_dig –include_scope –supply
{primary SS_digital}
set_port_attributes -ports out_dig –driver_supply SS_digital
set_level_shifter pd_dig_ls –domain pd_dig –applies_to inputs -
input_supply_set SS_ana -output_supply_set SS_dig –location
self   –rule low_to_high
add_port_state vdd_dig   -state { V130 1.3 }  -state { OFF off }
add_port_state vss   -state { OFF 0 }
```

Figure 7: Mixed-signal signal sub-block with internal level shifter, control logic, and UPF 2.0 design model. Separate power domains and relations are shown in different colors.

The block “AMS core” in Figure 7 forms a power domain “pd_ana” which takes the supply vdd_ana as primary input. The voltage regulator (LDO) outputs the internal supply “vdd_int”. The digital block belongs to the power domain “pd_dig” and is powered by the vdd_dig supply. The correspondig UPF code is shown in different colors. In case one of the interface signals running between analog and digital part has no level shifter (not shown in the

> “Error: (1801_LSH_NO_STRATEGY_LH_PATH_NOLSH) Level shifter strategy is not specified for low-to-high power or high-to-low ground state crossing, on a path that does not contain any level shifter cell.”

picture), the level shifter statement is not generated in UPF file, though power state tables (PST) are created in 1801 file and Verilog netlist will have the design connectivity. This issue is then be flagged as design error when checking the design by Conformal Low Power.

IV. Conclusion

We have applied two design methodologies for IEEE 1801 (power intent definition) 1) power supply implementation and 2) static low power checking on mixed-signal IP blocks. During the IP authoring, the power requirements are specified using the IEEE 1801 format. The VPM Import IEEE 1801 capability automates the creation of power supply connectivity in a design and thereby, increasing designers’ productivity. The VPM Export 1801 capability makes it possible to extract power intent that is implemented in our schematic designs and export it in the IEEE 1801 format. The exported power intent captures all the complex cases of internal supplies, special cells and hierarchical supply connectivity, and thus enables a thorough low power checking using Conformal Low Power, which was not possible with UPF interface models that have been used for IP blocks before.

Nevertheless the UPF format has certain limitations when it comes to mixed-signal design. One example is the tight relation of a power domain and power management cells, such as level shifters. The UPF standard defines that level shifters have to be inserted at the boundary of a power domain. For a mixed-signal block it is in the hands of the designer to set up the domain in a way that it matches the requirements coming from concept engineering but also fits to the position of level shifters in the design hierarchy. Therefore, this rule can lead to artificial domains or additional design hierarchies just in order to make the design compliant to the standard. Another example are analog elements like transmission gates that do not have any power supply. That makes it difficult to model them properly as leaf cell in the low power verification.

Acknowledgment

We would like to thank Steffen Rost, Jürgen Karmann and Gernot Zessar for bringing in much technical expertise and Ibrahim Khan, Werner Grollitsch, Gregor Kowalczyk and Thomas Cemernek for their active and valuable technical work and preparation of results. We also thank Madhur Sharma and Steffen Lorenz for their valuable support during the project development.

References

[1] S. Mandal , A. Bruto Da Costa, A. Hazra, P. Dasgupta, B. Naware, R. M. Chunduri, S, Basu, “Formal Verification of Power Management Logic with Mixed-Signal Domains”, in 30th International Conference on VLSI Design and 16th International Conference on Embedded Systems (VLSID), 2017.

[2] R. Lipon, “Rethinking SoC Verification”, white paper, Synopsys Inc, 2014

[3] L. Shaotao, D. Majhi, “UPF-Based Static Low-Power Verification in Complex Power Structure SoC Design Using VCLP”, in SNUG proceedings, 2015

[4] G. Delp, E. Marschner, K. Bakalar, “Understanding the Low Power Abstraction”, in DVCon proceedings, 2010

[5] IEEE Std 1801™-2009 for Design and Verification of Low Power Integrated Circuits. IEEE Computer Society, 2009.

[6] A. Srivastava, R. Mukherjee, E. Marschner, C. Seeley, S. Dobre, " Low Power SoC Verification: IP Reuse and Hierarchical Composition using UPF", in DVCon proceedings, 2012

[7] Virtuoso Schematic Editor L User Guide, chapter "Connectivity and Naming Conventions" [Online], 2018, Link (Link requires to enter the registered Login ID)