HYBRID EMULATION: ACCELERATING SOFTWARE DRIVEN VERIFICATION AND DEBUG

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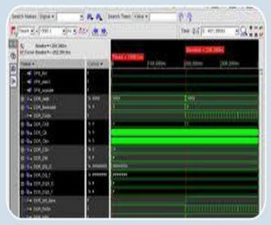
MOTIVATION TOWARDS HYBRID PLATFORM

Debugging HW/SW issues using real OS Apps on FPGA is challenging due to low design visibility.

TRYM-3135 took more than 3 months to resolve.



Complex real OS App issues could take weeks to generate the stimulus and reproduce at unit level simulation platforms

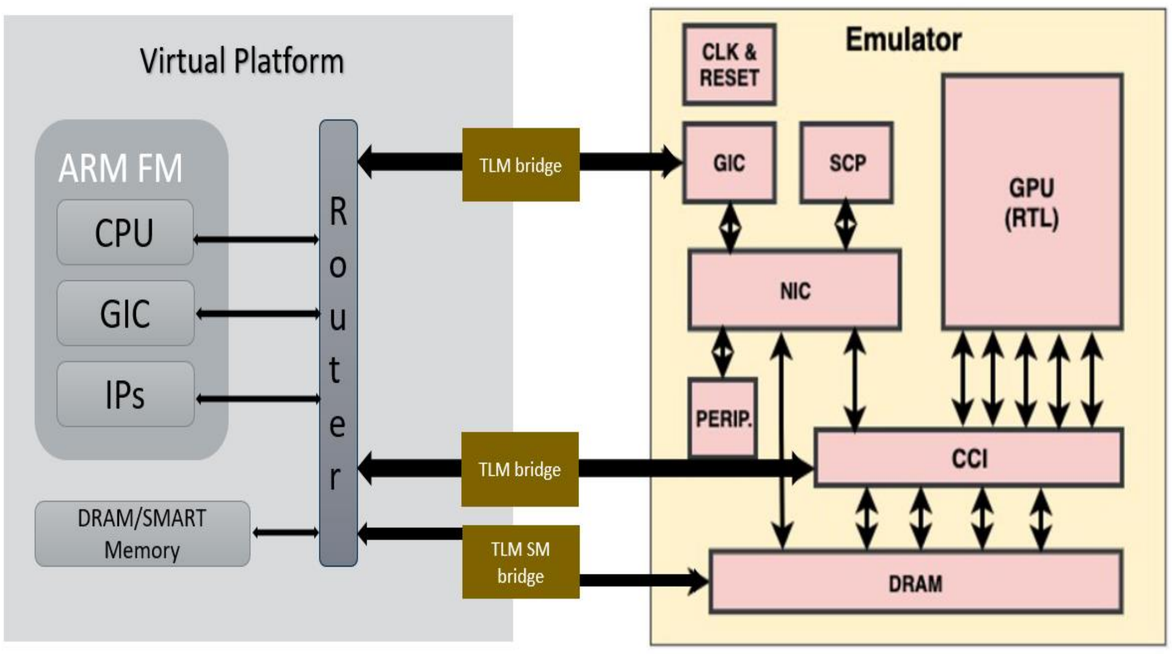
Mali® GPU HW and SW live debug is challenging in present platform setup

Issues reported in different verification platforms/tools typically are not cross reproducible

PROPOSED METHODOLOGY & ADVANTAGES

- A high-performance transaction-level model of the CPU subsystem running on Virtual Platform with RTL for the rest of the SoC running on the emulator
- Enables the software to execute at virtual platform speeds
- Higher performance for software-driven hardware verification even when RTL for critical blocks isn't available
- Early architecture validation and software development
- Easier platform upgradability and Much better design debug visibility
- Supports different debug methods over FPGA platform such as waveform, Smart memory debug tools, memory dump, tarmac, capture replay, monitors etc

HYBRID PLATFORM INTEGRATION

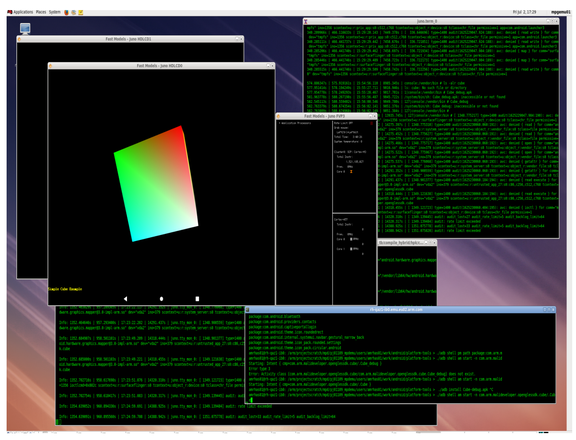


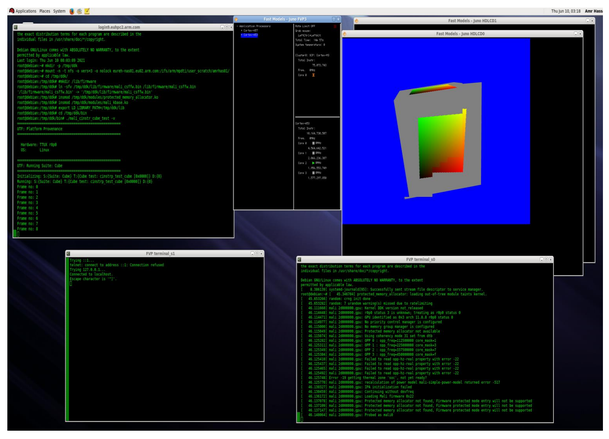
PLATFORM INTEGRATION STAGES

- Replaced RTL CPU and GIC with Arm Cortex A55 and GIC 600 fast model on the virtual platform
- Converted RTL memory to smart memory to enable the CPU to access it via backdoor
- Smart memory acts as shared memory which is visible to both virtual and RTL platforms
- Integrated TLM bridges to facilitate the communication between virtual and RTL platform
- CPU access the memory within the virtual platform and other peripherals in the RTL through TLM bridge connected to the CCI550
- GPU access the memory through CCI550 bridge

RUNTIME PERFORMANCE AND RESULTS

Test	Runtime
Linux Boot	62 sec
Android 10	2640 sec
Debian Buster 11	185 sec





CONCLUSION AND NEXT STEPS

- Helped reproducing the hardware and software issues captured in FPGA platform which enables much better turnaround time for the debug and corresponding patch validation
- Caters an effective co-ownership of FPGA based challenges in Software development, therefore it is certainly not a replacement of our existing FPGA platform
- Observed significant gain with Hybrid usage in Emulator which led us to explore and deploy it on bigger ecosystems of Arm

REFERENCES

Developer. Arm tools-and-software/development-boards/Juno-development-board