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High-Speed Interface IP Validation based on Virtual Emulation Platform

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Agenda

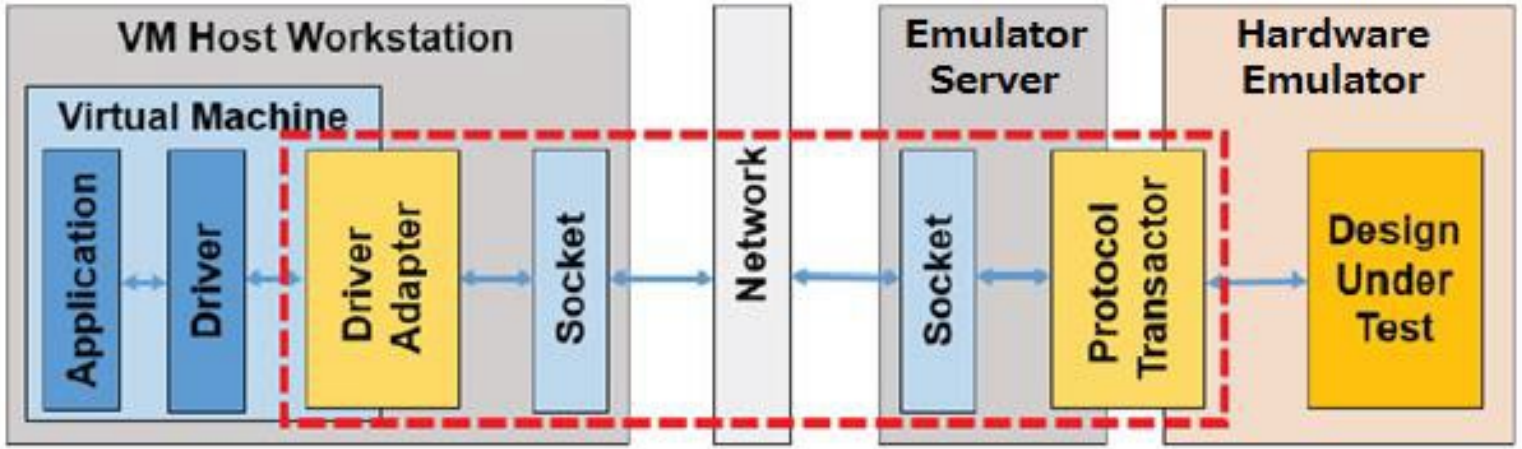
- Introduction
- The concept of Virtual Emulation
- Existing HSI IP validation flow
- Proposed HSI IP validation flow
- Method to accelerate pre-silicon validation
- How to debug in Virtual Emulation Platform
- Experiment results
- Conclusion

Introduction

- Modern SoC trend
  - Current electronic devices require large data storage to store numerous data and perform necessary calculations quickly
  - This requirement of high-speeds leads to wide usage of High-Speed Interface (HSI) IPs in various system-on-chip (SoC) products

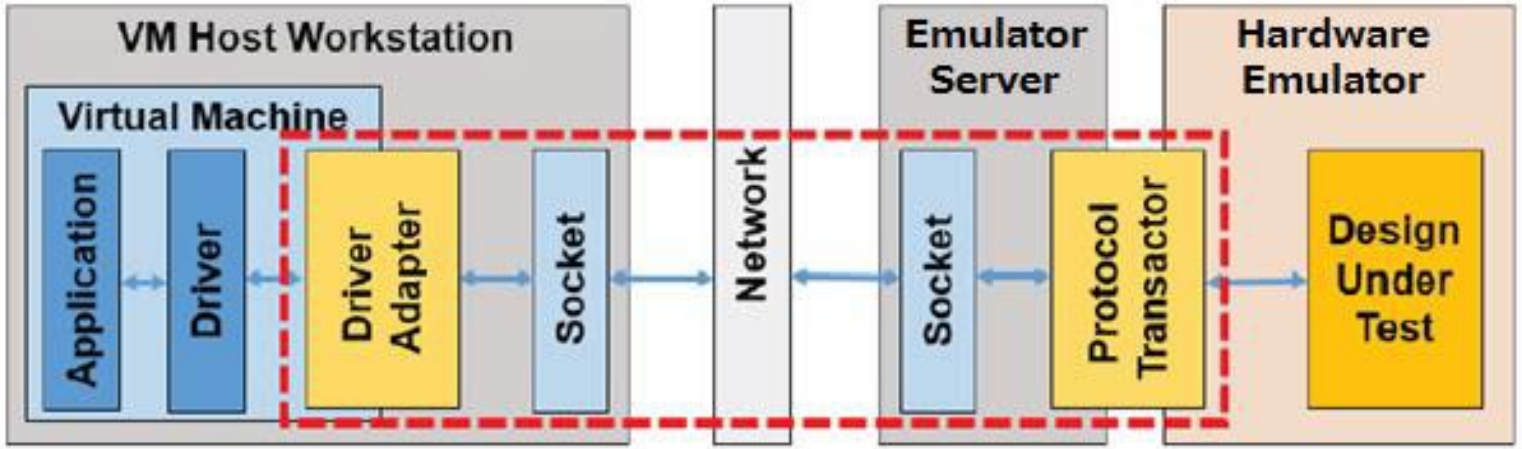
The concept of Virtual Emulation (1)

- What's the Virtual Emulation?
  - Virtual emulation technology needs a "**software adapter**" that enables user applications and OS drivers to establish a virtual protocol connection to the hardware emulator



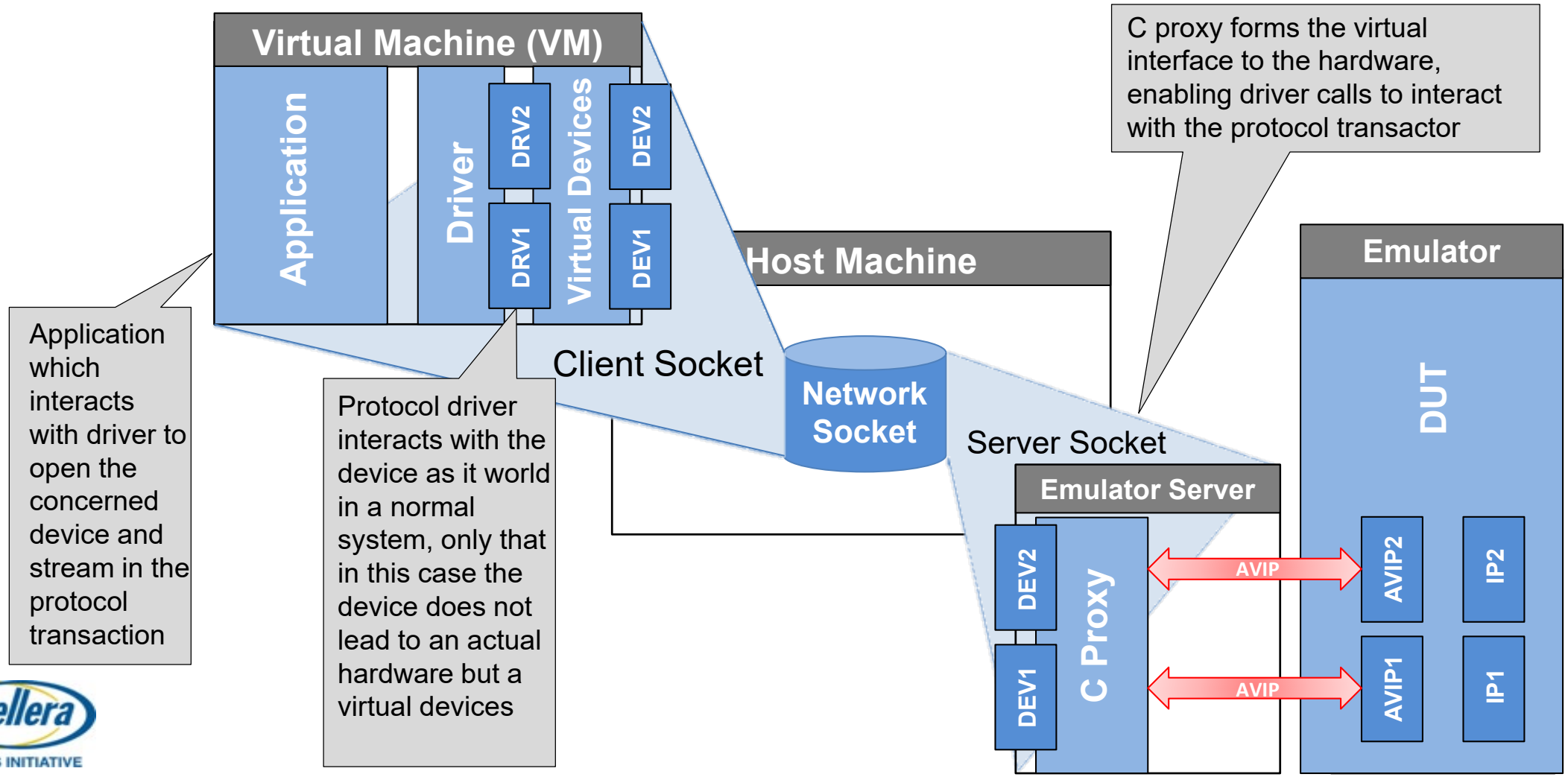
The concept of Virtual Emulation (2)

- Benefits
  - Flexibility to run jobs without physical constraints
  - Statically controlled runs allowing freedom to debug without timeouts
  - Validate system level S/W interoperability early in development cycle



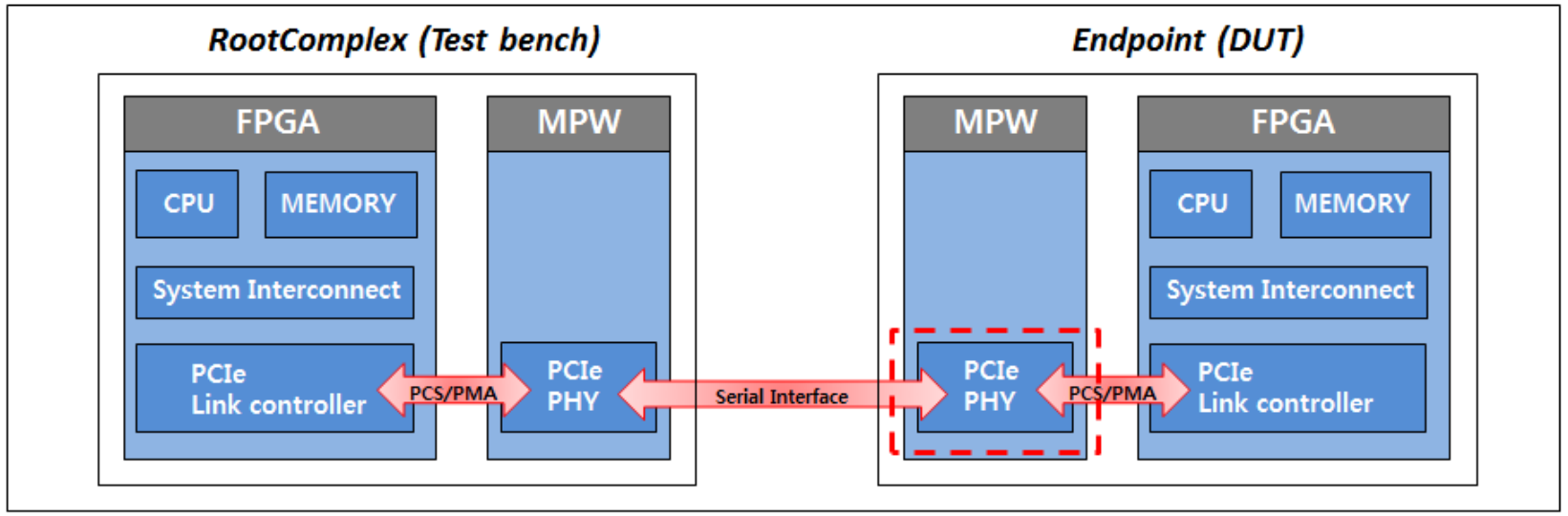
The concept of Virtual Emulation

- Architecture of Virtual Emulation Platform



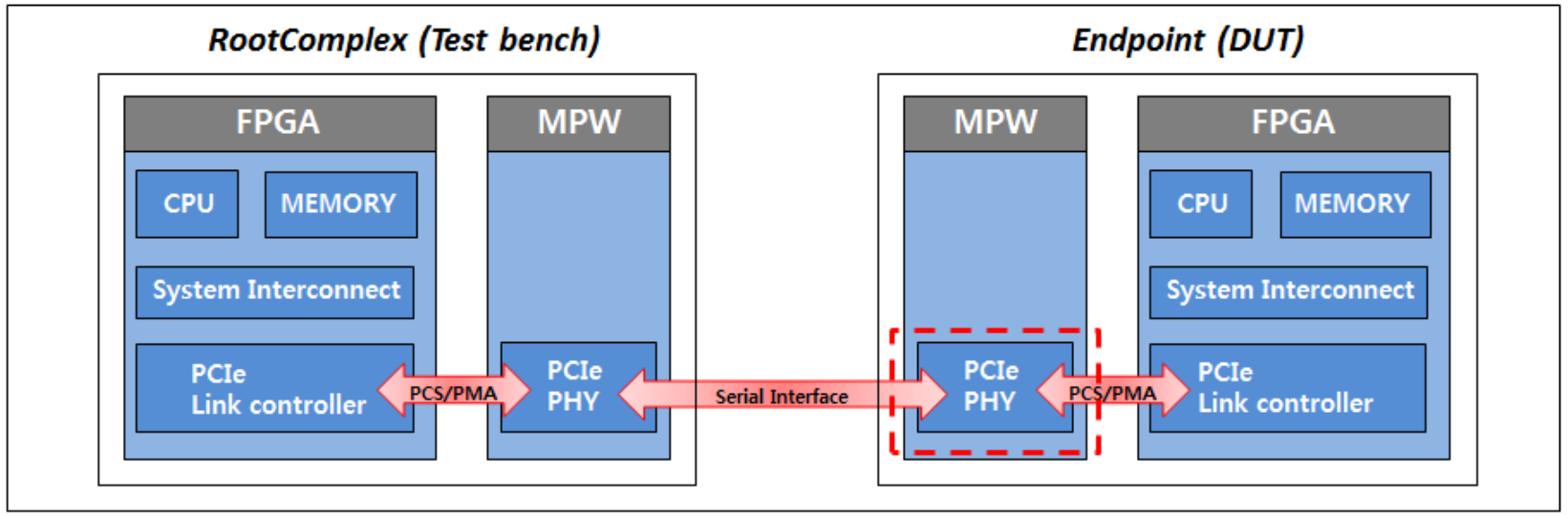
Existing HSI IP validation flow (1)

- HSI IP validation based on FPGA with MPW (Multi Project Wafer)
  - DUT: mini-SoC including PCIe Endpoint
  - Test bench: mini-SoC including PCIe Root Complex



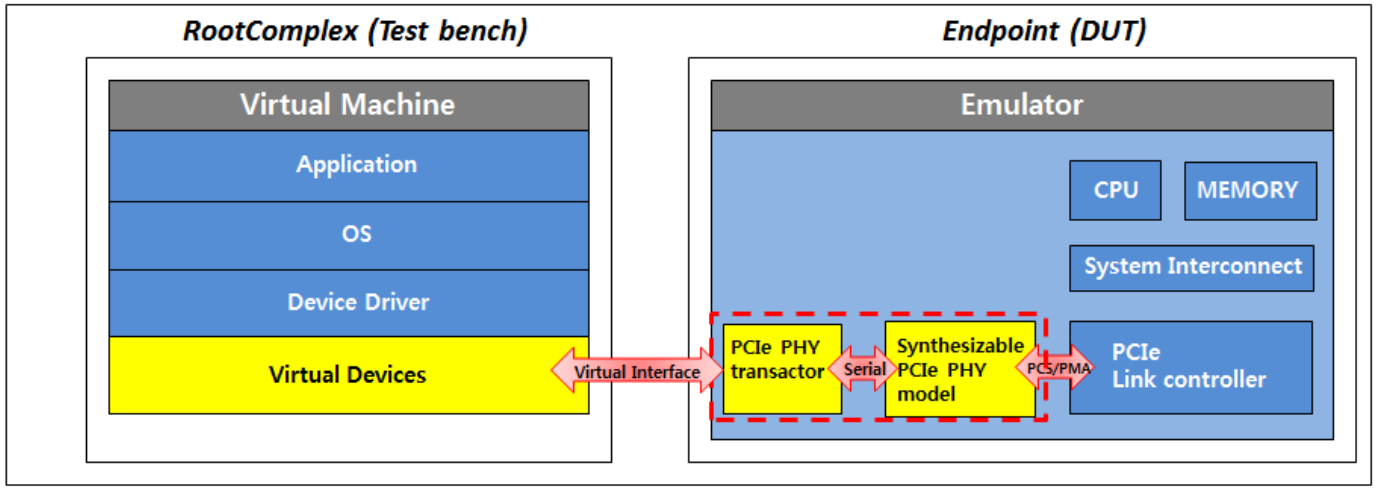
Existing HSI IP validation flow (2)

- Problems
  - Long TAT (Turn-Around-Time) because of MPW test chips
  - High effort to implement the DUT on FPGA



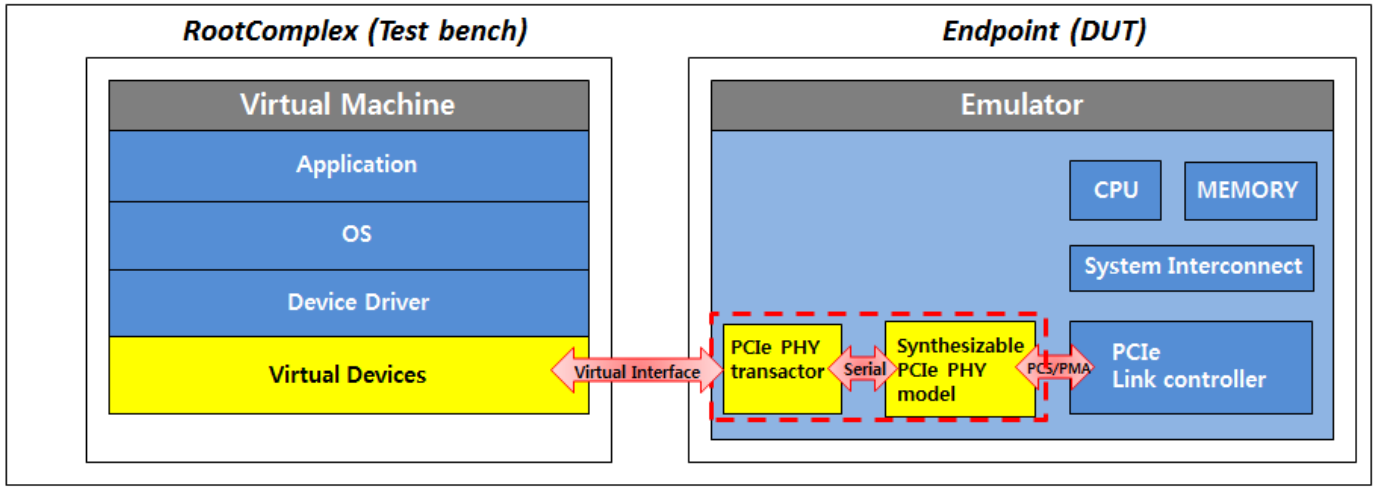
Proposed HSI IP validation flow (1)

- HSI IP validation based on virtual emulation platform
  - DUT: mini-SoC including PCIe Endpoint with PCIe transactor
  - Test bench: virtual devices with device driver on virtual machine



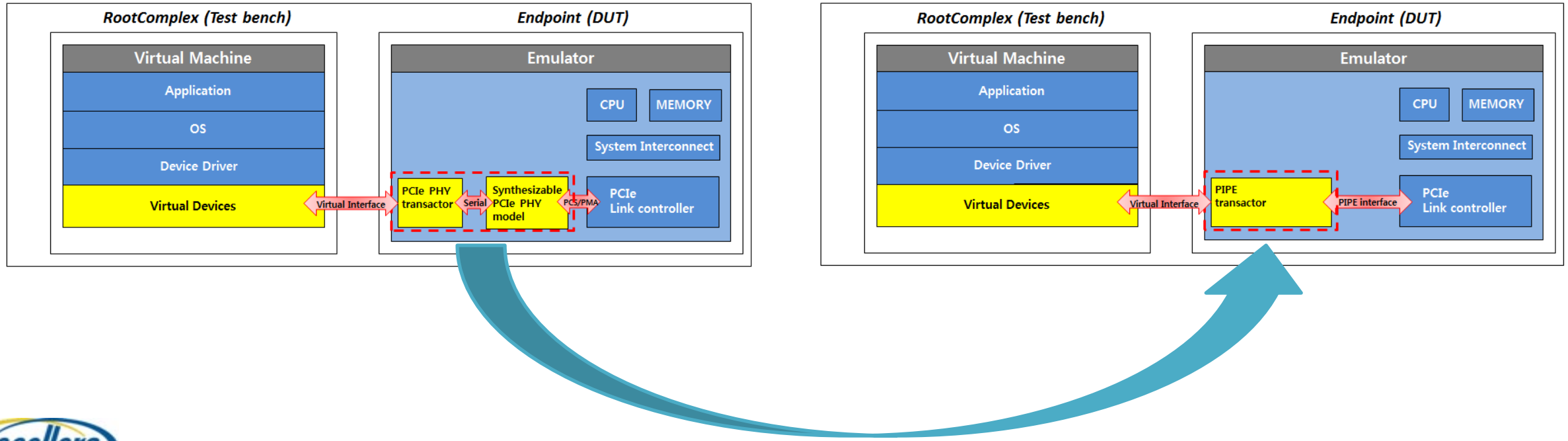
Proposed HSI IP validation flow (2)

- Benefits
  - Not require the MPW test chip and available at a pre-silicon stage
  - Reinforce the functional verification by performing OS-level scenarios



Method to accelerate pre-silicon validation (1)

- Using the PIPE (PHY interface for the PCI Express) interface
  - Replace PHY layer with PIPE transactor

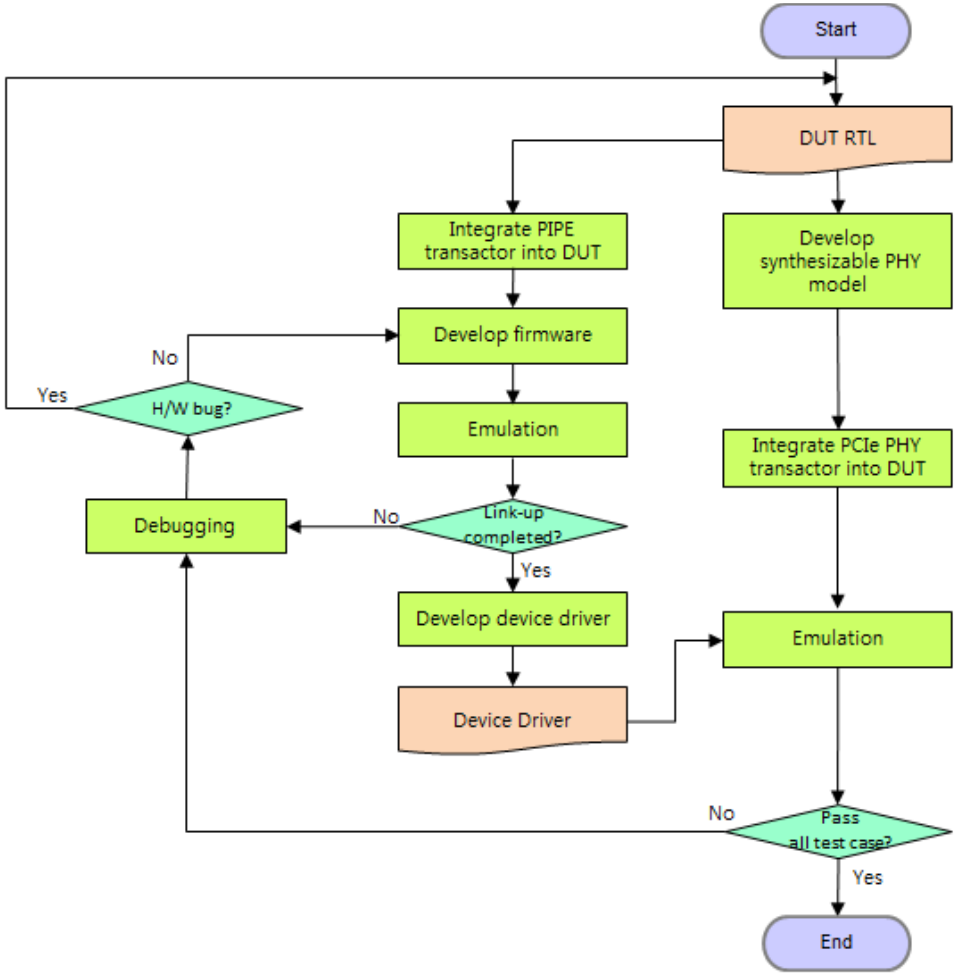


Method to accelerate pre-silicon validation (2)

Scenario / Interface	Gen3 Link-up		Loading VM and Transaction (4096 burst)	
	Simulation Time (ms)	Wall clock time (sec)	Simulation Time (ms)	Wall clock time (sec)
Serial Interface	62.7	3149.76	100	5006.75
PIPE Interface	2 x31.35	19.38 x162.5	18 x5.56	379.28 x13.2

Method to accelerate pre-silicon validation (3)

- Mixed interface flow for reduce development TAT (Turn-Around-Time)

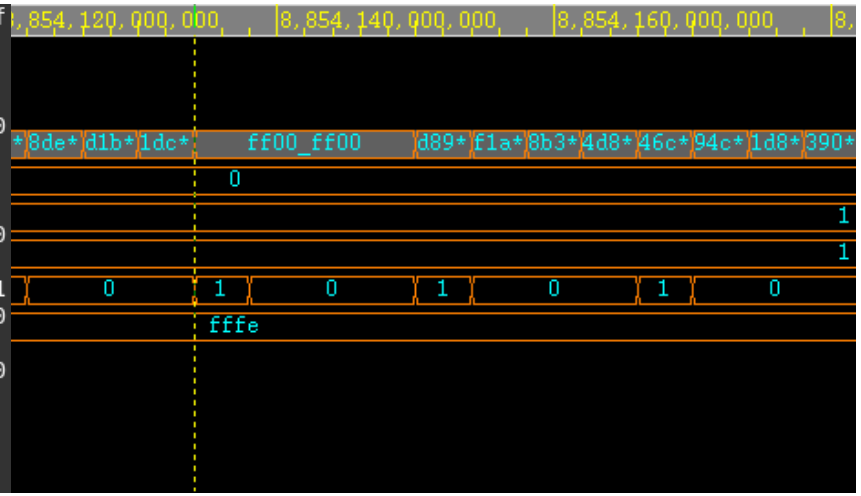


How to debug in Virtual Emulation Platform (1)

- H/W debugging method
  - Waveform dump with fully static environment
  - Transaction monitoring

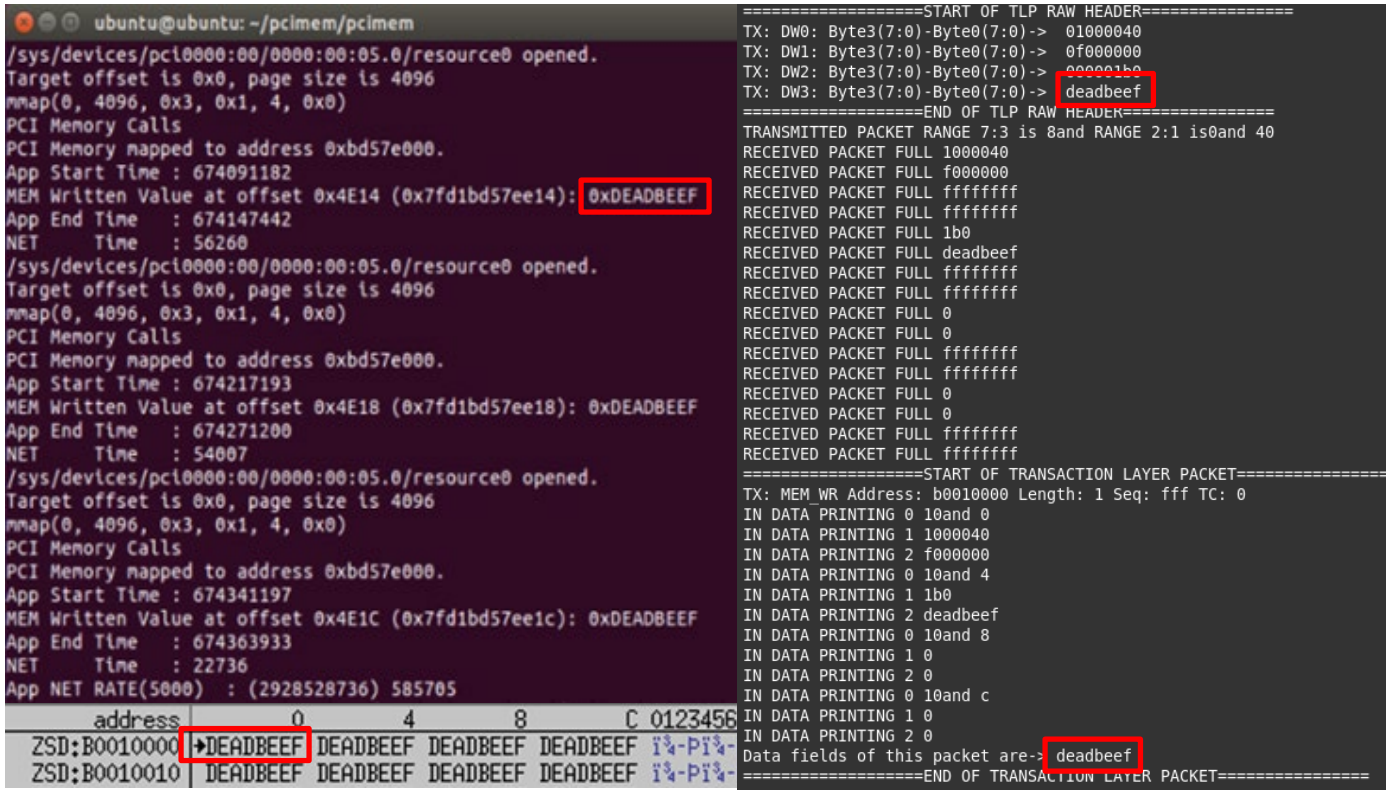
```
==================START OF TRANSACTION LAYER PACKET================
TX: CFG_WR0 Address: 30 Length: 1 Seq: fff Data: fffff800 TAG: 4
==================END OF TRANSACTION LAYER PACKET================
==================START OF TRANSACTION LAYER PACKET================
TX: CFG_RD0 Address: 30 Length: 1 Seq: fff TAG: 5
==================END OF TRANSACTION LAYER PACKET================
==================START OF TRANSACTION LAYER PACKET================
RX: CMPL_WITHOUT_DATA Requestor ID: 0 Completor ID: 0 Status : 0 Length: 0 Seq:

==================END OF TRANSACTION LAYER PACKET================
==================START OF TRANSACTION LAYER PACKET================
RX: CMPL_WITH_DATA Requestor ID: 0Completor ID: 0 Status : 0 Length: 1 Seq: fff

Data fields of this packet are-> ffff0000
==================END OF TRANSACTION LAYER PACKET================
DEBUG_REMOVE Assigned local_id = 6
DEBUG_REMOVE Assigned local_id = 7
DEBUG_REMOVE Assigned local_id = 8
DEBUG_REMOVE Assigned local_id = 9
==================START OF TRANSACTION LAYER PACKET================
TX: CFG_WR0 Address: 30 Length: 1 Seq: fff Data: ffff0001 TAG: 6
==================END OF TRANSACTION LAYER PACKET================
==================START OF TRANSACTION LAYER PACKET================
TX: CFG_WR0 Address: 10 Length: 1 Seq: fff Data: fe800000 TAG: 7
==================END OF TRANSACTION LAYER PACKET================
```

```
60,WRITE_SLV_CFG_0,PCIE,0,0,56,20,f,1,416.882848612,ffffffff
61,READ_SLV_CFG_0,PCIE,0,0,52,20,f,1,416.882909284,
62,WRITE_SLV_CFG_0,PCIE,0,0,56,20,f,1,416.885443729,0
63,READ_SLV_CFG_0,PCIE,0,0,52,24,f,1,416.885505469,
64,WRITE_SLV_CFG_0,PCIE,0,0,56,24,f,1,416.887329131,ff00ff00
65,READ_SLV_CFG_0,PCIE,0,0,52,24,f,1,416.887391100,
66,WRITE_SLV_CFG_0,PCIE,0,0,56,24,f,1,416.891628122,0
67,READ_SLV_CFG_0,PCIE,0,0,52,30,f,1,416.891695020,
68,WRITE_SLV_CFG_0,PCIE,0,0,56,30,f,1,416.893531233,fffff800
69,READ_SLV_CFG_0,PCIE,0,0,52,30,f,1,416.893596693,
70,WRITE_SLV_CFG_0,PCIE,0,0,56,30,f,1,416.896182963,ffff0001
71,WRITE_SLV_CFG_0,PCIE,0,0,56,10,f,1,416.896273871,fe800000
72,WRITE_SLV_CFG_0,PCIE,0,0,56,14,f,1,416.896325877,0
73,WRITE_SLV_CFG_0,PCIE,0,0,56,30,f,1,416.896372162,fe970000
74,READ_SLV_CFG_0,PCIE,0,0,52,3c,2,1,416.998889817,
75,WRITE_SLV_CFG_0,PCIE,0,0,56,3c,1,1,417.000649482,a
76,READ_SLV_CFG_0,PCIE,0,0,52,4,3,1,417.000713440,
77,WRITE_SLV_CFG_0,PCIE,0,0,56,4,3,1,417.003050944,147
```



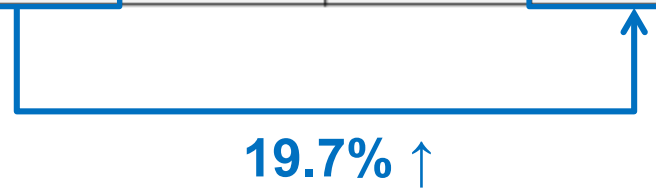
How to debug in Virtual Emulation Platform (2)

- S/W debugging method
  - S/W debugger
  - Transaction monitoring

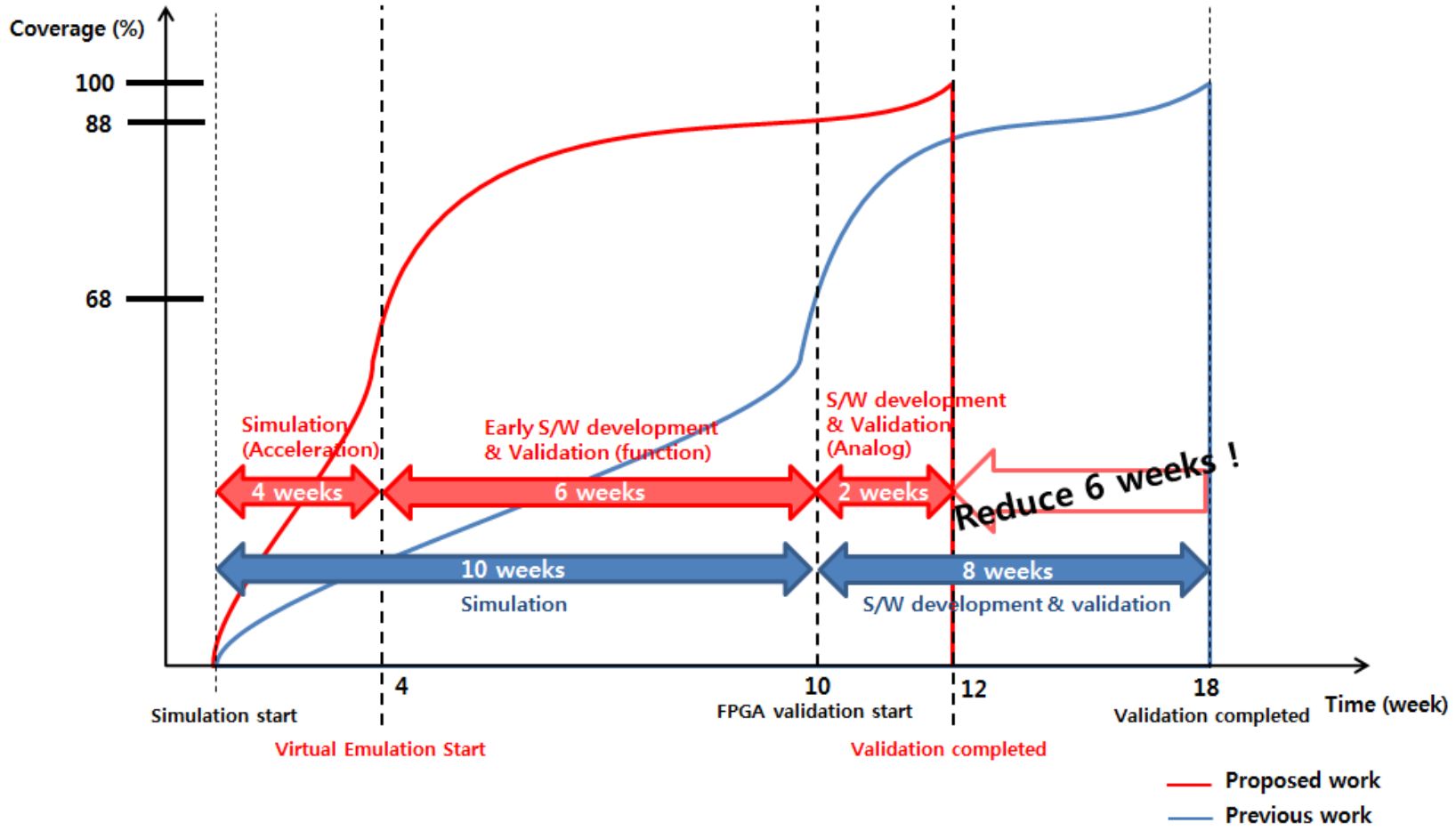


Experiment results (1)

Feature	Previous Work			Proposed Work		
	All	Completed	Coverage	All	Completed	Coverage
Normal operation (LTSSM, Speed Change, Interrupt, Bifurcation)	143	105	73.4%	143	120	83.9%
Transaction (Inbound, outbound, configuration, DMA)	38	23	60.5%	38	38	100%
Power Management (Aging, ASPM, PM)	33	11	33.3%	33	28	90.3%
Compliance	40	34	85%	40	37	92.5%
Total	254	173	68.1%	254	223	87.8%



Experiment results (2)



Conclusions

- The Virtual Emulation Platform (VEP) is proposed for the validation of High-Speed Interface IPs
  - Enable us to develop target S/W codes and take OS-level tests with the full speed of HSI IP at a pre-silicon stage
  - Reduce the TAT of a HSI IP validation
  - Have unique benefits such as flexibility, debug capability with static environment and accessibility at early stage

- For a industrial testcase, the proposed VEP able to achieve 19.7% coverage increase and 33.3% TAT (Turn-Around-Time) reduction

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Thank You

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