

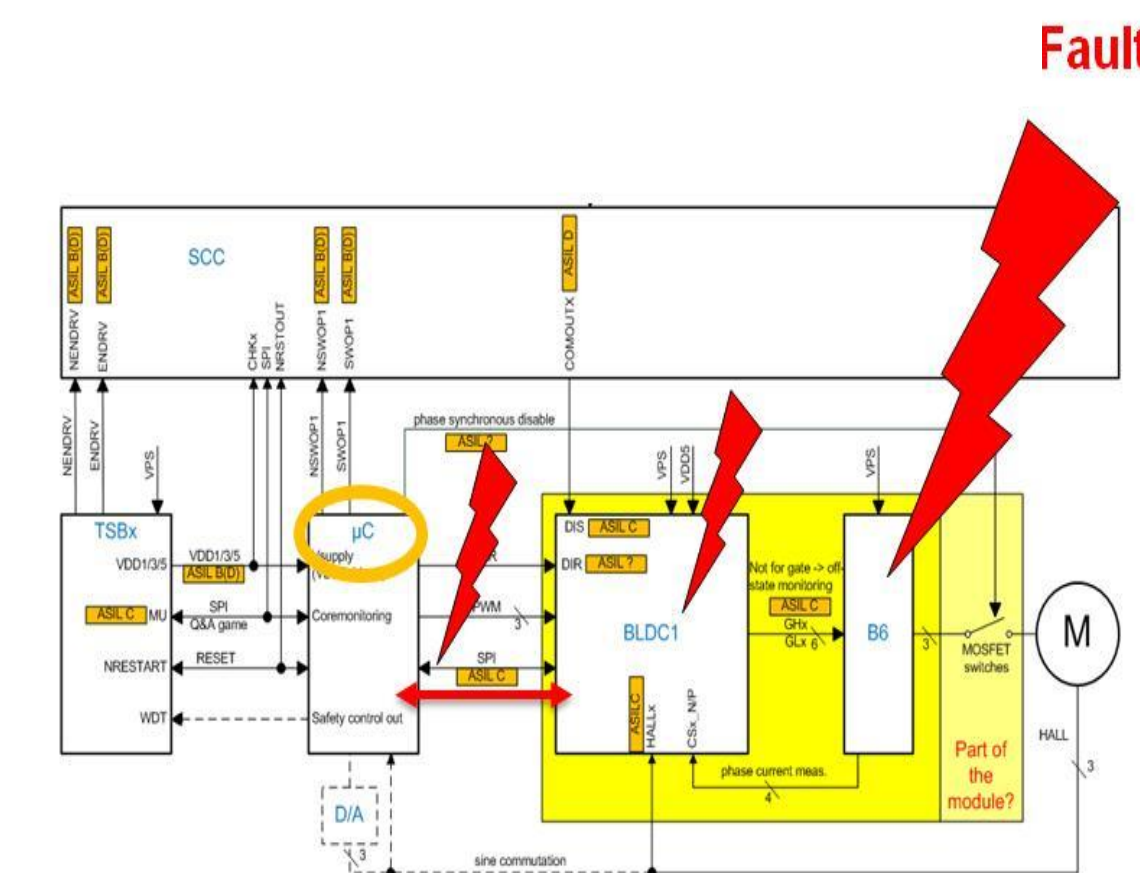
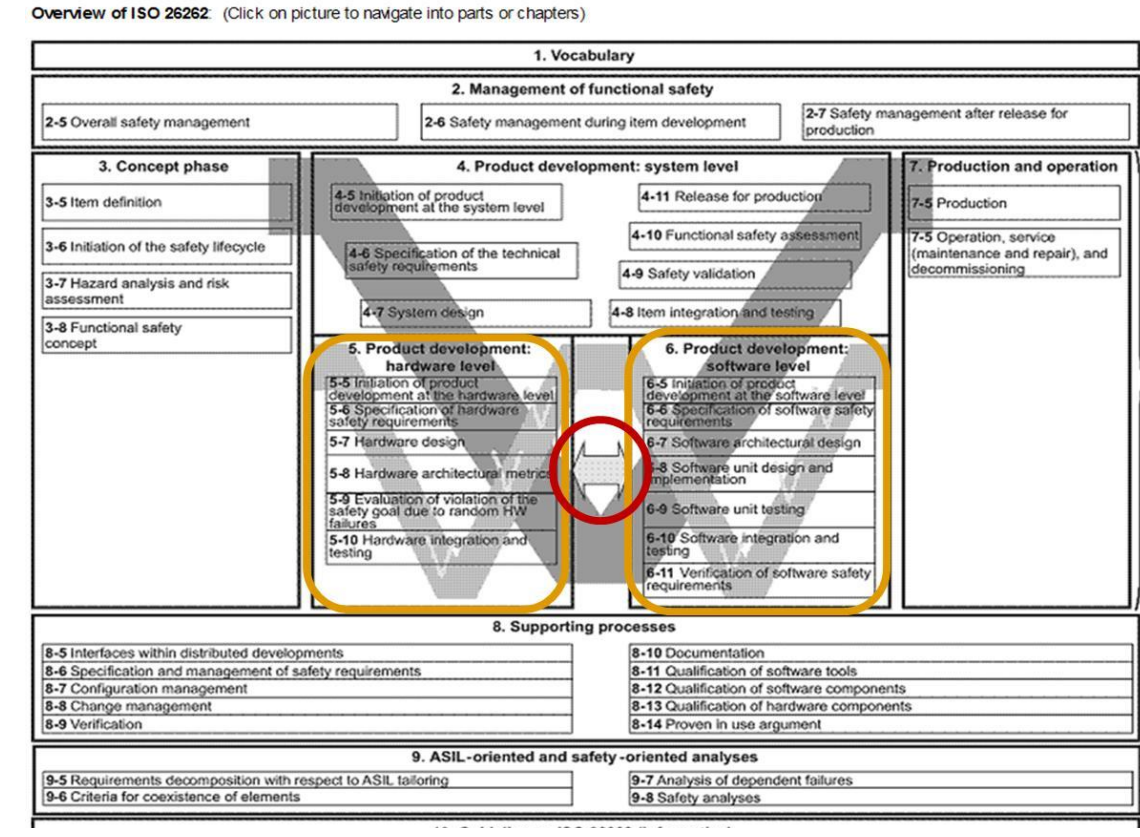
INTRODUCTION & MOTIVATION

KEY market demands

- Increasing safety level requested from OEMs
- ISO26262 standard up to ASIL-D
- Risk of product recall due to safety weakness
- More complex HW/SW automotive systems

Problem Areas

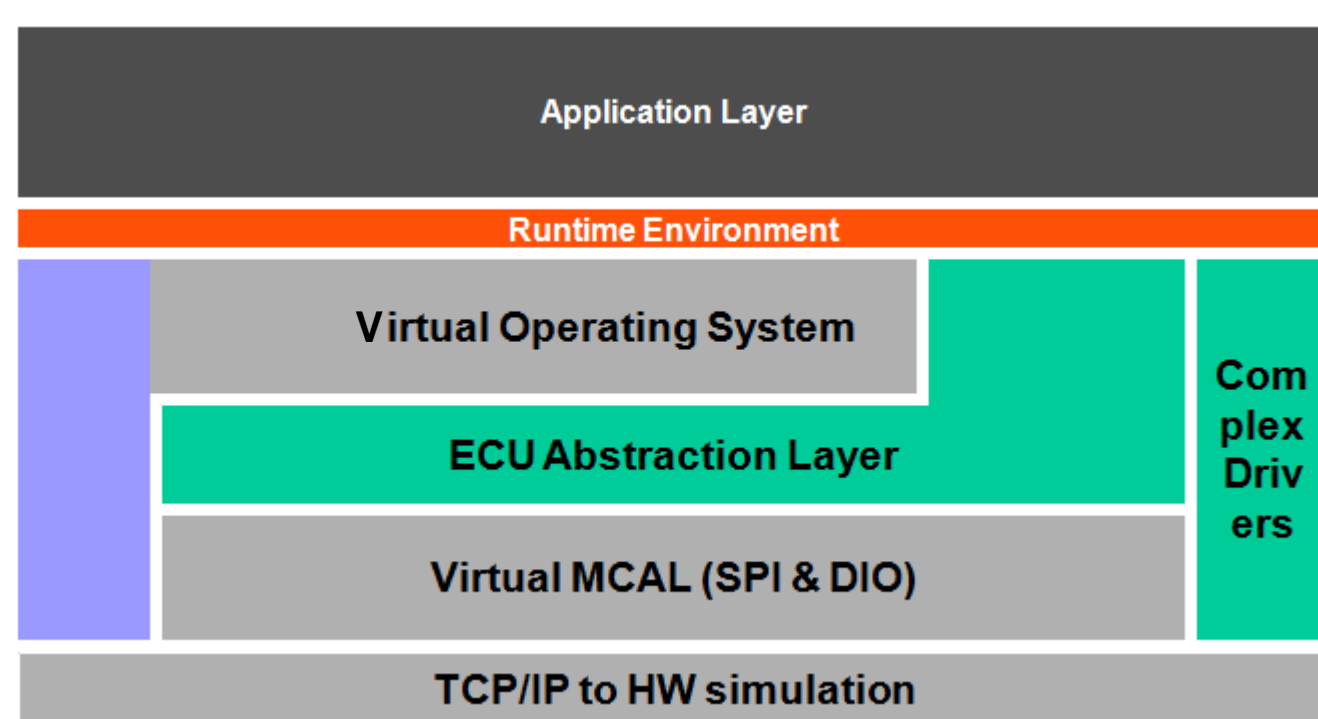
- late verification of SW driver interface to ASIC design can lead to ASIC redesign iterations
- late verification of safety architecture
 - fault injection only theoretically
 - late verification of HSI (e.g. SPI)
 - only possible with the first ASIC samples



OBJECTIVES

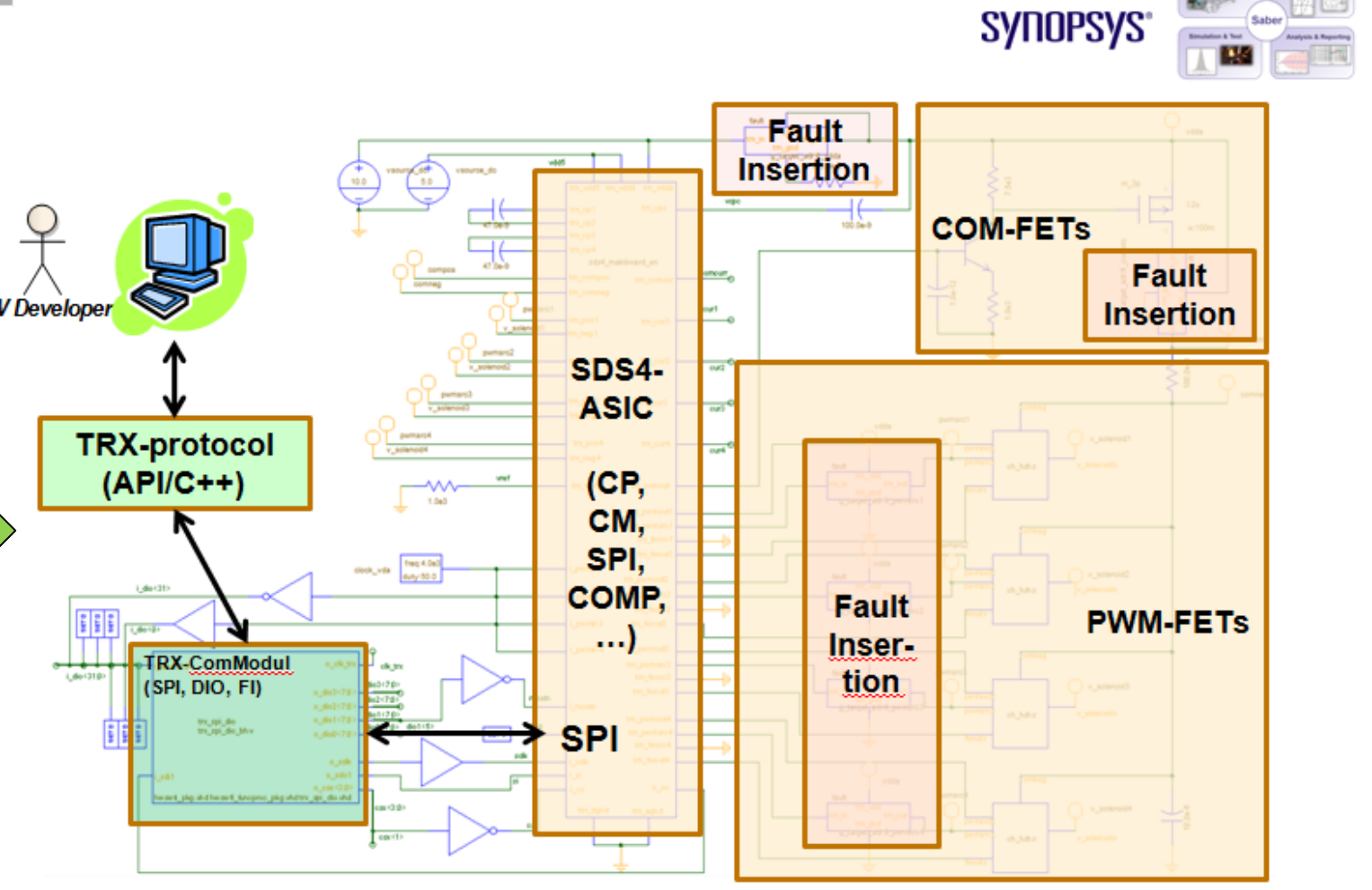
Early Integration	<ul style="list-style-type: none"> HW/SW-Cosimulation Early verification of HSI interface (e.g. SPI) 	<ul style="list-style-type: none"> Time to market 4-5 months earlier less ASIC redesign cycles
Fault modeling	<ul style="list-style-type: none"> Verification of functional safety concepts (system architecture) Regression testing 	<ul style="list-style-type: none"> Robust design quality improvement
Re-use	<ul style="list-style-type: none"> of HW tool chain and system models (VHDL-AMS/VHDL/C++) of SW tool chain and driver libs (compiler, debugger) 	<ul style="list-style-type: none"> No additional invest

RESULTS-1: Virtual HW-Prototype & Software Environment

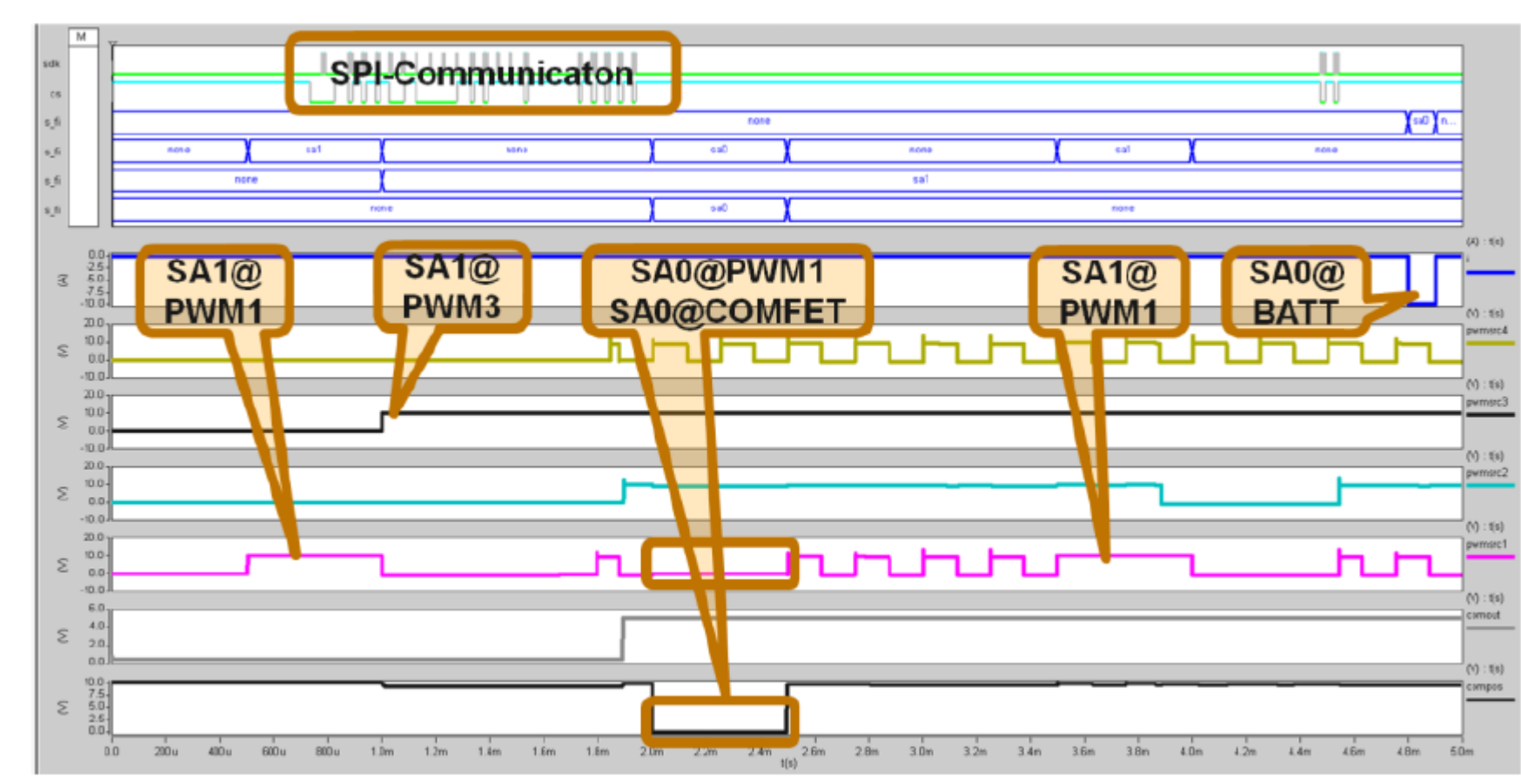


- Simulated AUTOSAR Software Architecture on PC Workstation
- Virtual MCAL layer and RTOS
- Use of ETAS ISOLAR EVE C++ framework

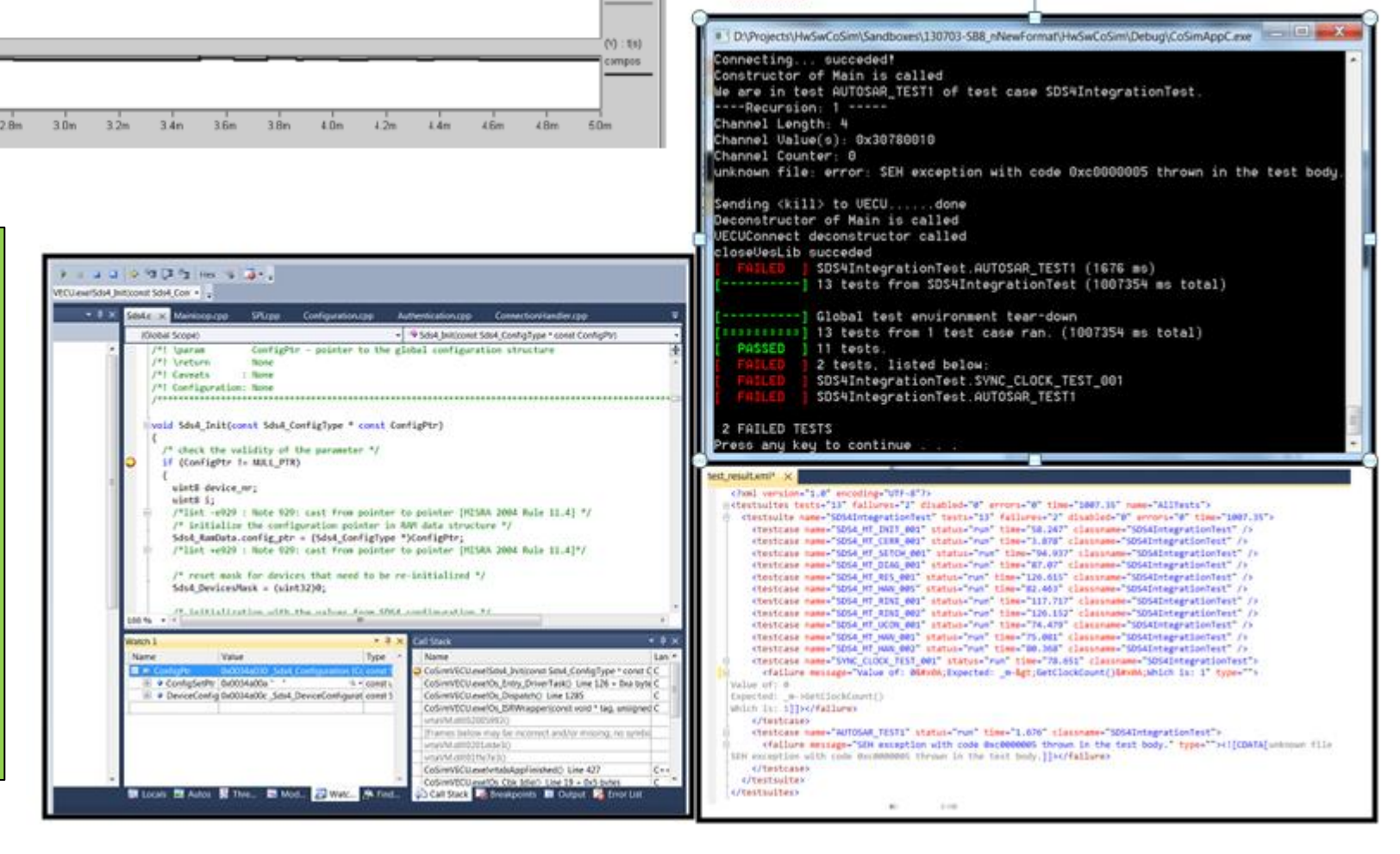
- Virtual Hardware Prototype (Synopsys Saber)
- Communication Module (TRX) offers access to software developer (DIO, SPI)
- Simulation of analog-mixed-signal components



RESULTS-2: HW/SW Co-Simulation & Fault Injection



- Automatic tests with Google Test framework
- Software Development in Visual Studio
- Fault Insertion in SW and HW



CONCLUSIONS

Validation of ASIC/HW Specification	<ul style="list-style-type: none"> Alignment with virtual models (VHDL, VHDL-AMS) Verification of HW/SW interface (e.g. SPI, DIO)
Regression Test	<ul style="list-style-type: none"> VHDL-Test benches for ASIC (HW) SW unit testing
Fault Insertion & Analysis	<ul style="list-style-type: none"> Multiple and sequential failures (HW, CRC) SW faults (incomplete messages, wrong timing) Verification of functional safety concepts
Early HSI Integration	<ul style="list-style-type: none"> Virtual prototype of ASIC for SW unit test Early SW driver development possible

REFERENCES

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