2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Hardware Emulation: ICE vs Virtual

A Mano-a-Mano Duel for Supremacy

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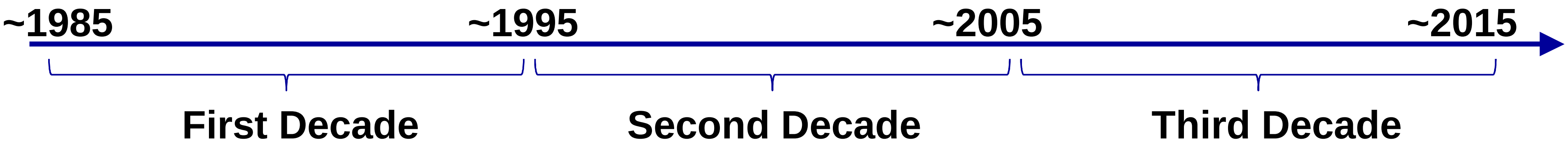
Agenda

- Hardware Emulation Timeline
- Hardware Emulation Evolution
  - The Objectives, The Modes, The Targets
  - The Usage
  - The Technology
- ICE versus Virtual
  - In-Circuit-Emulation (ICE) Mode
    - What is it?
    - Why Customers use ICE?
  - Virtual (or Acceleration) Mode
    - What is it?
    - Why Customers use Virtual Mode?
  - Advantages and Disadvantages

Hardware Emulation Timeline

FPGA-Based	FPGA-Based & Custom	FPGA-Based & Custom
In-Circuit-Emulation (ICE)	ICE & HDL Acceleration	ICE, All Types of Acceleration
• Zycad (1981) • Ikos (1984) • Quickturn (1987) • PiE (1990)	• Meta-Systems (Mentor) • Cadence (Quickturn) • Mentor (Ikos) • Akis Systems (Verisity/Cadence) • EVE	• Mentor • Cadence • Synopsys (EVE)



~1985 ~1995 ~2005 ~2015

First Decade

Second Decade

Third Decade

Hardware Emulation: Objectives, Modes, Targets

Early Years

- **One** Verification Objective
  - HW Functional Verification
- **One** Deployment Mode
  - In-Circuit-Emulation (ICE)
- **One** Target Industry
  - CPU/Graphics (largest designs in 1985-1995)

Today

- **Multiple** Verification Objectives
  - HW Functional Verification, HW/SW Integration, SW Validation, Power Domain Verification, Power Estimation, Performance Characterization,…
- **Multiple** Deployment Modes
  - ICE, Acceleration, Virtualization,…
- **Multiple** Target Industries
  - CPU/Graphics, Mobile, Video, Networking, Storage,...

Hardware Emulation: Usage

Early Years	Today
• **One** User	• **Multiple** Users (> 100)
• **Local** Resource	• **Central** Resource
• **No Remote** Access	• **Remote** Access
• **Unfriendly** to use	• **Easy** to use

Hardware Emulation: Technology

Early Years

- **Commercial FPGA** based
- Design Capacity: **330K**gates/Box[1]
- Setup Time: **Several Months**
- Compilation Time: **Days**
- Design Debug: **Partial Visibility**
- Cost: ~ **5$**/gate[1,2]
- Volume: **6,000mm^3**/gate
- Weight: **2gr**/gate
- Power: **50mWatt**/gate
- Reliability: **< One Day**

Today

- **Custom** silicon or **Commercial FPGA** based
- Design Capacity: **> 250M**gates/Box
- Setup Time: **< One Week**[3]
- Compilation Time: **Hours**[3]
- Design Debug: **100% Visibility**
- Cost: < **1cents**/gate
- Volume: **< 5mm^3**/gate
- Weight: **< 2mgr**/gate
- Power: **< 5uWatt**/gate
- Reliability: **> One Months**

(1): Quickturn Enterprise System (1992)

(2): Readjusted for inflation

(3): In the FPGA-based emulator the compilation time is adversely affected by the FPGA PAR time and the 100% visibility compromises significantly the speed of execution

Hardware Emulation: The Future

Hardware

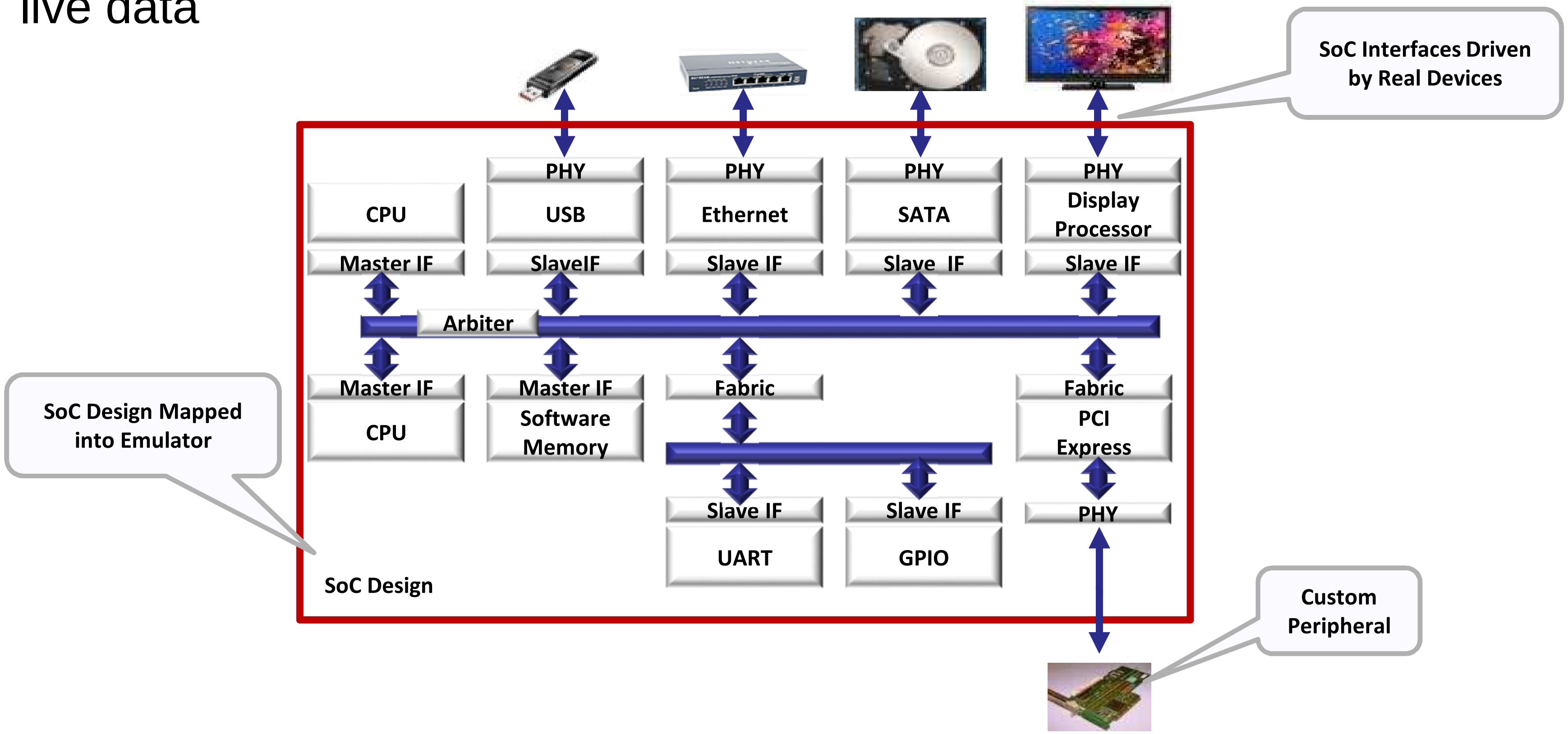
- Two basic architectures:
  - Commercial FPGA based
  - Custom Silicon based
- Capacity: several billion gates
- Smaller
- Faster
- Cheaper
- Highly reliable

Supporting Software

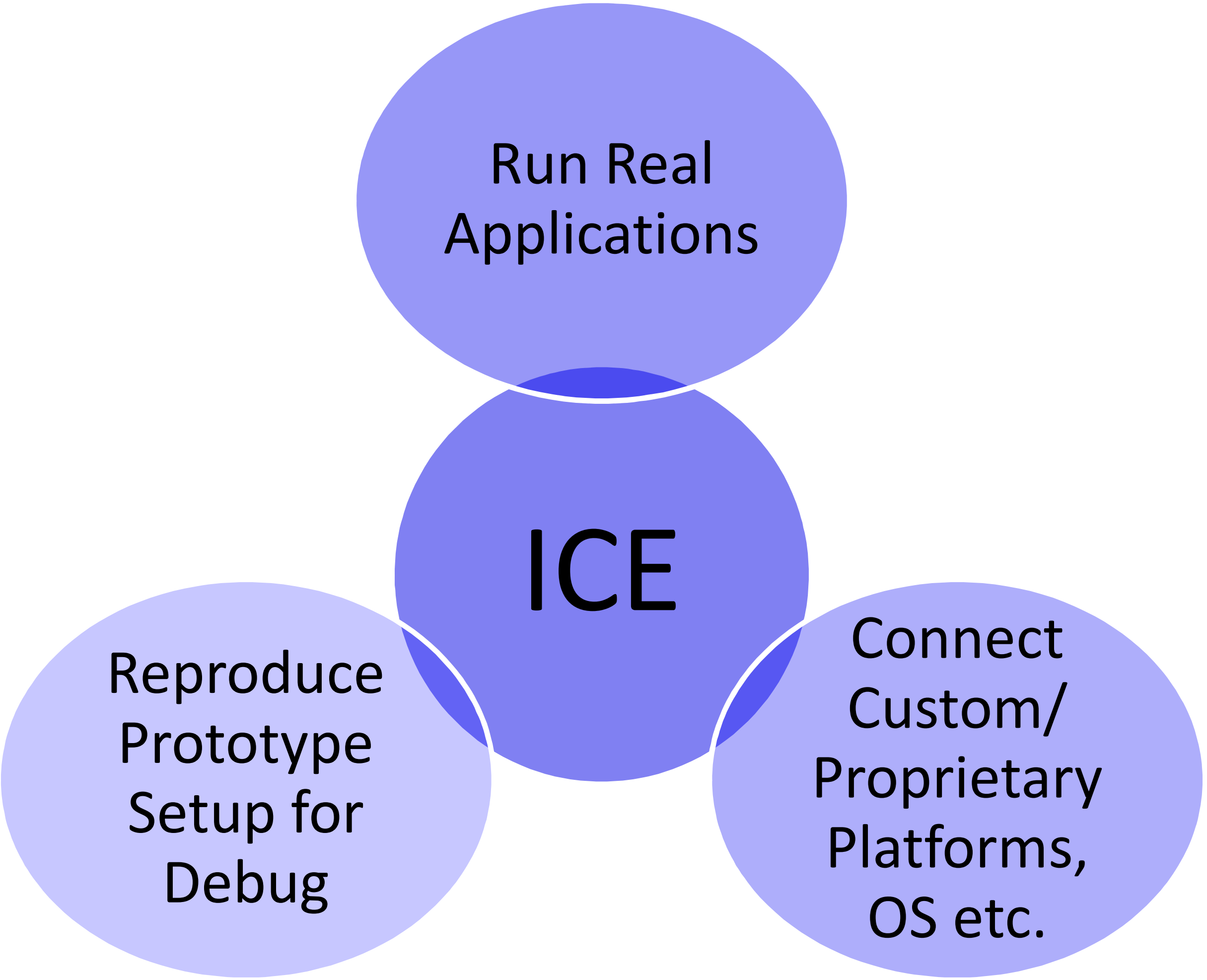
- Setup Time: ~ one day
- Compilation Time: less than one hour
- Integrated in a continuum of verification engines, sharing GUI and design database
- Access offered via datacenters
- ICE, acceleration, system validation, functional coverage, SVA, low-power verification, power estimation, DFT and test vector verification, performance characterization

ICE Mode: What Is It?

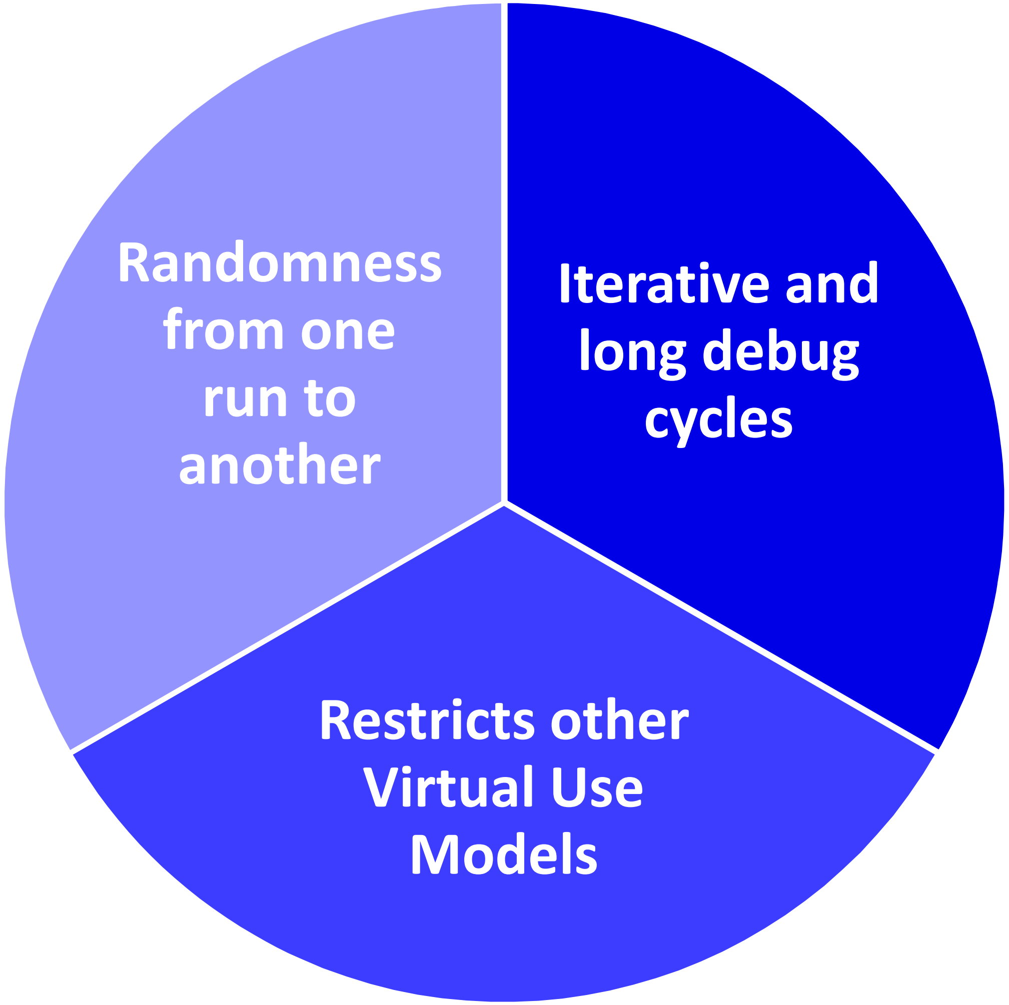
- In ICE mode, the emulator is plugged into a socket on the physical target system in place of a yet-to-be-built chip to support exercising and debugging the design-under-test (DUT) mapped inside the emulator with live data



Why Customers Use ICE


Run Real Applications
ICE
Reproduce Prototype Setup for Debug
Connect Custom/ Proprietary Platforms, OS etc.

Challenges using ICE



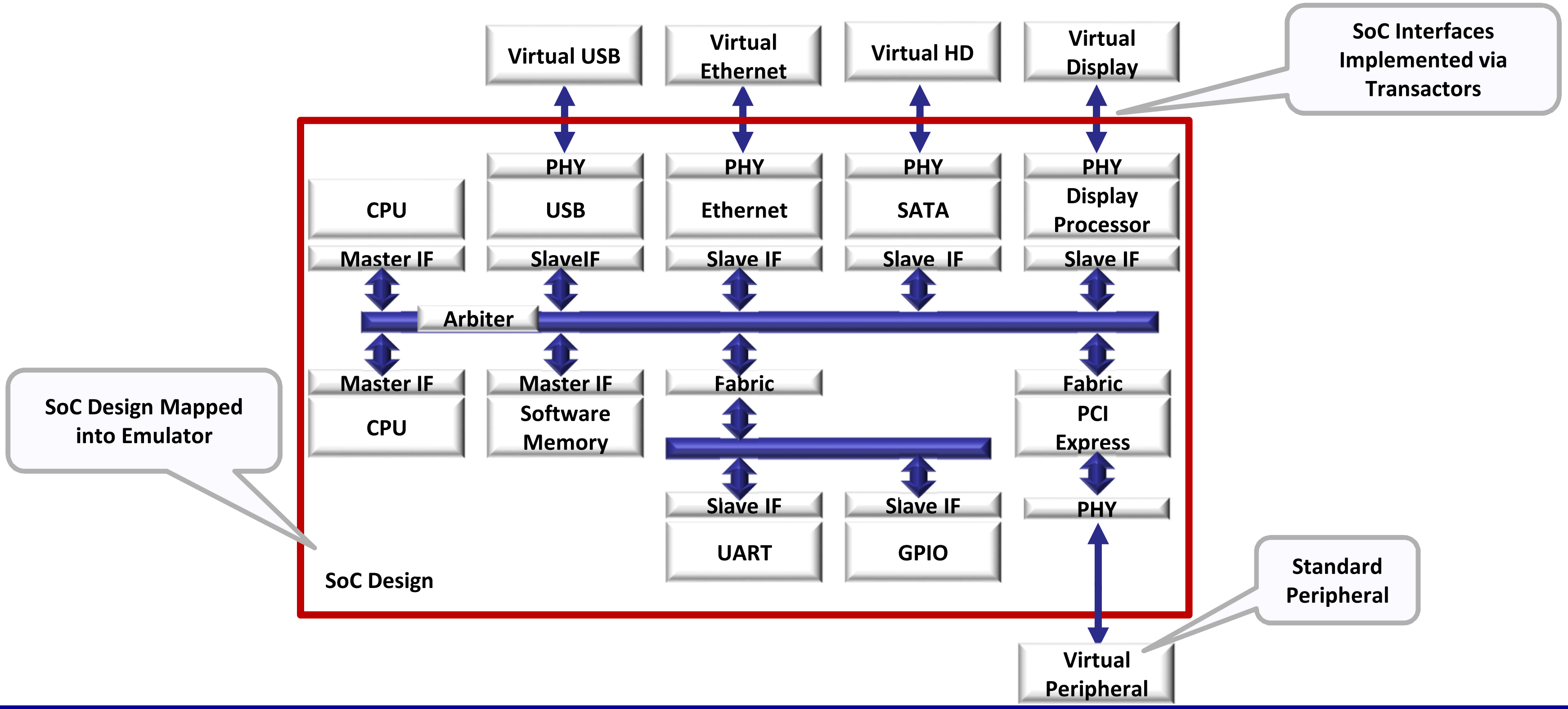
Randomness from one run to another

Iterative and long debug cycles

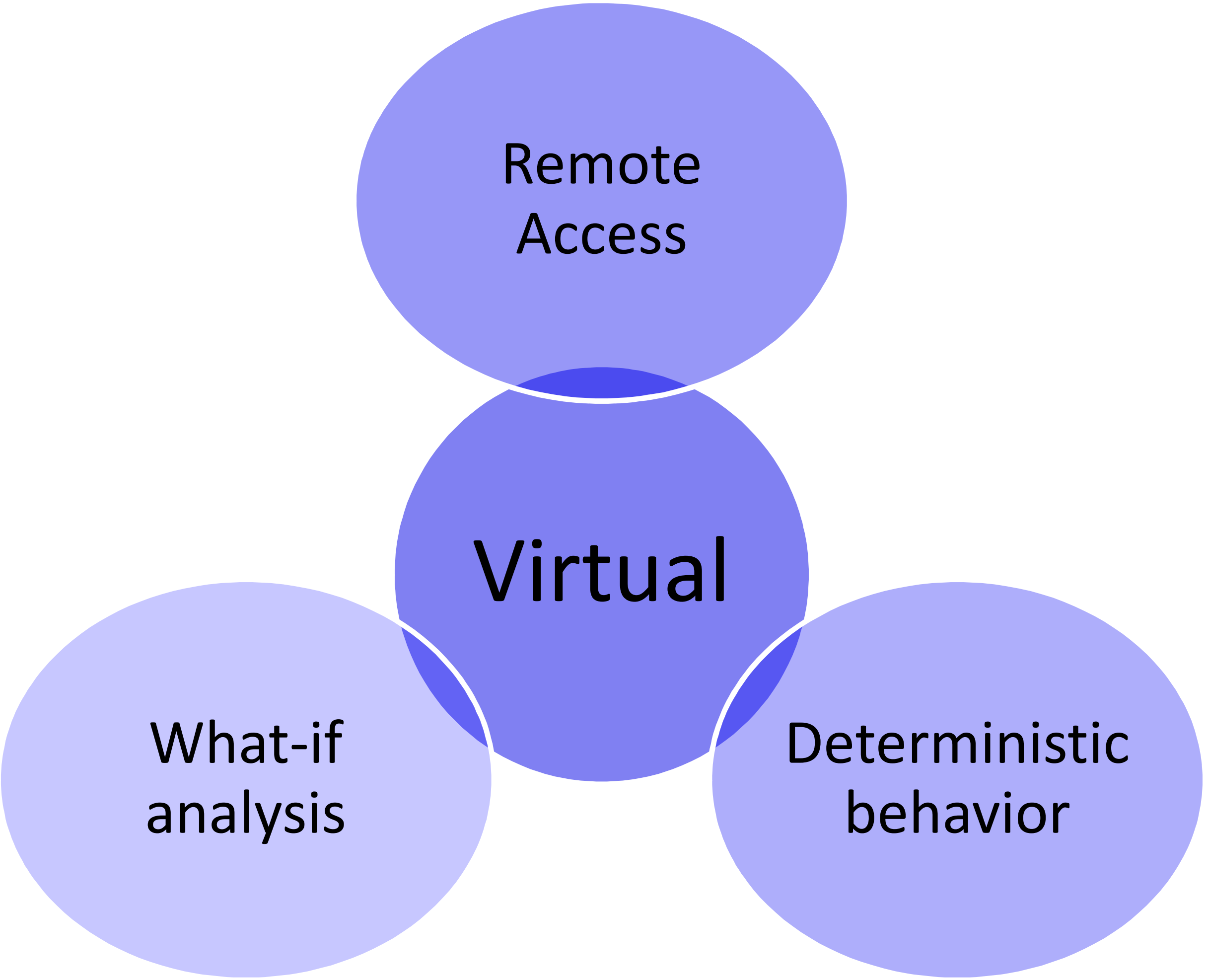
Restricts other Virtual Use Models

Virtual Mode: What Is It?

- In Virtual mode, the test environment is modeled in software at high-level of abstraction and connected to the design-under-test (DUT) mapped inside the emulator via a set of transaction-based interfaces



Why Customers Use Virtual Mode



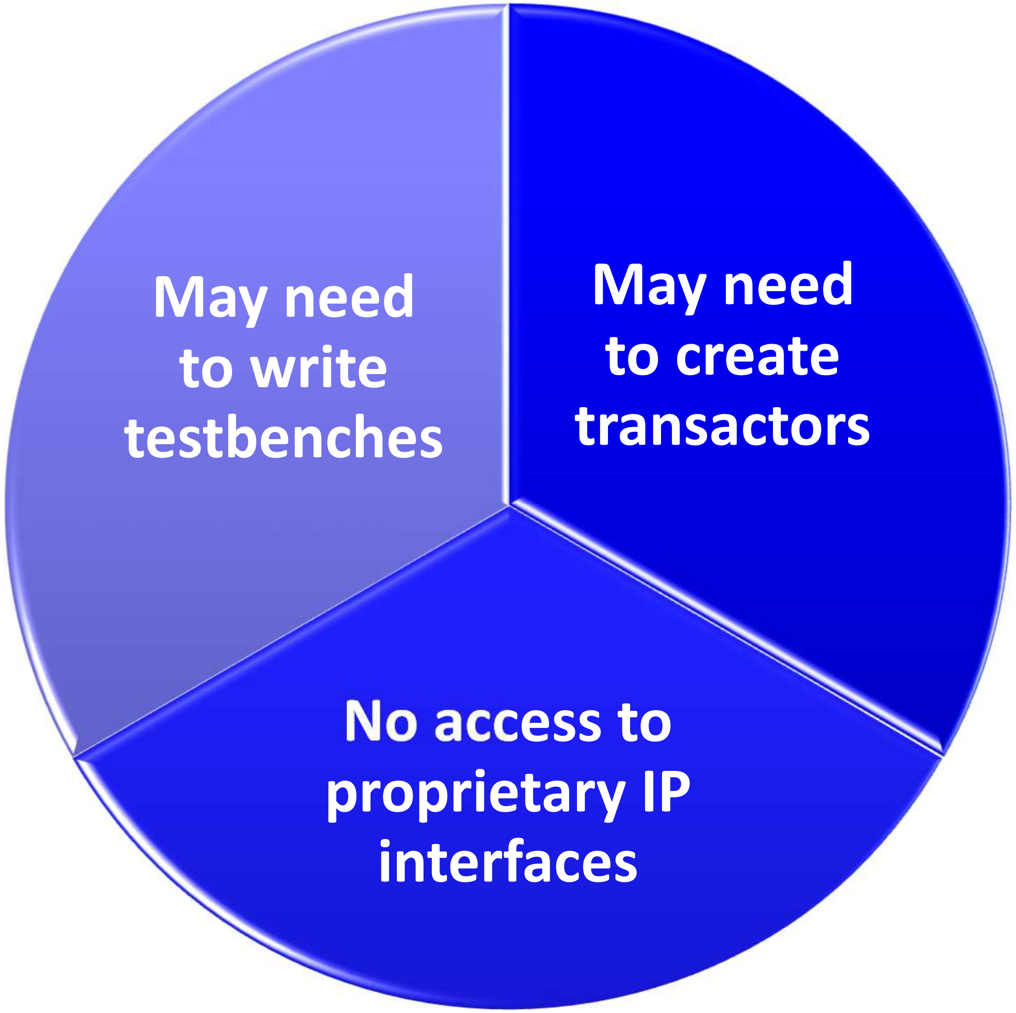
Remote Access

Virtual

What-if analysis

Deterministic behavior

Challenges using Virtual Mode



May need to write testbenches

May need to create transactors

No access to proprietary IP interfaces

ICE vs Virtual

Criteria	ICE	Virtual
Testbench Type	• Physical Target System o Run real applications or real traffic	• Virtual Target System
Testbench Creation	• No need to create testbenches; they are the target system	• Necessary to create tesbenches, a time-consuming, error-prone process
Interface between Target System and DUT	• Requires speed adapters to target system for each interface protocol • Significant H/W dependencies (reset circuitry, noise) • Board completion is in critical path; emulation cannot begin until board is ready • Lab setup becomes a bottleneck • Power hungry • Additional cost	• Requires transactors for each interface protocol • No H/W dependencies • Completion of S/W development is not in critical path; can begin with existing testbench and emulate parts of design incrementally • No power consumption • Less expensive than speed adapters
Customization	• ICE is critical for customized interfaces o Fidelity of the model o Non-standard interface o Knowledge (IP) can't be shared outside the company • Development platforms can be supplied by OEM vendors to early adopters • Reproduce FPGA Prototype Setup for Complete Debug	• Custom virtual interface protocols can be built but require unusual expertise not readily available

ICE vs Virtual

Criteria	ICE	Virtual
Flexibility	• Inflexible, difficult to modify • Restrict emulation access	• Flexible, easier to modify S/W than H/W • Ideal from remote access
Reusability	• Limited reuse; if next design has different interfaces, new board design required	• Highly reusable; transactors are written once and used many times
Productivity	• Hinders productivity	• Increases productivity
Reliability	• Complex, potentially not reliable	• No HW means highly reliable
Design Debug	• Not deterministic o Randomness from one run to another	• Deterministic o Repeatable behavior
Performance	• Run at maximum emulation speed	• May run at maximum emulation speed

Conclusion

- ICE and Virtual are not necessarily replacement for one another
- ICE is best to test the DUT with real traffic, and when proprietary interfaces are required
- Virtual is best for remote access, deterministic behavior, and what-if-analysis

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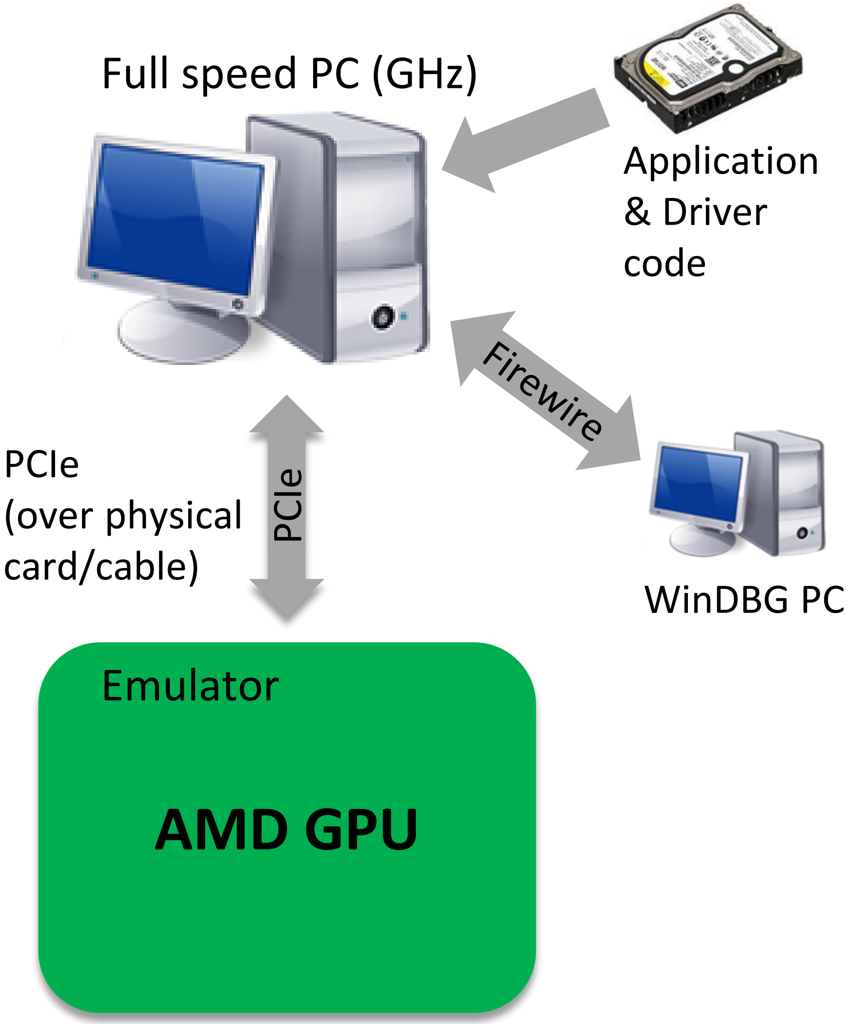
Hardware Emulation: ICE vs Virtual
User Experiences

Alex Starr, AMD

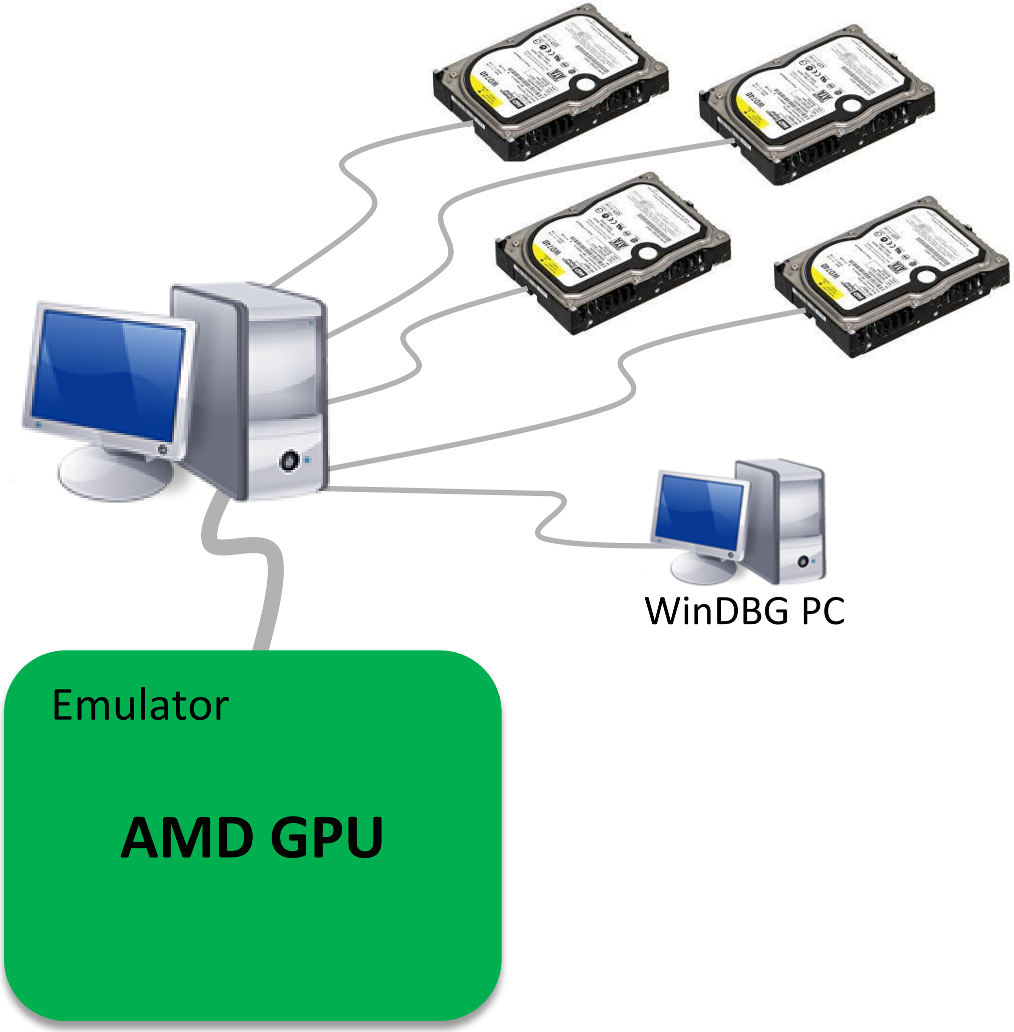
AMD | *Enabling today. Inspiring tomorrow.*

Traditional GPU Emulation Solution



- ICE: In-circuit emulation
- PCIe rate adaptor connects 'Test PC' to emulator
- Hard disk provides software
- Windows software debug done via additional PC running WinDBG
- Three main classes of testing done
  - Traditional Verification work
    - Linux Based
    - Bring up and initialization
    - Low level feature testing
  - OS Driver & User level code
    - Windows Based (Software Team)
    - Real Kernel Mode Driver
  - Feature/System diagnostics
    - Memory coherence
    - Power Gating
    - Early silicon bring up work

In-Circuit Challenges



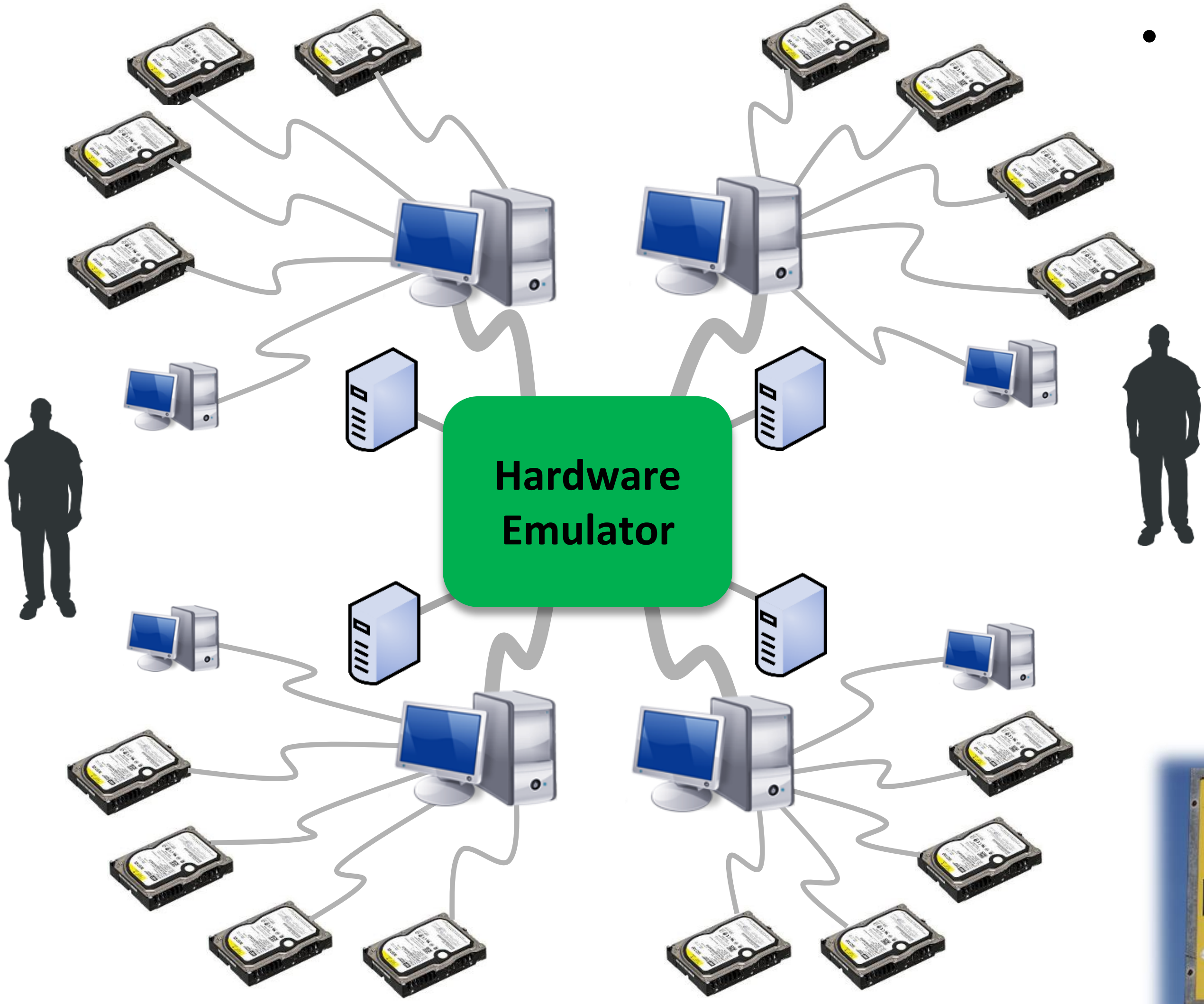
WinDBG PC

Emulator

AMD GPU

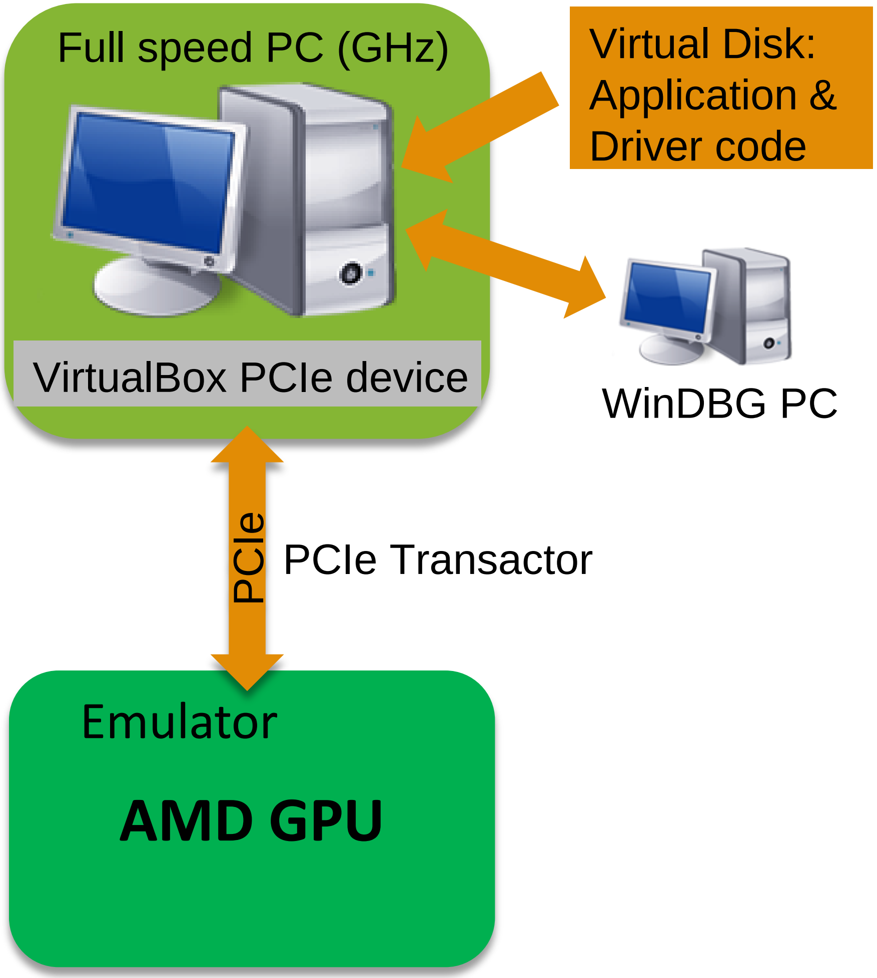
- Efficiency, productivity and reliability challenges
  - Physical disk swapping
  - Ethernet controlled disk switchers
  - Complex target cabling a reliability problem
  - Custom hardware for “Test PC”
  - No save and restore

Multi-setup Complexity



- Efficiency, productivity and reliability challenges
  - Multiple setups increase complexity
  - Specific target hardware for each setup limits flexibility
    - On a single emulator and across sites
  - Humans cause problems!

Virtual Target Solution

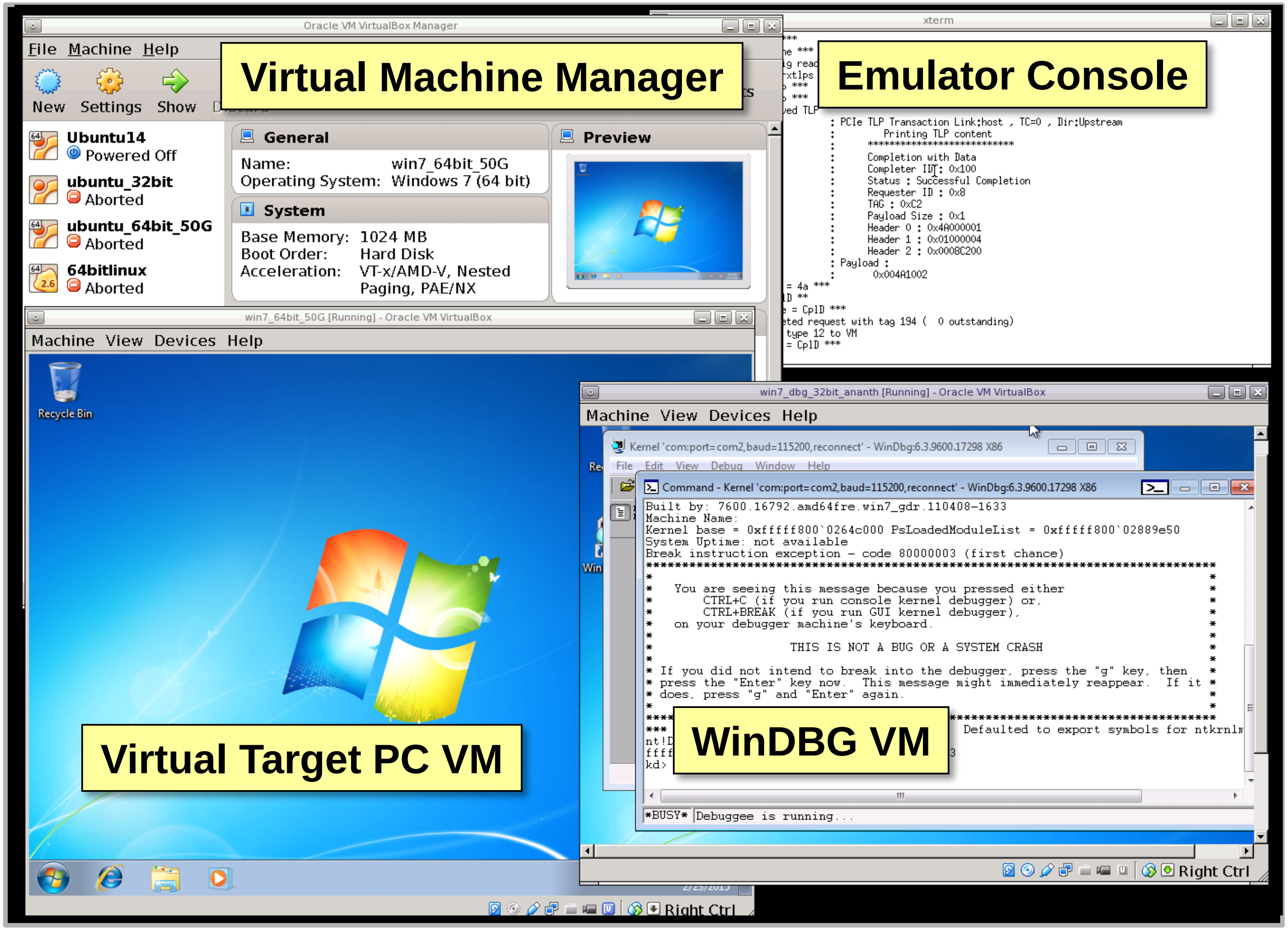


- Enable connection to virtualized host machines
- PCIe transactor connects from the host workstation to the emulation hardware
  - No in-circuit PCIe connection
- Removal of all in-circuit target devices
- Virtual disks allow images to be used by the VM: no physical disk swapping
- Disk images can be prepared offline in standalone VM
- WinDBG host connection maintained for software debug

Virtual Targets: Reduced Complexity

Challenge Area	Traditional ICE Solution	Virtual Solution
‘Test PC’ hard disk changes	Physical Disk Swapping Ethernet Controlled Disk Switchers	Eliminated: VM disk image selection
Save/Restore	Not possible	Possible (untested)
Cabling Complexity	Complex Target/Test PC cabling	Just single cable to workstation
“Test PC” custom hardware requirements	Custom hardware for “Test PC” required	Generic workstation, unless specific new silicon required
Data Center Compatibility	“High touch”	“No touch”
Flexibility	Physical target/emulator board constraints	Dynamically reconfigurable targets via VM

End User Experience


Oracle VM VirtualBox Manager
File Machine Help
New
Settings
Show
Ubuntu14
Powered Off
ubuntu_32bit
Aborted
ubuntu_64bit_50G
Aborted
64bitlinux
Aborted
General
System
Preview
win7_64bit_50G [Running] - Oracle VM VirtualBox
Machine View Devices Help
Recycle Bin
Right Ctrl
xterm
win7_dbg_32bit_ananth [Running] - Oracle VM VirtualBox
Machine View Devices Help
Kernel 'com:port=com2,baud=115200,reconnect' - WinDbg:6.3.9600.17298 X86
File Edit View Debug Window Help
Command - Kernel 'com:port=com2,baud=115200,reconnect' - WinDbg:6.3.9600.17298 X86
Right Ctrl

Virtual Machine Manager

Name: win7_64bit_50G
Operating System: Windows 7 (64 bit)

Base Memory: 1024 MB
Boot Order: Hard Disk
Acceleration: VT-x/AMD-V, Nested Paging, PAE/NX

Emulator Console

```
***
ne ***
ig reac
rxtlps
o ***
o ***
ved TLP
         : PCIe TLP Transaction Link:host , TC=0 , Dir:Upstream
         :        Printing TLP content
         :      *************************
         :      Completion with Data
         :      Completer ID : 0x100
         :      Status : Successful Completion
         :      Requester ID : 0x8
         :      TAG : 0xC2
         :      Payload Size : 0x1
         :      Header 0 : 0x4A000001
         :      Header 1 : 0x01000004
         :      Header 2 : 0x0008C200
         : Payload :
         :       0x004A1002
 = 4a ***
lD **
e = CplD ***
eted request with tag 194 (  0 outstanding)
 type 12 to VM
 = CplD ***
```

Virtual Target PC VM

WinDBG VM

```
Built by: 7600.16792.amd64fre.win7_gdr.110408-1633
Machine Name:
Kernel base = 0xfffff800`0264c000 PsLoadedModuleList = 0xfffff800`02889e50
System Uptime: not available
Break instruction exception - code 80000003 (first chance)
*******************************************************************************
*                                                                             *
*   You are seeing this message because you pressed either                    *
*       CTRL+C (if you run console kernel debugger) or,                       *
*       CTRL+BREAK (if you run GUI kernel debugger),                          *
*   on your debugger machine's keyboard.                                      *
*                                                                             *
*                   THIS IS NOT A BUG OR A SYSTEM CRASH                       *
*                                                                             *
* If you did not intend to break into the debugger, press the "g" key, then   *
* press the "Enter" key now.  This message might immediately reappear.  If it *
* does, press "g" and "Enter" again.                                          *
*                                                                             *
****                                       ************************************
***                                        Defaulted to export symbols for ntkrnlm
nt!D
ffff                                       3
kd>
*BUSY* Debuggee is running...
```

Advanced Virtual Options

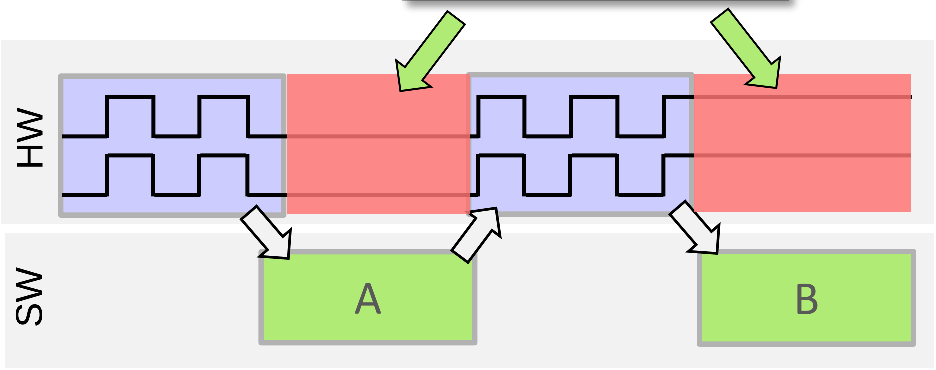
Coupled

- Deterministic
- Typically reduced throughput
- Emulator clocks stop to maintain determinism
- Great for debugging
- Keeps Verification engineers warm and cozy!

Decoupled

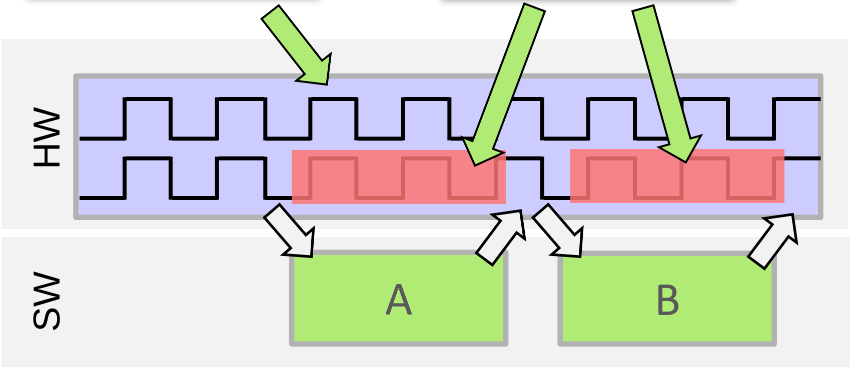
- Non-deterministic
- Full speed
- Same performance as ICE
- Streaming unidirectional monitors
- Can scare Verification engineers!

All threads blocked



Thread free running

Thread functionally blocked



ICE + Virtual Combination?

- Get the benefits of ICE and transactors
- Decouple transactors from ICE clock domains
- Concept: Controlled vs Uncontrolled clock domains
- “ICA”: In-Circuit Acceleration
- Don’t stop those clocks with dynamic targets attached

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VirtualBox Virtual Machine: Oracle. [Online] www.virtualbox.org