Generic Solution for NoC design exploration

Tushar Garg

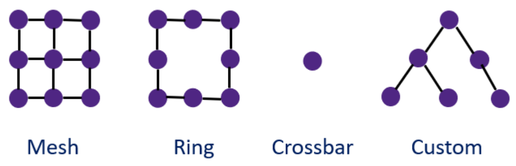
Ranjan Mahajan

Problem Statement/Introduction

- Interconnect is one of the key component in System
- Important to analyze power and performance of Interconnect in full use case-based scenario
- Growing complexity of design evolved Interconnect from shared interconnects or crossbar to Network on Chip
- Disadvantages of Crossbar Interconnect:
  - Single channel, global interconnection
  - Low bandwidth, high latency
  - High power consumption and scalability
- To overcome these problems, NoC was introduced:
  - Several cores are connected through network of routers
  - Routers arranged according to different topologies
  - Topology with different routing algorithms to get best results
- Paper presents NoC TLM model which can support multiple topologies, its architectures and its routing mechanisms

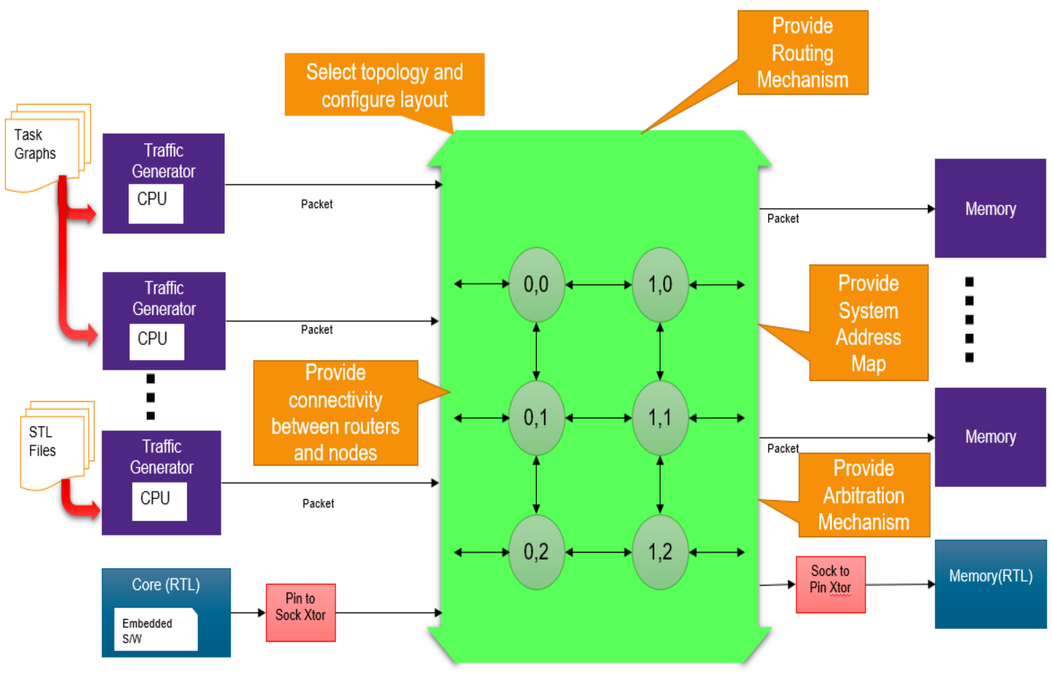
Proposed Methodology/Advantages

- Currently no NoC TLM model which supports multiple topologies and its options
- Proposed Generic model of a NoC that allows exploration of system with NoC interconnects
  - Has important configurable options to mimic different NoC architectures
  - Configurable topology exploration options
  - Custom interfaces to mimic specific interconnect behavior
  - Detailed analysis views for root cause analysis and system optimization
- In this solution
  - User will start creating full system with Bus placeholder
  - Then select topology for the Bus:

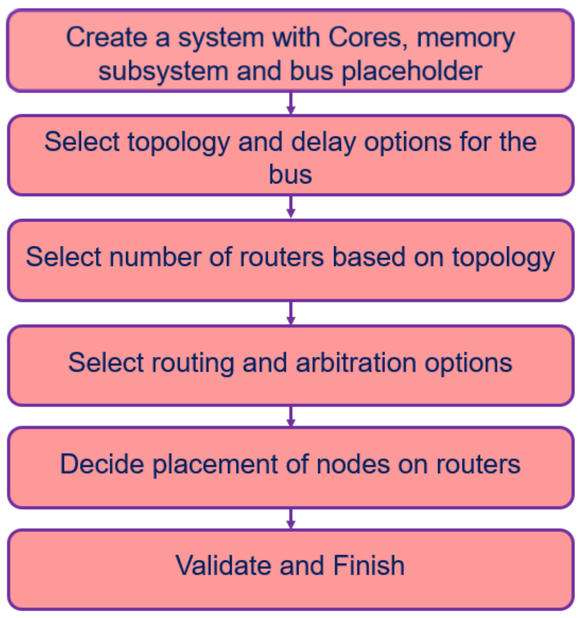


  - Configure selected topology, routing algorithm and arbitration mechanism
  - Configure connection of routers to nodes(initiators and targets) and generate the bus

Implementation Details/Diagram

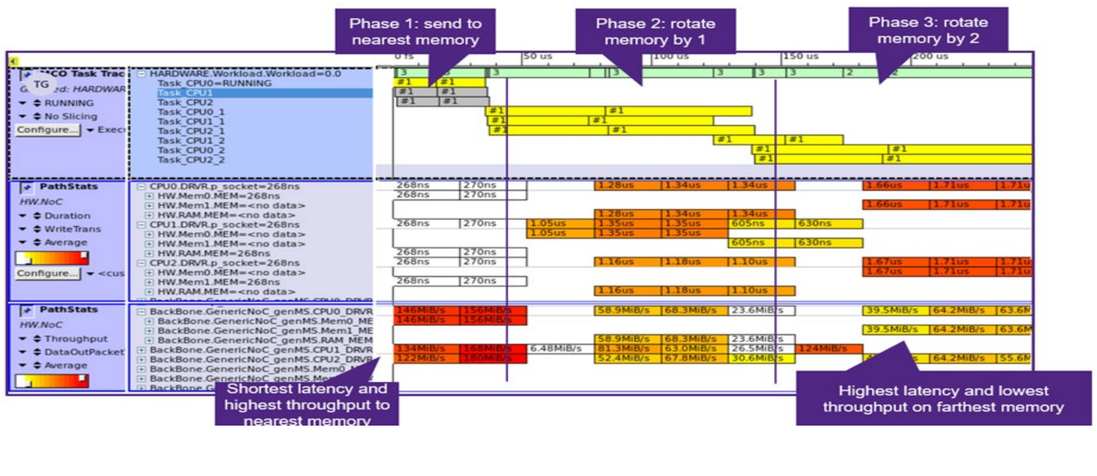


Implementation Details/Flow Chart



Results Table

- For the analysis, simple system was created in which for a single core, there are memories connected which are moving further away from the core
- As seen in Figure, when the memory is at shortest distance from the core, then is shortest latency and highest throughput and moving further away, latency is increasing, and throughput is decreasing
- So, through this solution user can decide on NoC architecture which can be used for a particular SoC



Conclusion

- Generic model of NoC to provide capabilities to mimic typical NoC architectures
  - Supports multiple topologies for design exploration
  - Selectable topology options to explore design options
- Multiple configuration knobs to explore design space for NoC architectures
  - Customization options to implement specific NoC logic
  - Out of box solution to tune typical NoC parameters
- Detailed analysis views for system optimization opportunity identification

REFERENCES

- Van den Brand, J. W. and Ciordas, C. and Goossens, K. and Basten, T., ‘Congestion-Controlled Best-Effort Communication for Networks-on-Chip
- Atienza, D., Angiolini, F., Murali, S., Pullini, A., Benini, L., De Micheli, G., ‘Network-on-Chip design and synthesis outlook.’, The VLSI journal, Elsevier, 2008.
- Alakesh Kalita & Kaushik Ray & Abhijit Biswas, ‘A Topology for Network-on-Chip’.
- Duato, J. and Yalamanchili, S., Ni, L., ‘Interconnection Networks.’, Morgan-Kayfmann, 2002.
- Songwen Pei, Xinyi Wang, “Shuttle: A Novel Topology Model for 3D NoC” Journal of Convergence Information Technology(JCIT) Volume 7, Number 19, Oct 2012.