

# Generic Solution for NoC design exploration

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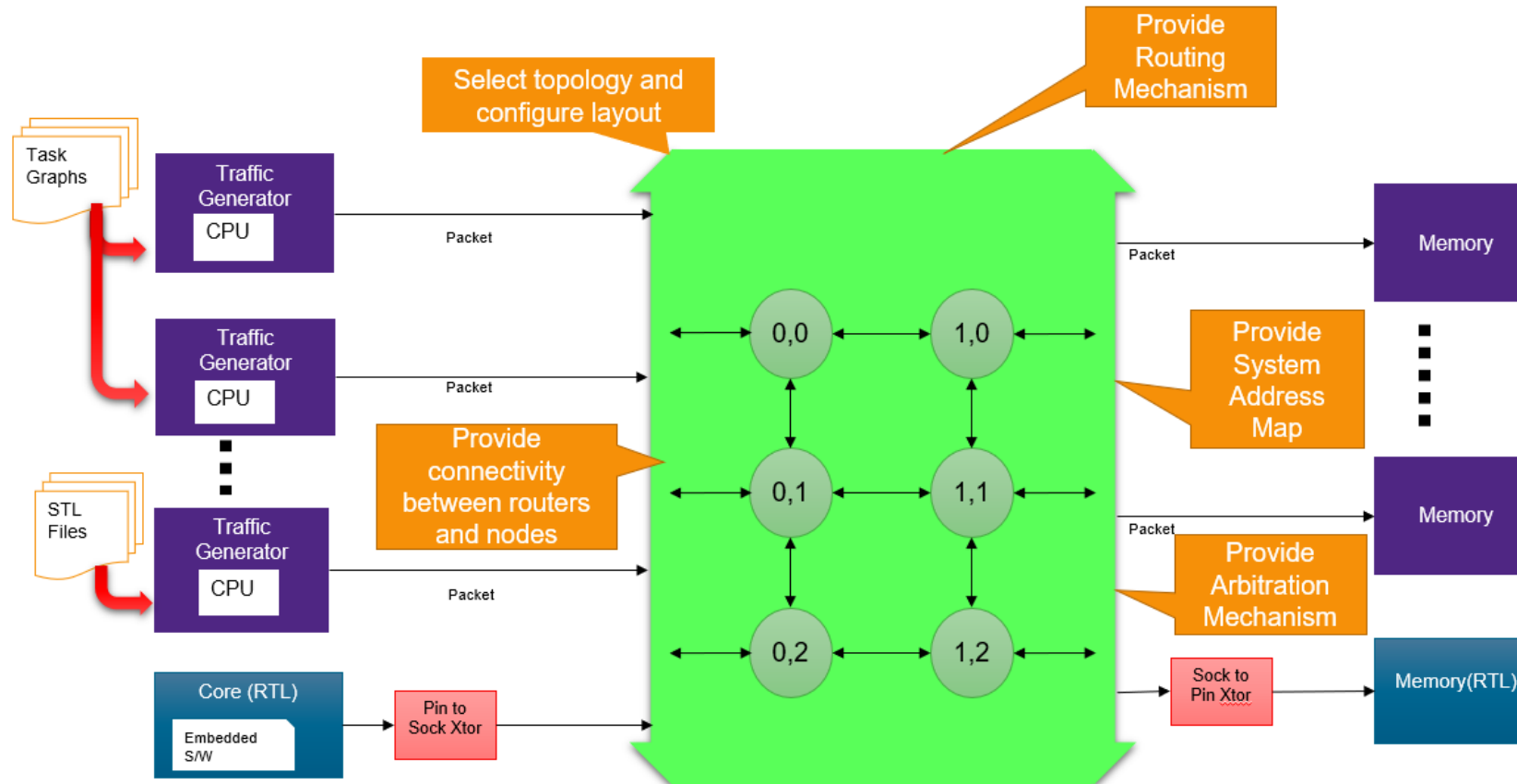
# Introduction

- As key component in System, it's important to analyze power and performance of Interconnect in full use case-based scenario
- Growing complexity of design evolved Interconnect from shared interconnects or crossbar to Network on Chip(NoC)
- Disadvantages of Crossbar Interconnect includes single channel, global interconnection , low bandwidth, high latency ,high power consumption and scalability
- To overcome these problems, NoC was introduced:
  - In which network of routers arranged according to different topologies
  - Topology with different routing algorithms to get best results
- Paper presents NoC TLM model which can support multiple topologies, its architectures and its routing mechanisms

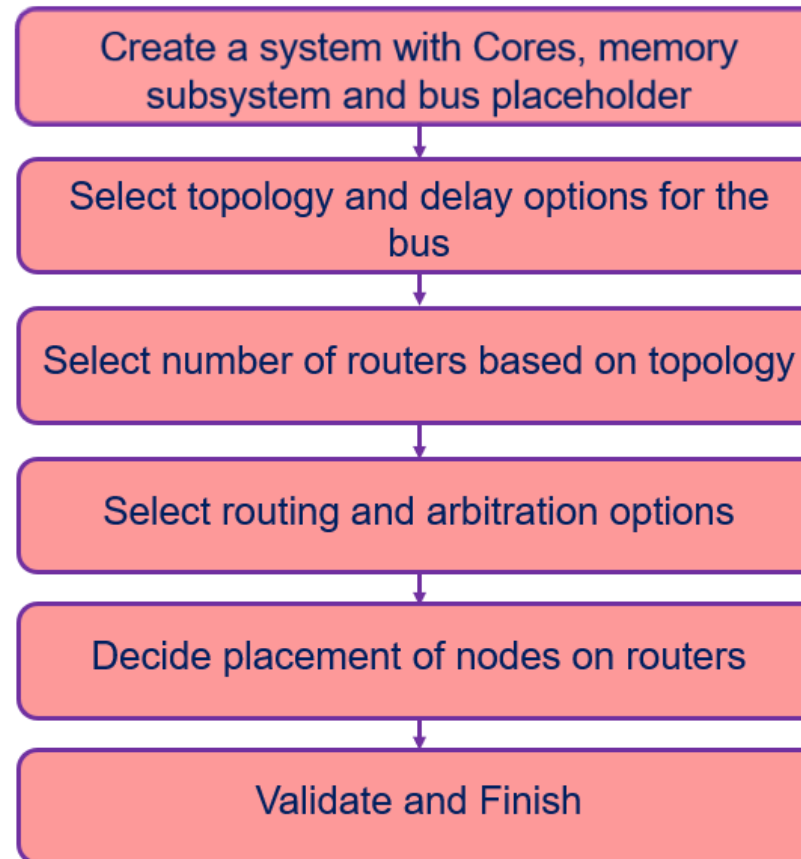
# Proposed Solution

- Currently no NoC TLM model which supports multiple topologies and its options
- Proposed Generic model of a NoC that allows exploration of system
  - Has important configurable options to mimic different NoC architectures
  - Configurable topology exploration options
  - Custom interfaces to mimic specific interconnect behavior
  - Detailed analysis views for root cause analysis and system optimization
- In this solution
  - User will start creating full system with Bus placeholder
  - Then select topology for the Bus
  - Configure selected topology, routing algorithm and arbitration mechanism
  - Configure connection of routers to nodes(initiators and targets) and generate the bus

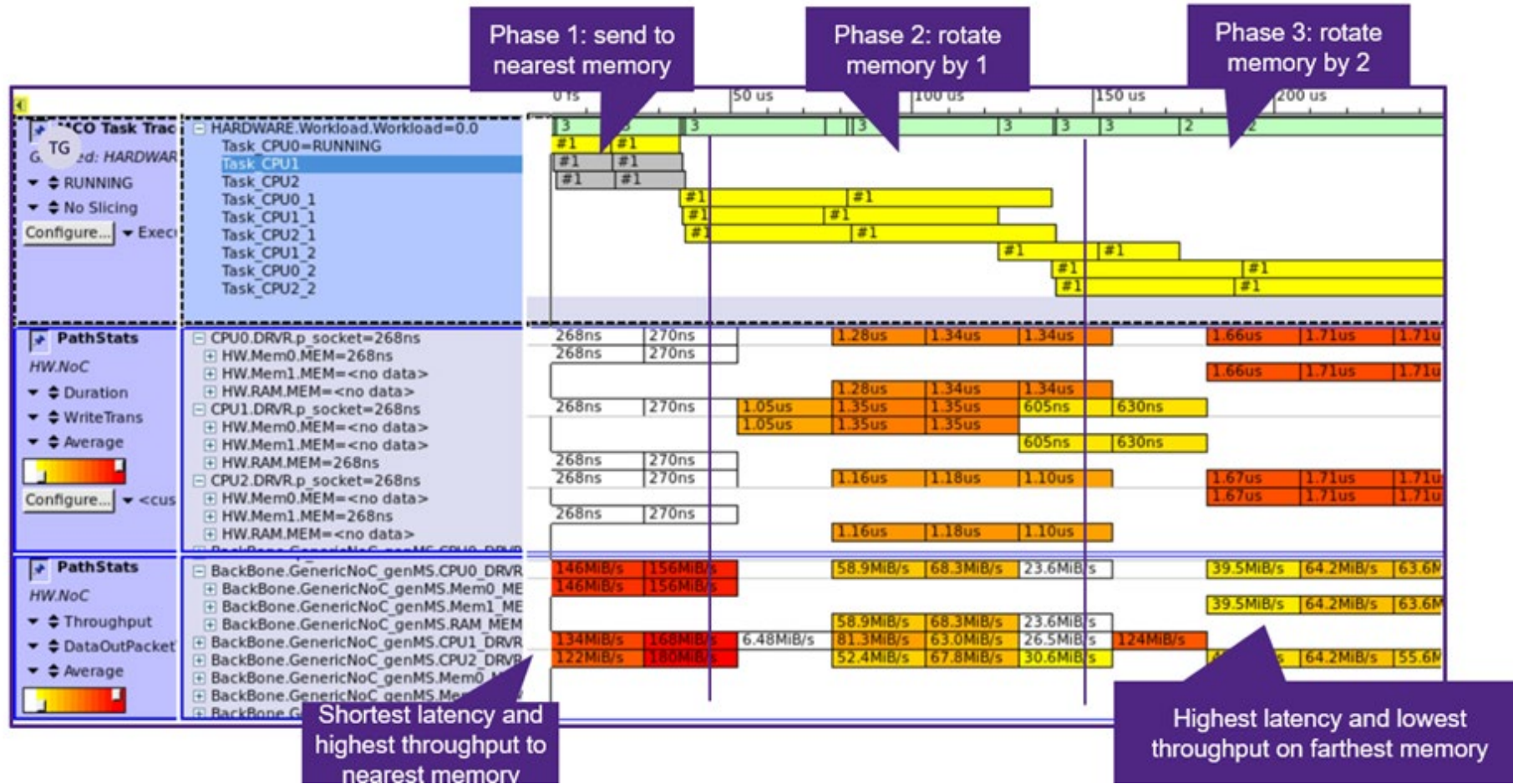
# Implementation Diagram



# Implementation Flow Chart



# Analysis Results



# Conclusion

- Generic model of NoC to provide capabilities to mimic typical NoC architectures
  - Supports multiple topologies for design exploration
  - Selectable topology options to explore design options
- Multiple configuration knobs to explore design space for NoC architectures
  - Customization options to implement specific NoC logic
  - Out of box solution to tune typical NoC parameters
- Detailed analysis views for system optimization opportunity identification

# References

- Van den Brand, J. W. and Ciordas, C. and Goossens, K. and Basten, T., ‘Congestion-Controlled Best-Effort Communication for Networks-on-Chip
- Atienza, D., Angiolini, F., Murali, S., Pullini, A., Benini, L., De Micheli, G., ‘Network-on-Chip design and synthesis outlook.’, The VLSI journal, Elsevier, 2008, 41, pp. 340 - 359.
- Alakesh Kalita & Kaushik Ray & Abhijit Biswas, ‘A Topology for Network-on-Chip’.
- Duato, J. and Yalamanchili, S., Ni, L., ‘Interconnection Networks.’, Morgan-Kayfmann, 2002.
- Songwen Pei, Xinyi Wang, “Shuttle: A Novel Topology Model for 3D NoC”



Questions?