2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Full Flow Clock Domain Crossing
- From Source To Sí

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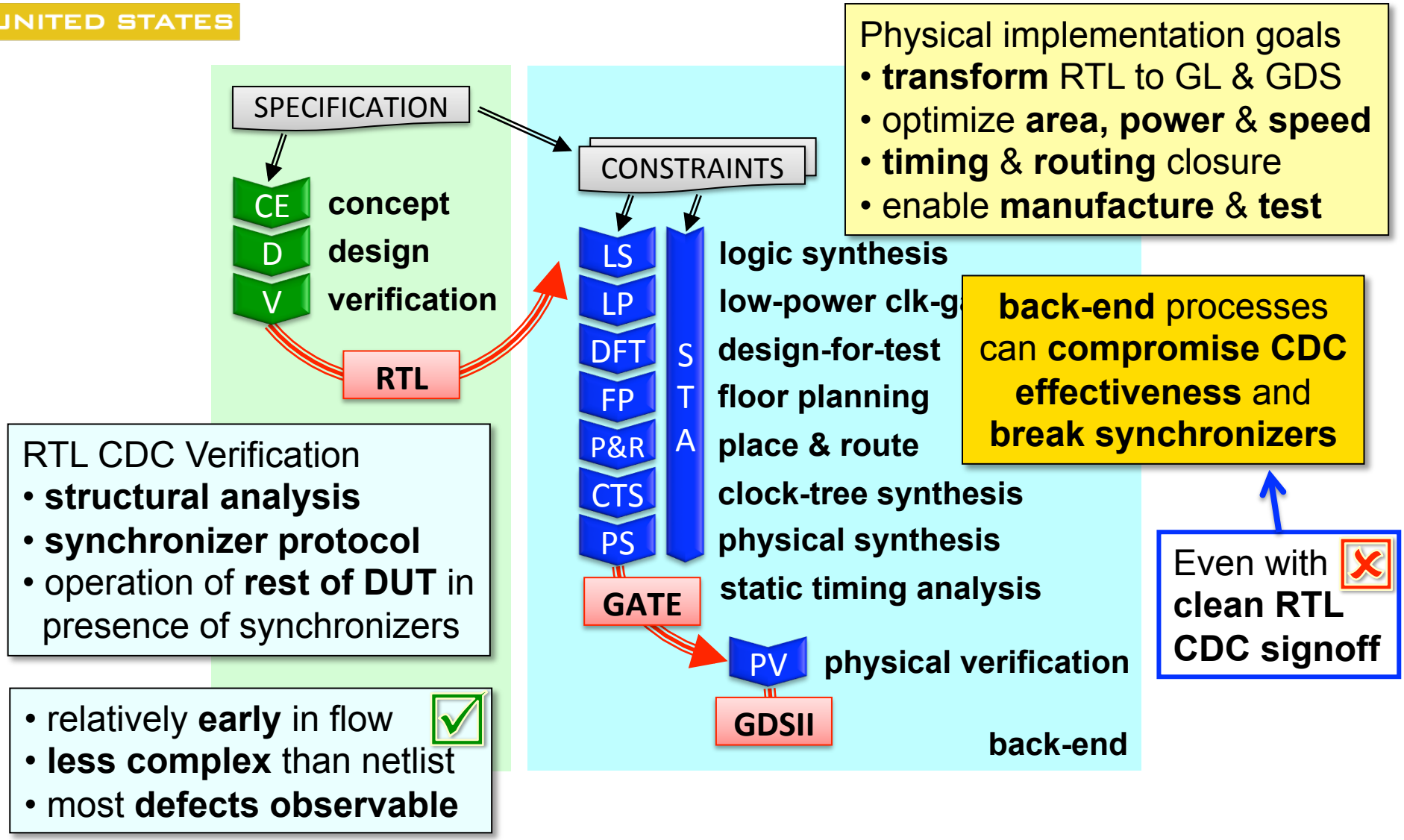
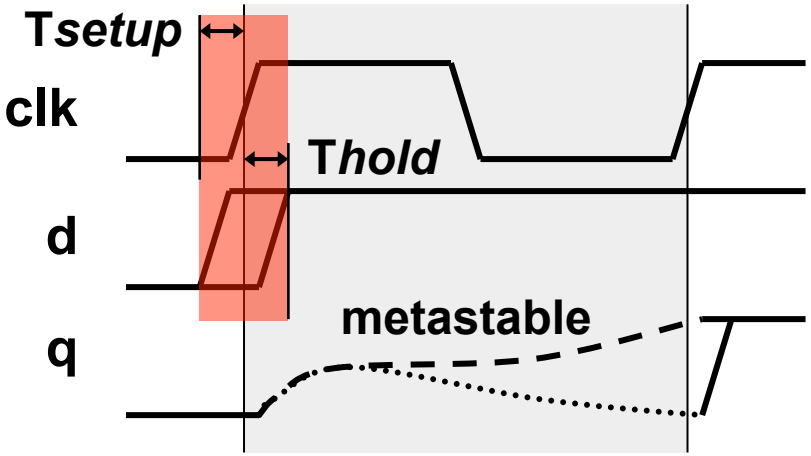
Introduction

- Overview
  - pre-silicon flow, metastability & MTBF, timing analysis for CDC & synchronizers
- Physical Requirements
  - 2FF, parallel, handshake & phase-detect synchronizers
  - timing requirements & failure modes
- Continuity & Closure
  - pragmatic solutions for encapsulation
  - SVA timing checks for continuity
  - closure using gate-level CDC analysis, constraints management & CDC review

Pre-Silicon Flow



Metastability & MTBF



$$MTBF = \frac{e^{Ts/Tc}}{T_w F_c F_d}$$

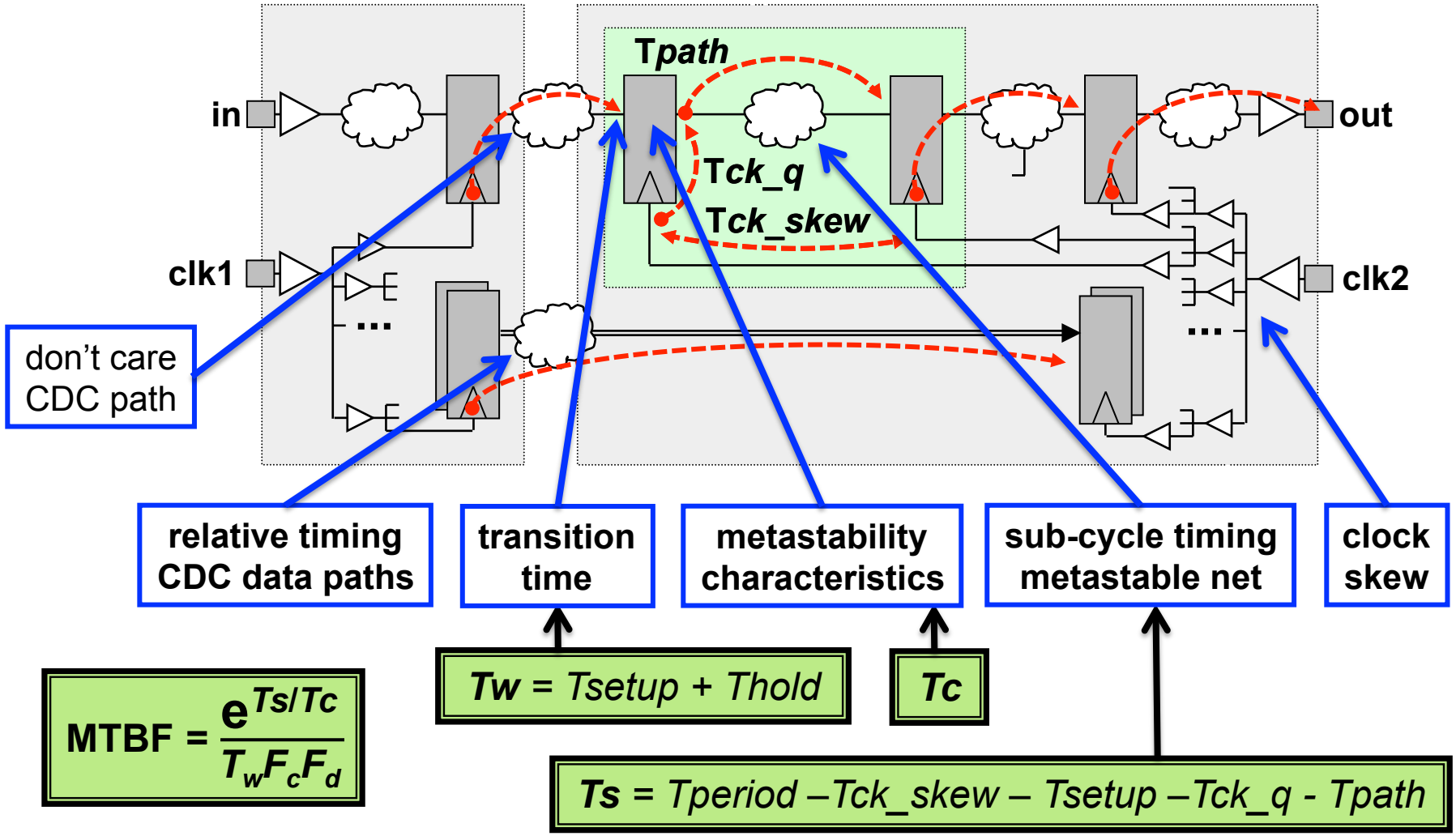
Technology & Implementation

T_s = settling window
T_c = settling time constant
T_w = window of susceptibility
F_c = clock frequency
F_d = data update rate

Concept & Application

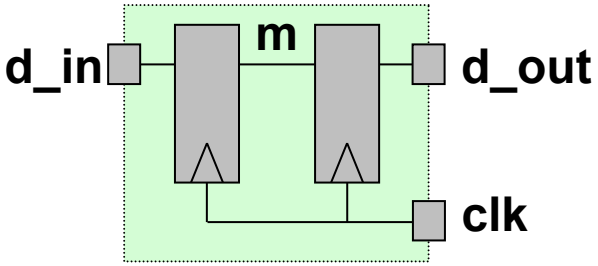
- **Violation** of setup or hold times causes **metastability**
  - **unstable** state eventually decays to 0 or 1, but **unpredictable**!
  - **real-life** transistor effect, not observable in simulations or formal
  - **cannot be avoided**, must be designed around & managed
- **Mean Time Between Failures** (MTBF)
  - **probability** of metastability **not decaying** to stable legal value in time for the next sampling event => catastrophic failure

Timing Arcs & CDC Paths



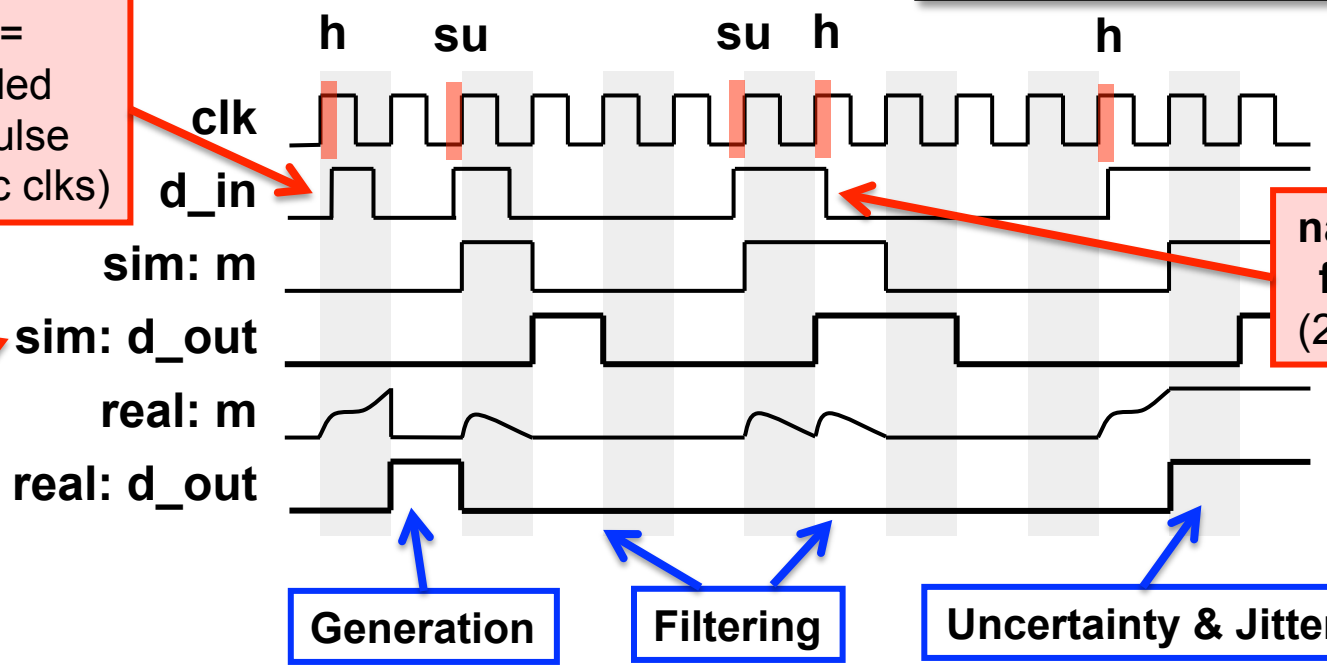
2FF Synchronizer

RTL CDC Requirements
- **no logic** on CDC path
- **no glitches** on D input
- **D stability** > 2 clock



PHY CDC Requirements
- **sub-cycle timing** on **m**
- fast **transition time** at **d_in**
- fast **metastability damping**
- no scan insertion 2nd FF
- tight clock-skew tolerance

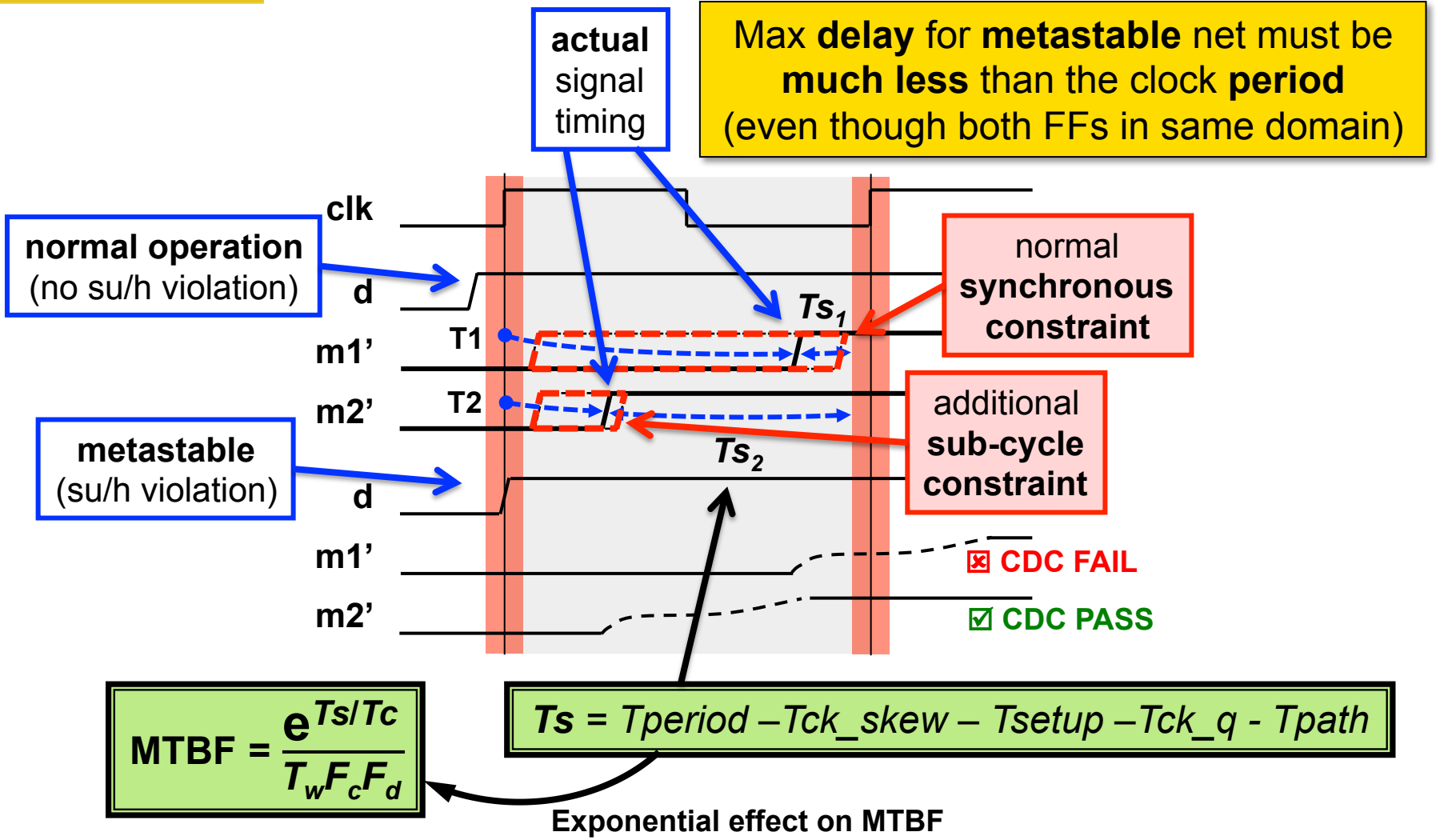
glitch = unsampled narrow pulse (≈ many src clks)



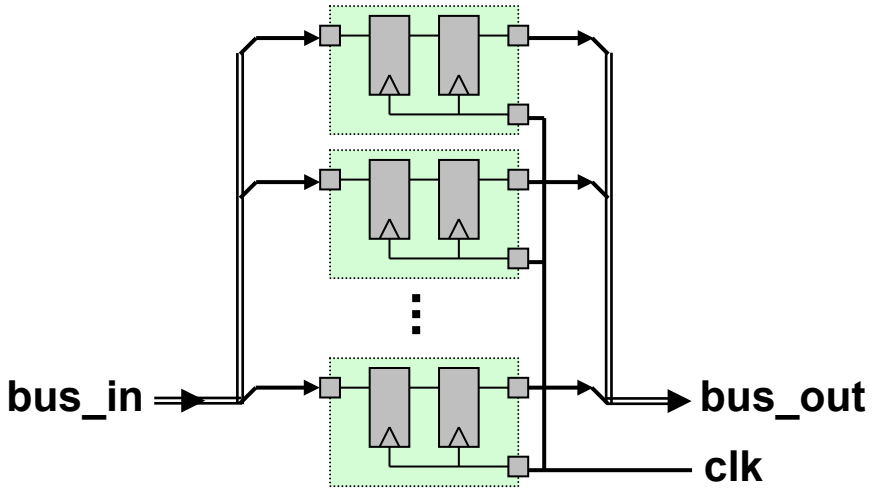
RTL or **GL** sim

narrow pulse **filtered** out (2 clk edges!)

Failure: Sub-Cycle Timing



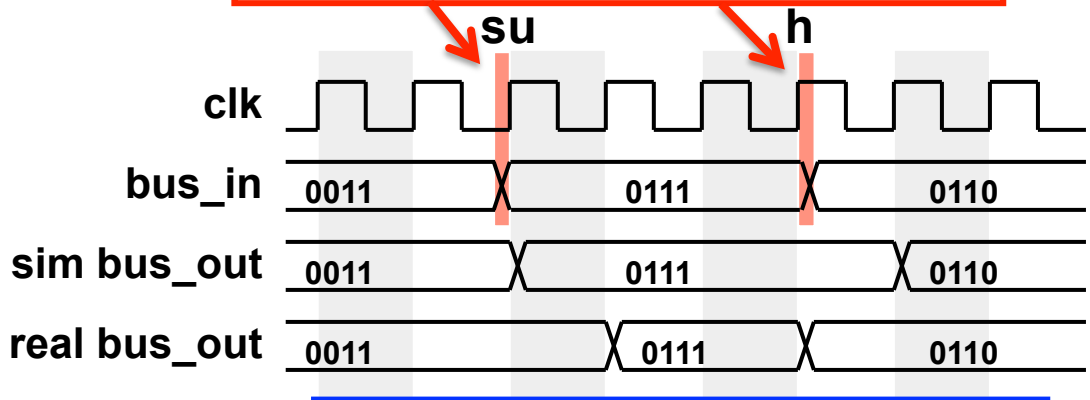
Parallel Synchronizer



RTL CDC Requirements
- **bus is gray-coded** at source (only one bit change per clock)

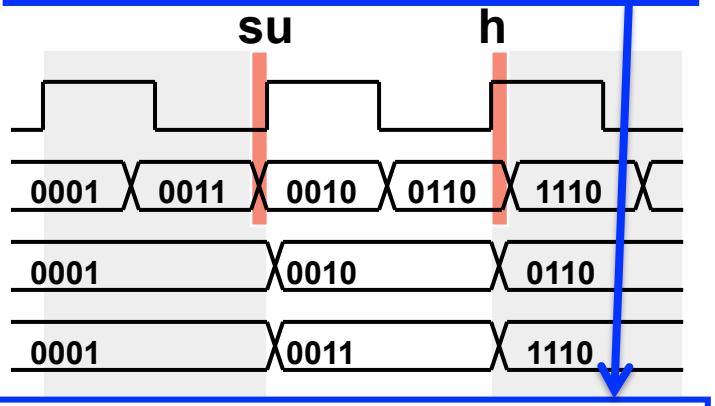
PHY CDC Requirements
- **relative timing** for **all bits** must ensure bus is gray-coded **on arrival** at 1st FFs

only 1 bit ***can*** go **metastable** per **clk**



slow-to-fast (all codes transported)

- **no stability check** in each 2FF
- **no gray-code check** @ dest clk



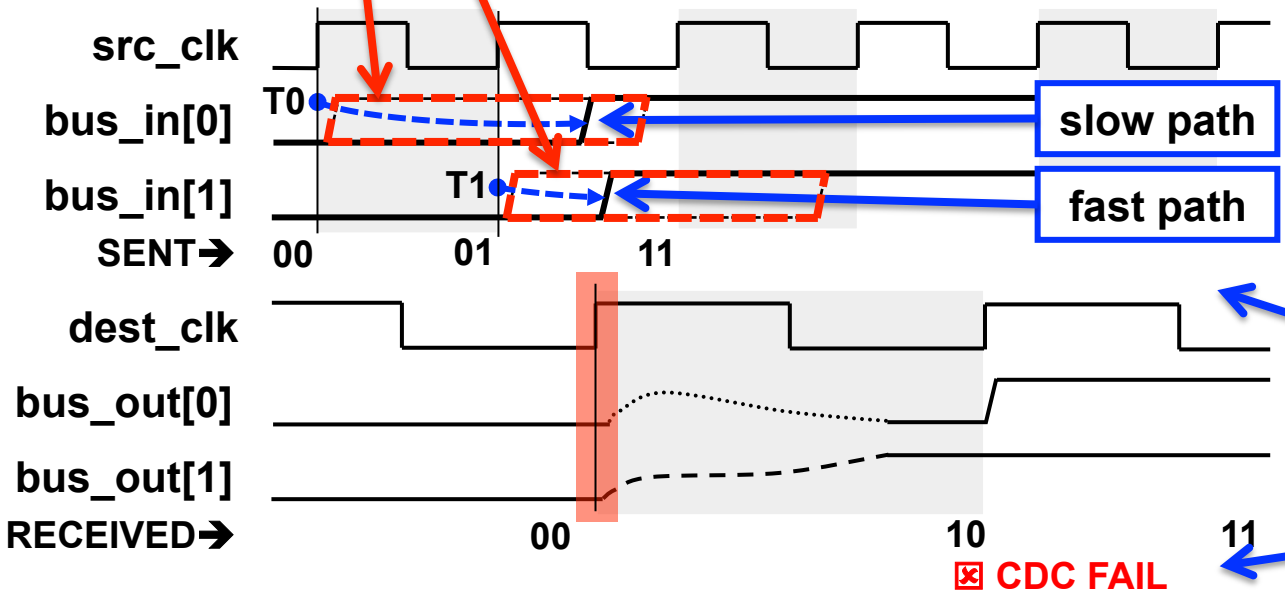
fast-to-slow (some codes dropped)

Failure: Path Variance

No absolute path delay requirement, but **relative timing** for all **parallel paths** must ensure **in-order** and **variance >*Tw***

Pragmatic: **delay** for all **paths** must be **less** than one **source** clock **period**

CDC bus **under-constrained**, e.g.
- marked as **false-path** (unconstrained)
- marked as **multi-cycle path** (either clk)
- using slow **destination clock** period
- **default constraints** (slow-speed scan)



Normal failure: **signal reorder** (visible in GLS)

Corner case: **close together** but in-order

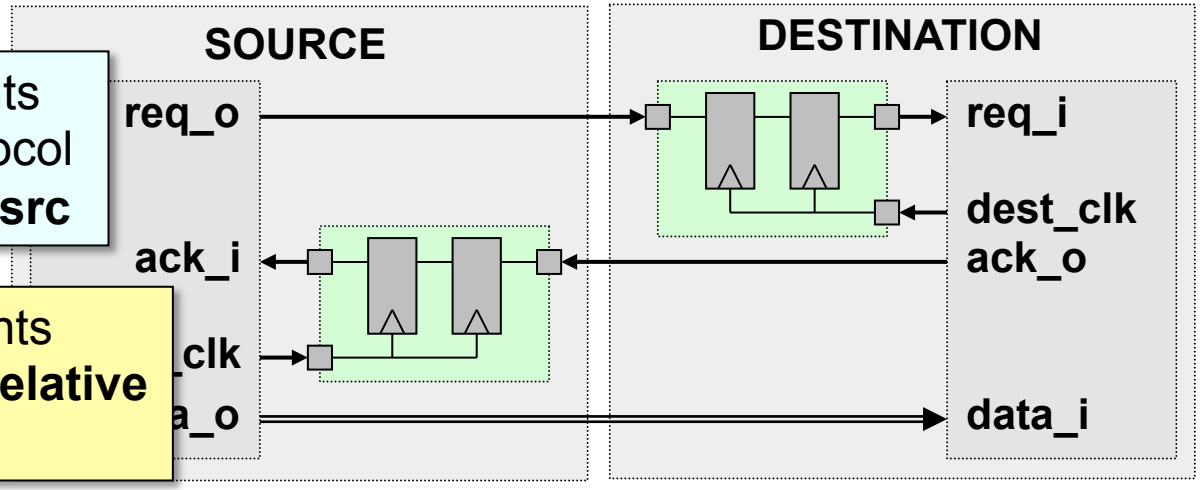
Received **value** was **not sent**

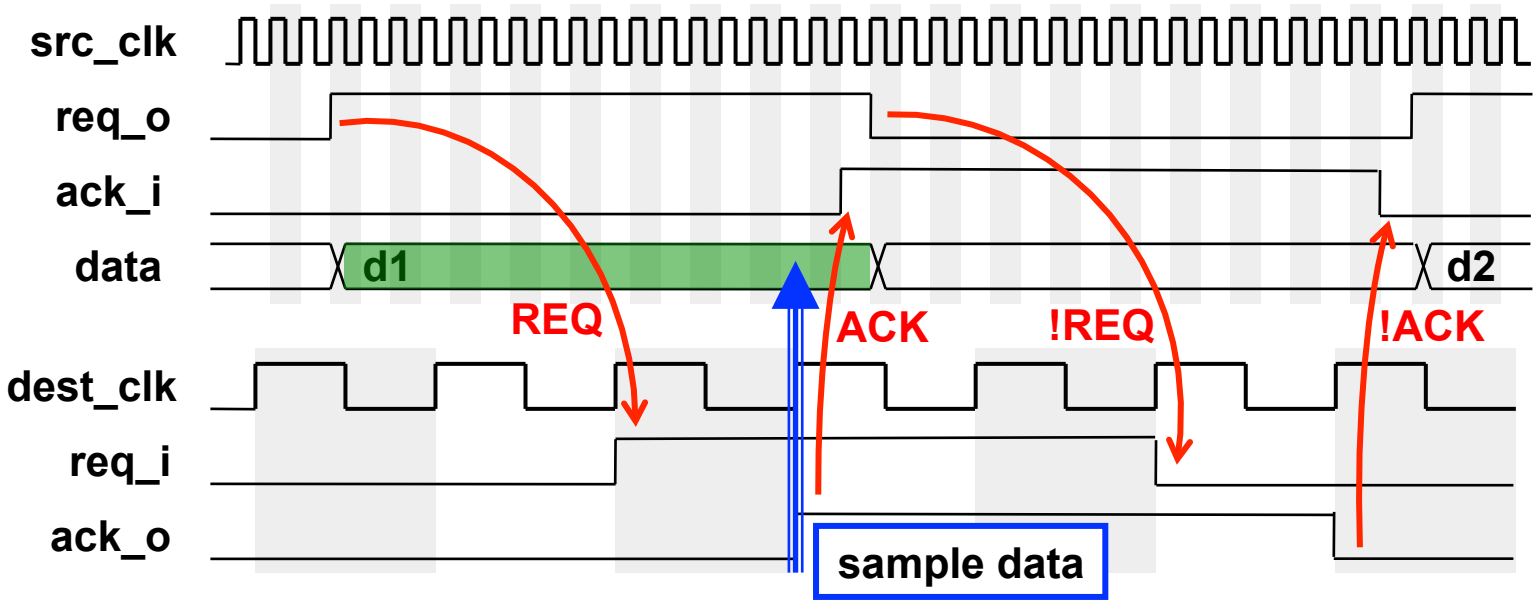
$$[(Tperiod_1 + T1) - (Tck\_skew_1 + T0)] > (Tsetup_2 + Thold_2)$$

Handshake Synchronizer

RTL CDC Requirements
- **full handshake** protocol
- **D stable** until **ack** in **src**

PHY CDC Requirements
- **max delay** on **data relative** to **req** and **dest_clk**



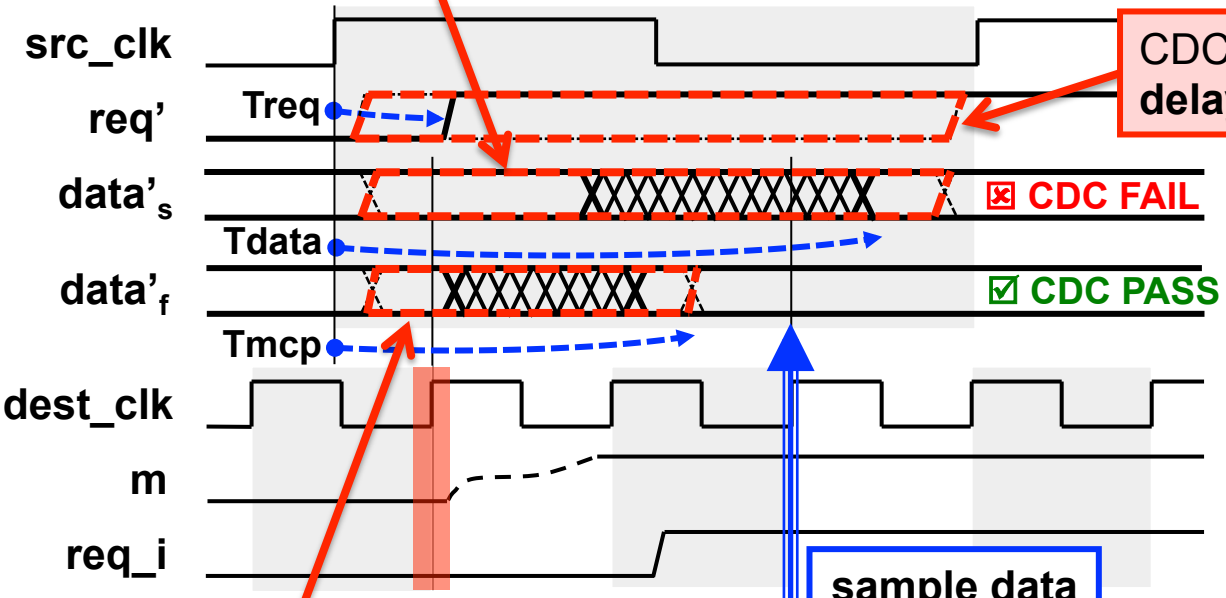


Failure: Slow Path

CDC **data under-constrained**, e.g.
- marked as **false-path** (unconstrained)
- marked as **multi-cycle path** (src_clk)
- using slow **source clock** period
- **default constraints** (slow-speed scan)

Data has **path delay** requirement, **relative** to req and destination clock

Pragmatic: **MCP** of **2 x dest_clk** periods (slight over-constrained if *Treq* > *Thold*$_2$)



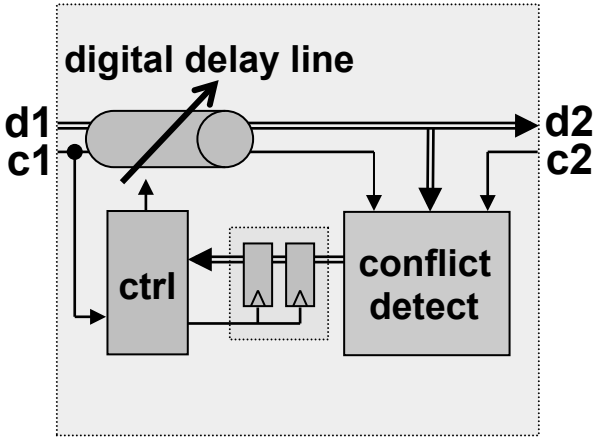
CDC **control no path delay** requirement

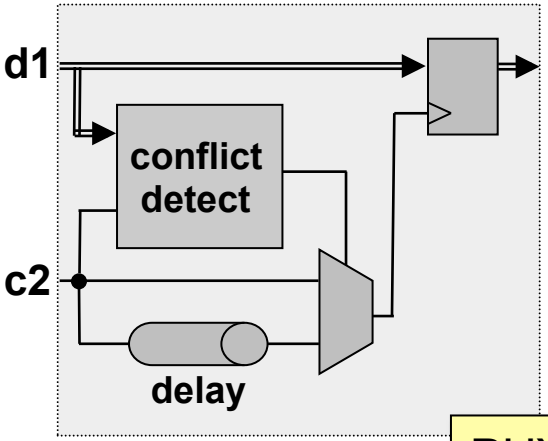
multi-cycle path relative to **dest_clk**

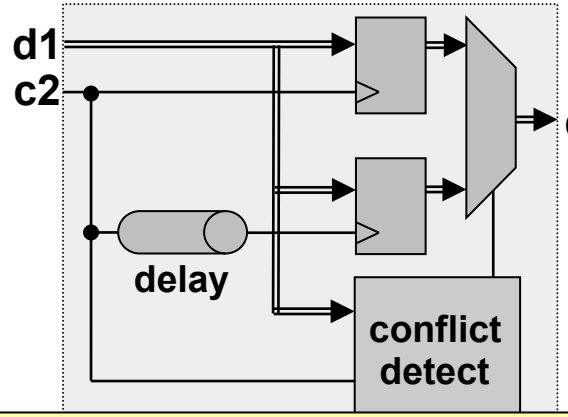
sample data (earliest)

$$(Tdata + Tck\_skew_1) < [Treq + (2 \times Tperiod_2) - Thold_2)]$$

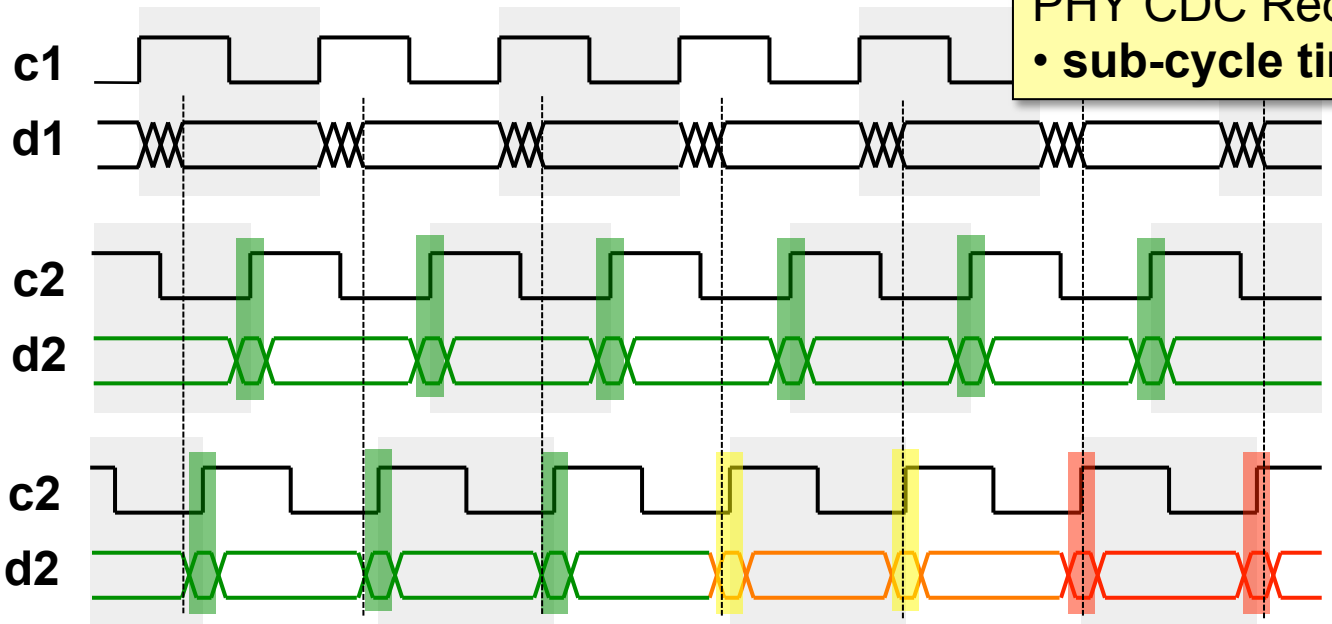
Phase-Detect Synchronizers







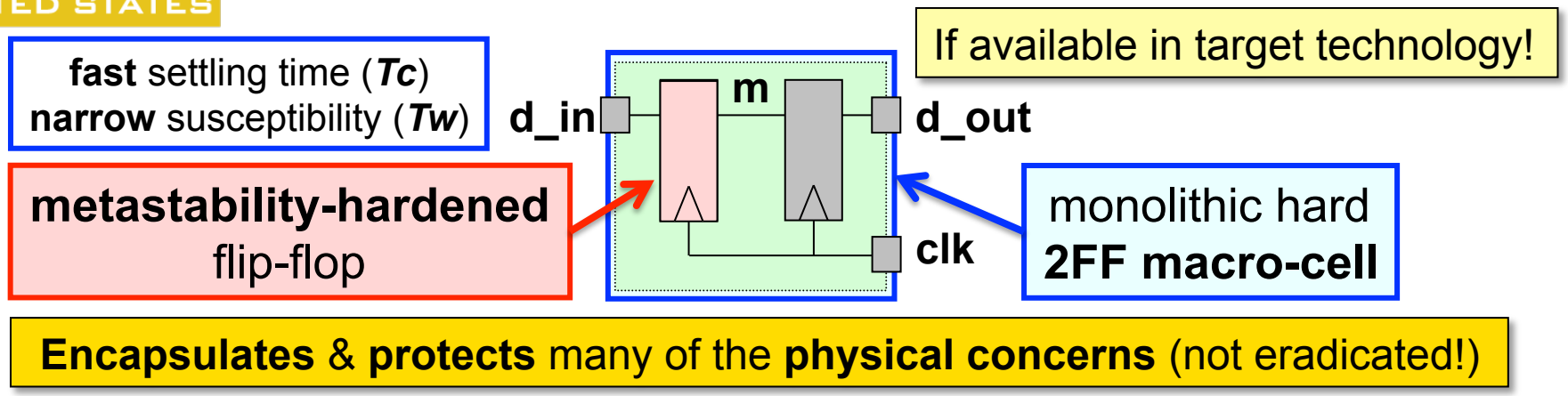
PHY CDC Requirements
- **sub-cycle timing** on **CDC data**



Mesochronous
(phase offset)

Plesiochronous
(phase changes)

Pragmatic Solutions



- **Synthesize** to **meta-hard** FF or (better) 2FF **macro-cell**
  - hard to map all RTL to desired circuits (e.g. no reset, no scan)
  - manageable with internal blocks, difficult with third-party IP
- **Instantiate meta-hard** FF or 2FF **macro-cell** into **RTL**
  - compromises portability and flexibility of the RTL (RTL becomes technology and frequency dependent)
  - manageable for internal designs and technology derivatives
  - inappropriate or impossible if using or supplying third-party IP

SVA Timing Checks

- **SVA** allows ***time*** and ***EventExpression*** formal arguments
- Actual arguments are supplied by **assert property** statement

```
property p_max_time(start, stop, duration);
  time start_time;
  @(start)
    (1,start_time = $time) |=>
  @(stop)
    (($time - start_time) <= duration);
endproperty
```

argument used as **event expression**

argument used as **time variable**

```
a_meta_sub_cycle: assert property (p_max_time(posedge clk, m, 300ps));
```

maximum **delay** from **posedge clk** to any **change** on **m** must be less than **300ps**

- Use **assertions** for both **RTL** and **gate-level**

Provides good **safety net** for validating **closure** on some **timing**-based **intent** ...

... but **be aware** that assertion **binding** to **optimized netlist** can be **non-trivial!**

Tools & Methodology

- **Gate-level CDC** analysis
  - some formal CDC analysis tools can handle GL complexity
  - add structural checks, clock-tree aware, reuse RTL intent
  - complement, but do not eradicate CDC-aware STA
- **Constraints management**
  - evolution and refinement of constraints is major issue
  - especially with multiple tool vendors in the flow
  - tools emerging to manage & validate equivalence of constraints
- **Multi-discipline** CDC **reviews**
  - recognize that CDC is not just an RTL problem...
  - review CDC functional operation and synchronizer physical implementation with a multi-discipline multi-talented team!

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Conclusion

- Presented an **overview** of the **problem**
  - RTL verification of CDC is necessary but not sufficient
  - additional requirements need to be understood front & back-end
- Illustrated **detailed hazards** for some common synchronizers
  - intra-domain operation within synchronizers
  - inter-domain CDC requirements and relationships
- Discussed some **pragmatic solutions** & tool advances
  - anything which closes the gap is good!

Primary **goal:** raise **multi-discipline CDC awareness**

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