

# DVCon<sup>2012</sup>

Design & Verification Conference & Exhibition

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## From Spec to Verification Closure:

A case study of applying UVM-MS for first pass success to a complex MS-SoC design

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# Why apply metrics Driven verification (MDV) to Analog?

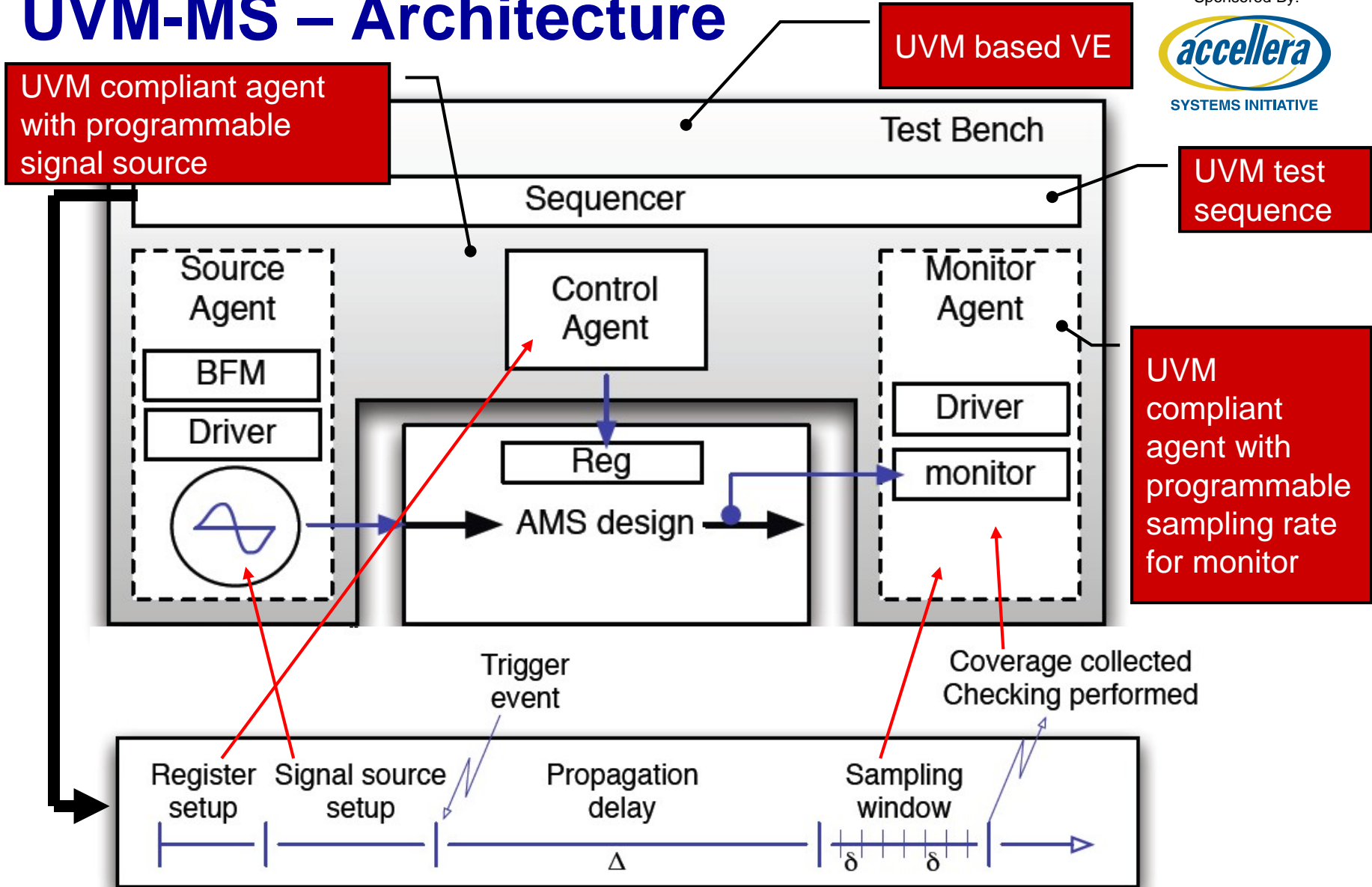
- MS Verification Challenges growing exponentially
  - Digital IP:  $\leftrightarrow$  Interface with real world analog in nature
  - Analog IP:  $\leftrightarrow$  Complex digital control – Calibration, Low-Power, Numerous operating modes
- Traditional methods manual and inefficient
  - Static in nature, little interaction between digital & analog
  - Manual and limited throughput & scalability
  - Fuzzy signoff metrics
- Existing Approaches based on simple black-box models of analog inadequate. How to automate, verify & measure:
  - Complex interaction between digital & analog
  - Complex dependencies – feedback loops
- Evolution: Augment traditional Analog Verification with MDV



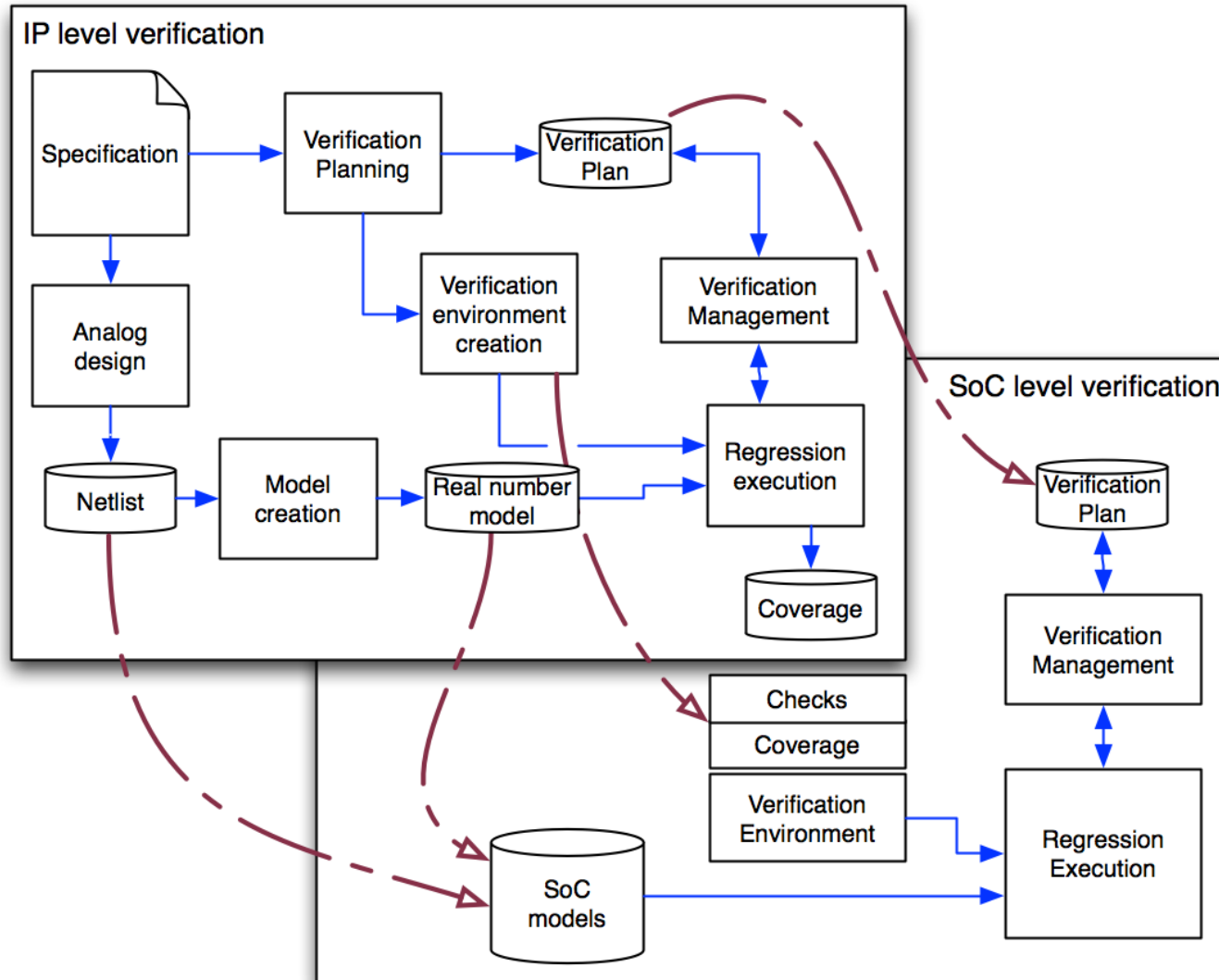
# How to apply MDV to Analog?

- Extend UVM concepts to cover M/S: UVM-MS
  - Analog uVC
  - Sequences for Analog
  - Analog Coverage
  - Analog Checks
- Make UVM aware of analog concepts:
  - Sampling rate
  - Sampling window
  - Trigger event
- Verification Planning
  - Executable vPlan for Analog
  - Analog checks, metrics mapped to the vPlan
  - Analog metrics annotated back to the vPlan

# UVM-MS – Architecture

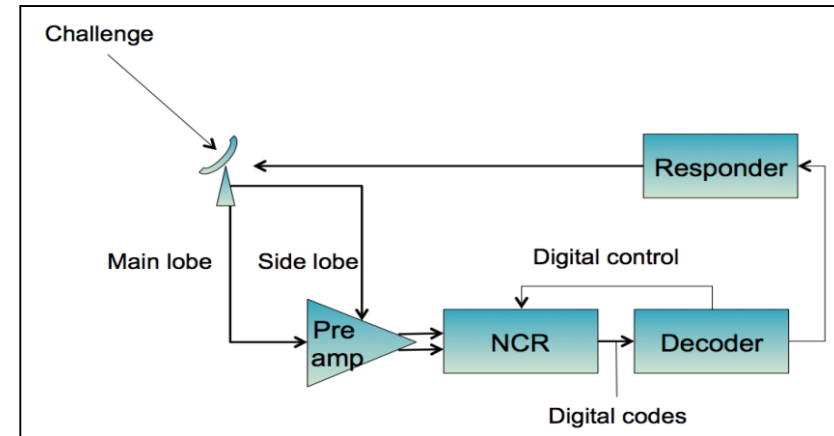


# Applying UVM-MS at IP & SoC Level



# DUT – Noise Cancelling Receiver

- Main lobe signal carries data + noise
  - Carrier signal is 1-3 GHz
  - Noise modeled by 1-100 KHz small signal
  - Data is short bursts of 30-40 KHz small signal
- Side lobe signal carries noise only
- Digital controls
  - Gain setting for each channel
    - Table of expected gains
  - Side lobe select
    - In “off” setting, mixer takes locally generated frequency (“LO”) - no noise cancellation
    - In “on” setting, mixing side lobe eliminates noise
- Main output checking
  - Lookup table converting from data frequency to voltage

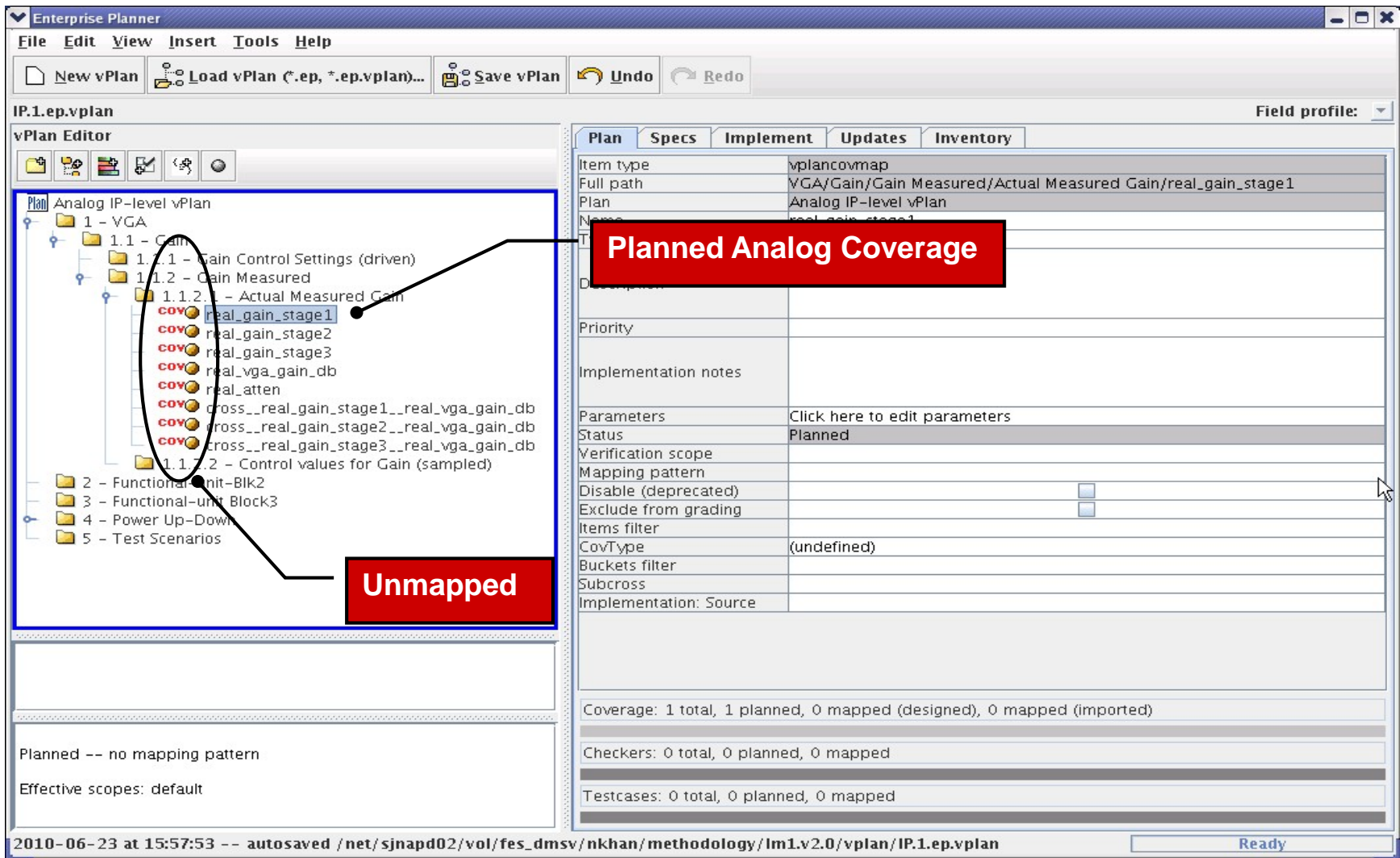


**Disclaimer:** *This is a made-up design for training purposes only*

# Creating Executable Verification Plan for Analog

The screenshot displays the vPlan Editor interface. On the left, a tree view shows the structure of the verification plan, including sections for LP Filter performance and Filter corner. A red callout box labeled "Analog Features of interest for Verification" points to the "1.1 - Filter corner" section. On the right, a "Spec manager" window is open, displaying a Bode plot for "Spec\_sample.pdf". A red callout box labeled "Analog Spec" points to the plot. The Bode plot shows Gain in dB versus Frequency in Hz, with a roll-off frequency marked at 1.1: 40 and a slope of -20 dB/decade. The plot is divided into Passband and Stopband regions.

# Verification Plan - Planned Analog Coverage



The screenshot shows the Enterprise Planner vPlan Editor interface. On the left, a tree view displays the hierarchy of analog coverage items under 'Analog IP-level vPlan'. A red box labeled 'Unmapped' points to the 'real\_gain\_stage1' item, which is currently unmapped. A red box labeled 'Planned Analog Coverage' points to the 'real\_gain\_stage1' item in the tree view, indicating its planned status.

The right pane shows the properties for the selected item, 'real\_gain\_stage1'. The 'Status' is 'Planned'. The 'Verification scope' is 'VGA/Gain/Gain Measured/Actual Measured Gain/real\_gain\_stage1'. The 'Implementation: Source' is 'vplancovmap'. The 'Coverage' summary at the bottom indicates: Coverage: 1 total, 1 planned, 0 mapped (designed), 0 mapped (imported). Checkers: 0 total, 0 planned, 0 mapped. Testcases: 0 total, 0 planned, 0 mapped.

Item type	vplancovmap
Full path	VGA/Gain/Gain Measured/Actual Measured Gain/real_gain_stage1
Plan	Analog IP-level vPlan
Name	real_gain_stage1
Description	
Priority	
Implementation notes	
Parameters	Click here to edit parameters
Status	Planned
Verification scope	VGA/Gain/Gain Measured/Actual Measured Gain/real_gain_stage1
Mapping pattern	
Disable (deprecated)	<input type="checkbox"/>
Exclude from grading	<input type="checkbox"/>
Items filter	
CovType	(undefined)
Buckets filter	
Subcross	
Implementation: Source	vplancovmap

Coverage: 1 total, 1 planned, 0 mapped (designed), 0 mapped (imported)

Checkers: 0 total, 0 planned, 0 mapped

Testcases: 0 total, 0 planned, 0 mapped

2010-06-23 at 15:57:53 -- autosaved /net/sjnapd02/vol/fes\_dmsv/nkhan/methodology/lm1.v2.0/vplan/IP.1.ep.vplan



# Closing the loop – Map Collected to Planned Coverage in vPlan

**Coverage section in vPlan**

**Raw, Unmapped coverage data**

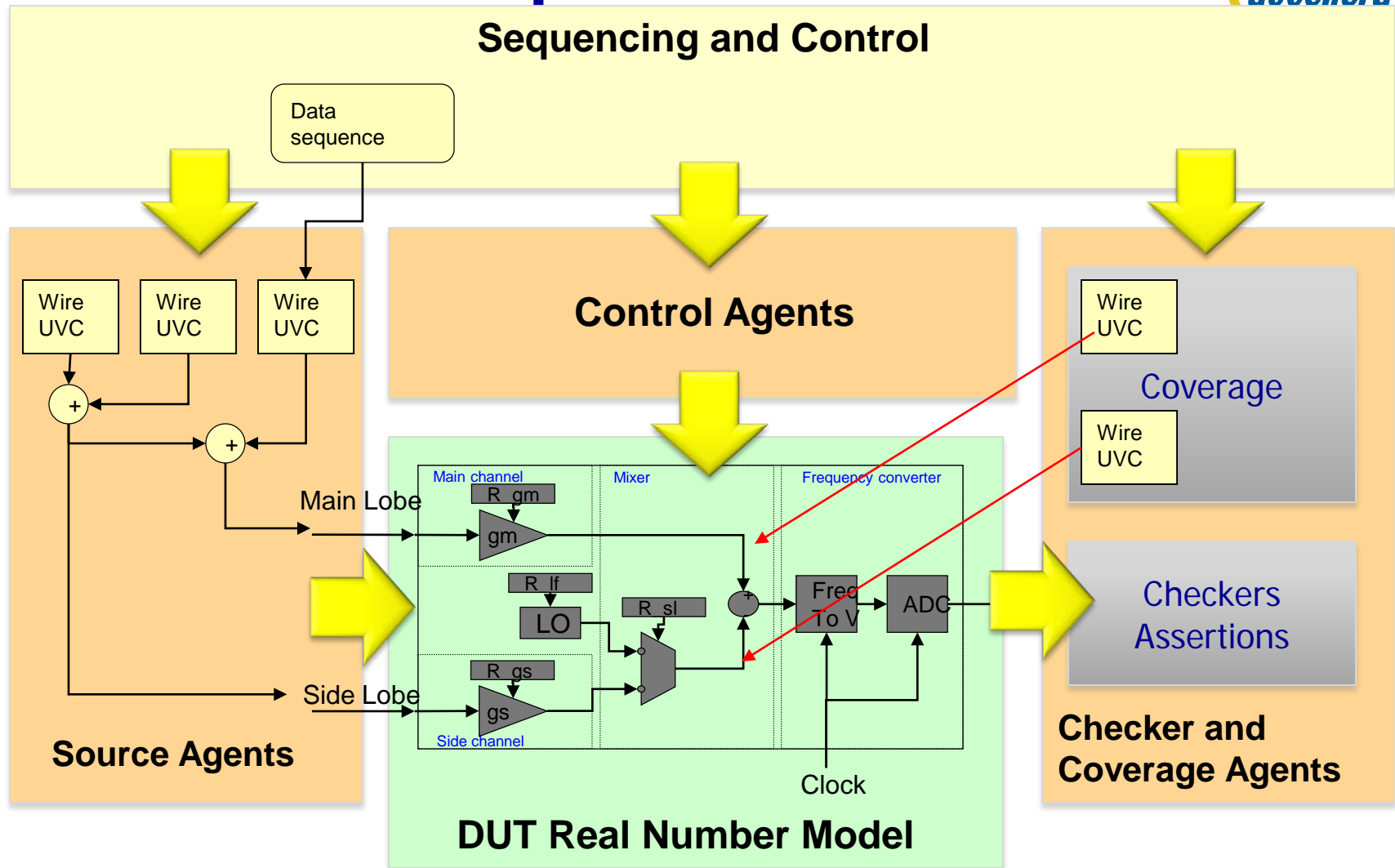
**Map to vPlan**

**Mapped coverage data**

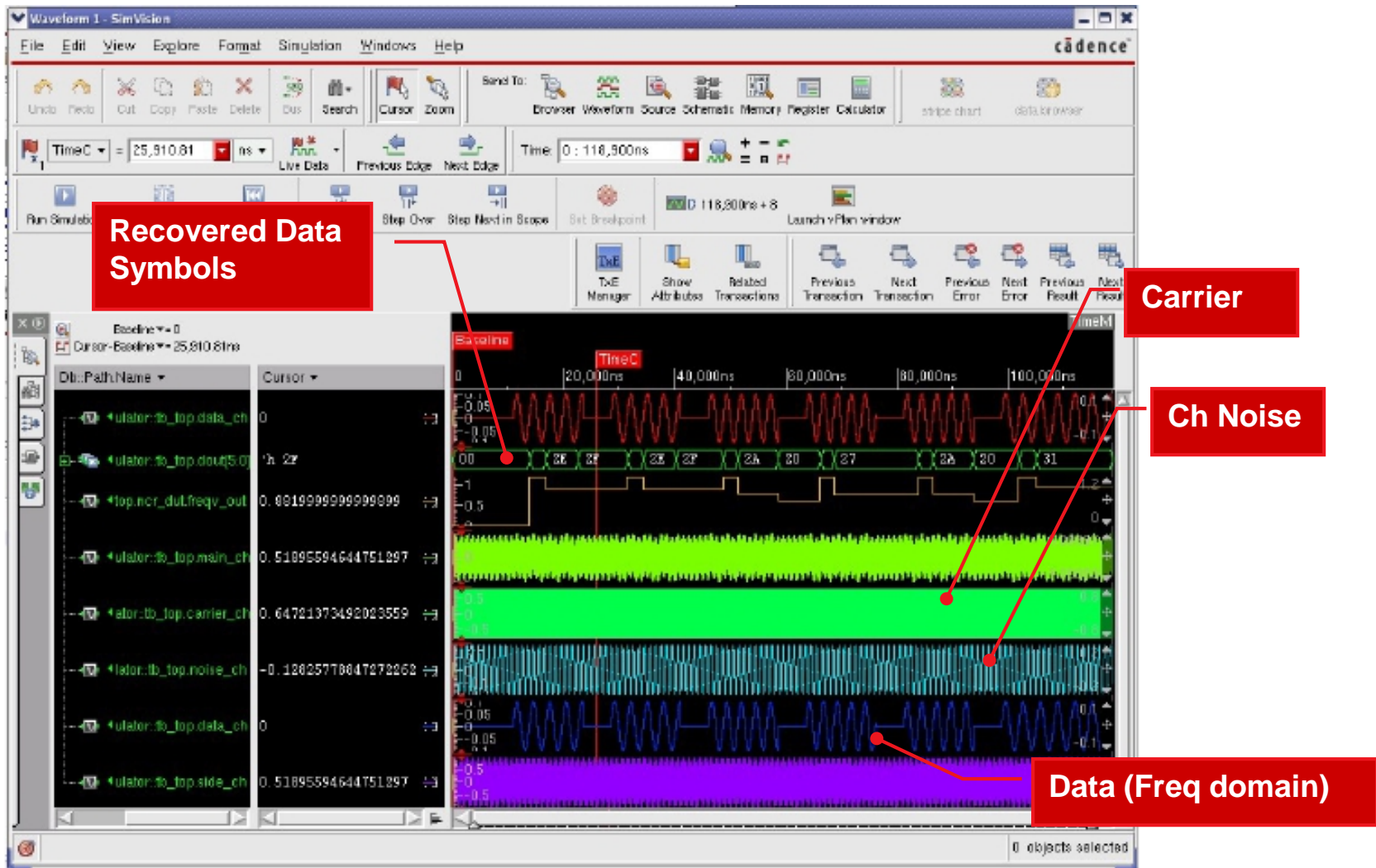
**Unmapped Coverage Data**

Mapping pattern: (e.type)gain\_mon\_u.gain\_sample.real\_gain\_stage1  
Effective scopes: (Functional scalar coverage) real\_gain\_stage1

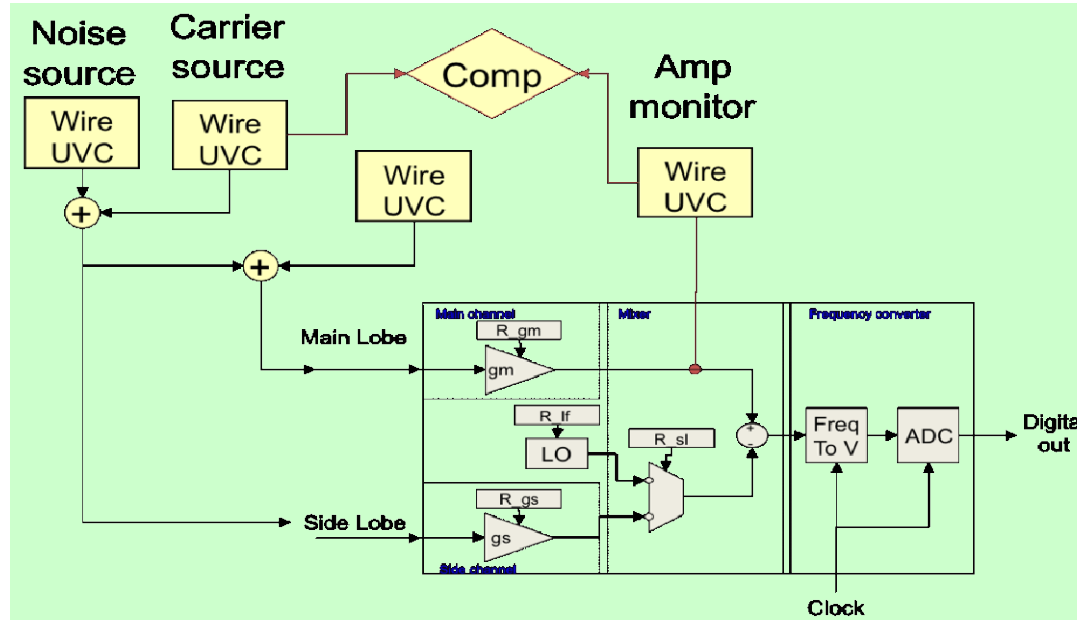
# Simulation Setup



# DUT Operation: Data Symbols Extracted from Noisy Signal

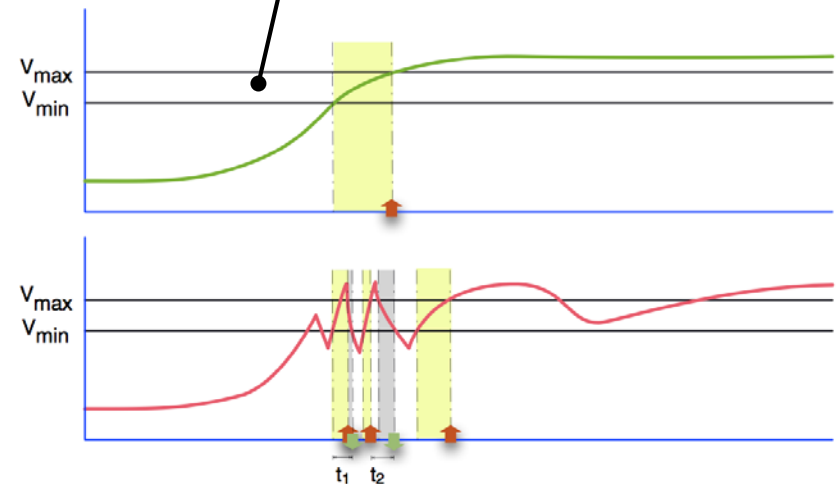
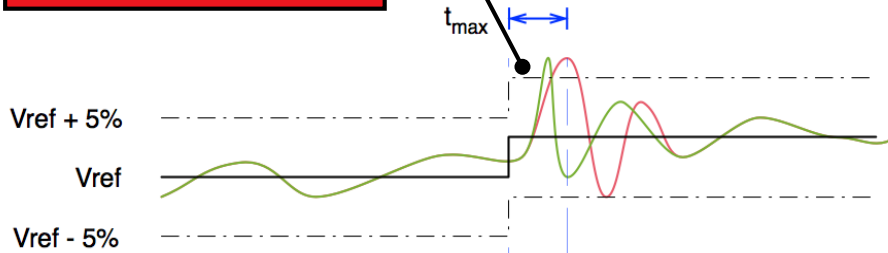


# Analog Checkers

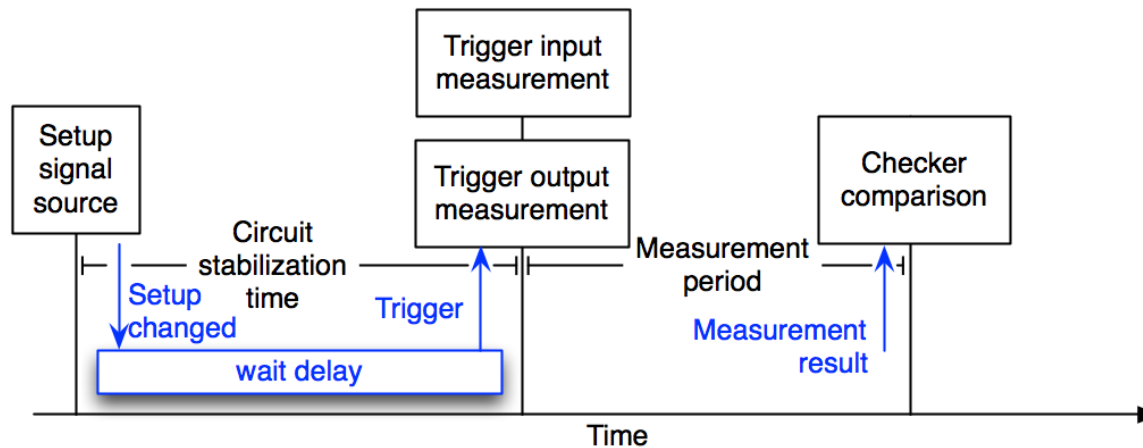
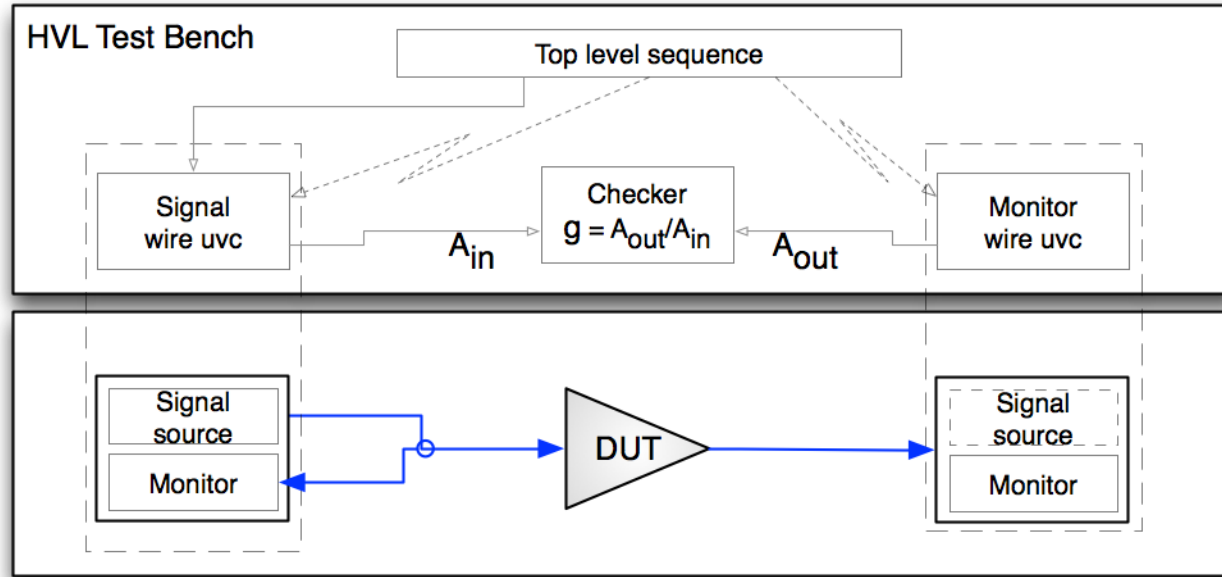


Check: threshold crossing [Vmax, Vmin]

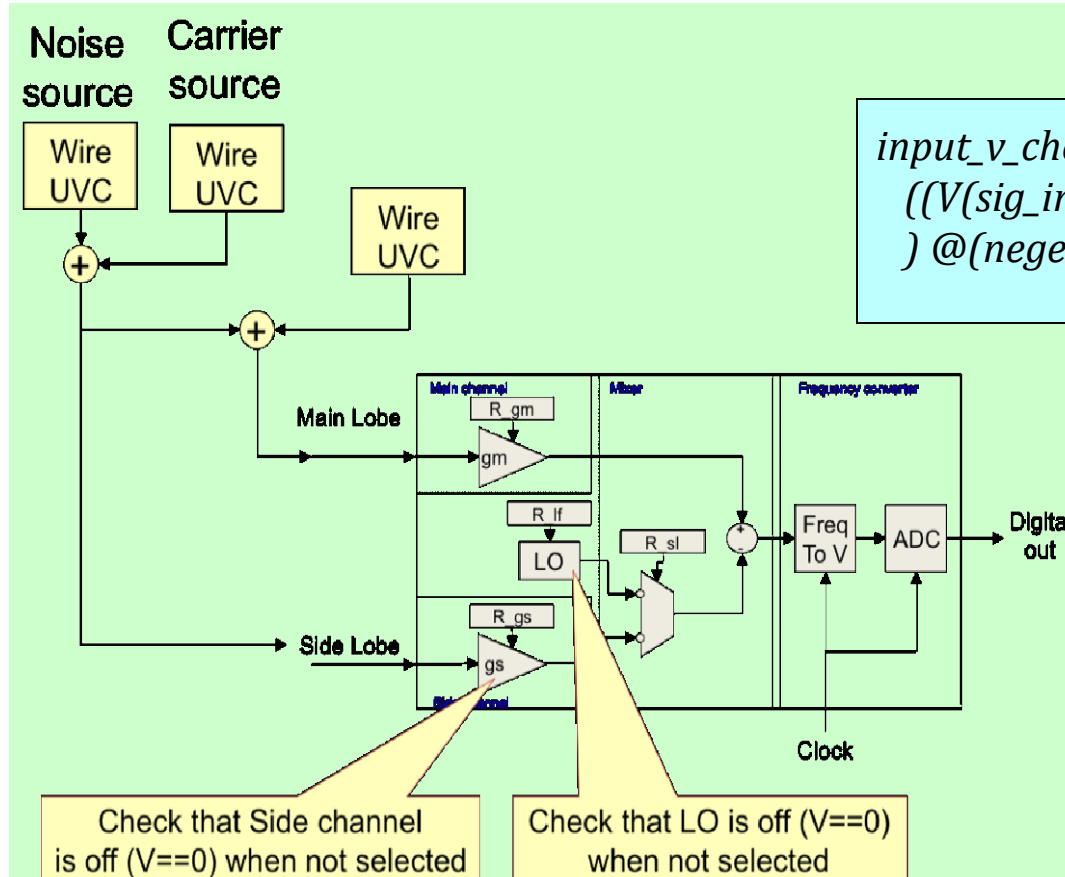
Threshold crossing a Vref



# Triggering Checks



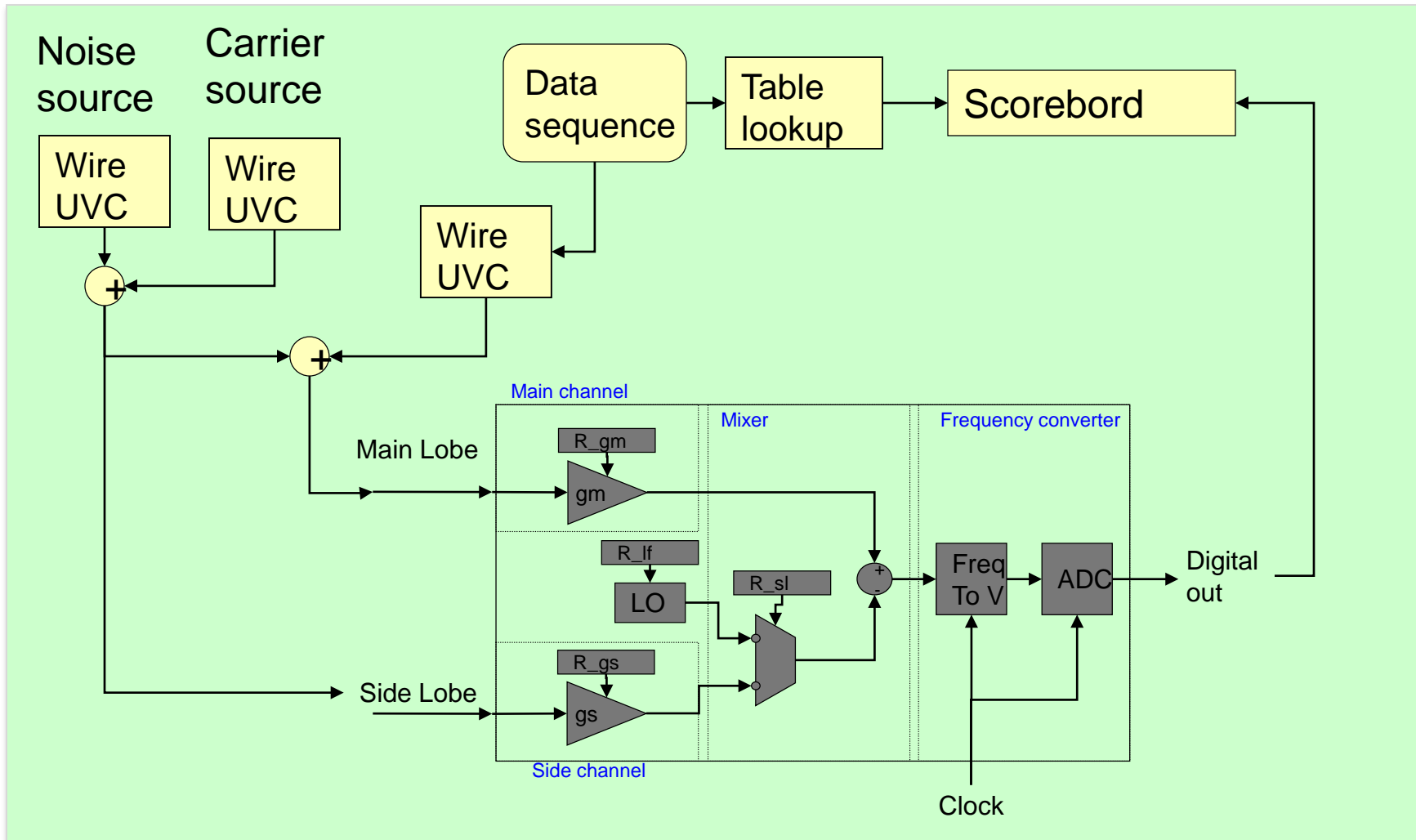
# Assertion Based Checkers



```
input_v_check: assert always
  ((V(sig_in)>0.5m) &&(V(sig_in)<10m)
  ) @(negedge reset);
```

```
Check1_Stage2: assert (always
  ({reg_side_sel == 1} | => {V(side_out) == 0.0}
  ) @(posedge ctrl_write_clk) );
```

# End-to-End Checks using Scoreboard



# Achieving Verification Closure – Analyzing Analog Coverage

**Coverage column**

Reports the percentage of coverage points that have filled, assertions that have completed successfully

**Check Column**

Reports the percentage of failed and passed

**Individual Coverage**

Reports individual coverage points that have filled

The screenshot shows a verification tool interface with a coverage tree on the left and an 'Input symbols' table on the right. Red arrows point from text boxes to specific elements in the interface.

**Coverage Tree:**

- 2 - automatic\_top (100% coverage)
  - 2.1 - NCRReceiver (100% coverage)
    - 2.1.1 - Gain accuracy (100% coverage)
      - Gain accuracy check (100% Passed)
    - 2.1.2 - Modulation detection (100% coverage)
      - Input symbols (90% coverage)
      - Symbol match scoreboard (100% Passed)
      - Symbol detect timing (N/A)
      - scoreboard\_empty\_at\_end (100% Passed)
    - 2.1.3 - Test mode (N/A)
    - 2.1.4 - Control regs (46% coverage)
    - 2.1.5 - Input signal (28% coverage)
      - 2.1.5.1 - Carrier (12% coverage)
      - 2.1.5.2 - Noise (43% coverage)

**Input symbols Table:**

Grade	Name	Runs	Hits	At Least	Hits / At Least
1%	DC	0	0	1	
1%	Top	0	0	1	
100%	A	1	11	1	
100%	B	1	9	1	
100%	C	1	13	1	
100%	D	1	7	1	
100%	E	1	7	1	
100%	F	1	6	1	
1%	High	0	0	1	
N/A	others	0	0	0	

**Functional Simple Item Details:**

Name: sys.tb\_env\_data\_src\_agent.monitor.cov\_dms\_mawire\_measureme  
Spec text: The signal may be amplitude modulated by frequency 200-4000Hz using that measured digital code value. The





# Conclusion

## Applying advanced verification concepts from digital verification realm very helpful for Analog IP verification

- UVM based
  - Reconfigurable and reusable at both IP & SOC level
- Executable verification plan
  - Know up front what's needs to be verified.
  - Identify Missing specs
  - Prioritize and manage resources and focus where needed
- Analog coverage
  - Provides an impartial metric of design quality
  - Highlights what was verified and more importantly what was not!
- Automated checks for Analog is a must have
  - Too many problems missed by traditional approach of eyeballing...
- Verification environment reusable at many levels
  - Tradeoff speed vs. accuracy: DUT (Verilog-AMS, wreal-model, Spice)

**High impact on Quality, Predictability and Productivity**