From Spec to Verification Closure:
A case study of applying UVM-MS for first pass success to a complex MS-SoC design

by
Neyaz Khan
Senior PMTS
Maxim Integrated Products

by
Yaron Kashai
Distinguished Engineer
Cadence Design Systems
Why apply metrics Driven verification (MDV) to Analog?

- MS Verification Challenges growing exponentially
  - Digital IP: $\leftrightarrow$ Interface with real world analog in nature
  - Analog IP: $\leftrightarrow$ Complex digital control – Calibration, Low-Power, Numerous operating modes

- Traditional methods manual and inefficient
  - Static in nature, little interaction between digital & analog
  - Manual and limited throughput & scalability
  - Fuzzy signoff metrics

- Existing Approaches based on simple black-box models of analog inadequate. How to automate, verify & measure:
  - Complex interaction between digital & analog
  - Complex dependencies – feedback loops

- Evolution: Augment traditional Analog Verification with MDV
How to apply MDV to Analog?

• Extend UVM concepts to cover M/S: UVM-MS
  - Analog uVC
  - Sequences for Analog
  - Analog Coverage
  - Analog Checks

• Make UVM aware of analog concepts:
  - Sampling rate
  - Sampling window
  - Trigger event

• Verification Planning
  - Executable vPlan for Analog
  - Analog checks, metrics mapped to the vPlan
  - Analog metrics annotated back to the vPlan
UVM-MS – Architecture

- UVM compliant agent with programmable signal source
- UVM based VE
- UVM compliant agent with programmable sampling rate for monitor
- UVM test sequence
- Source Agent: BFM, Driver
- Control Agent
- Monitor Agent: Driver, monitor
- AMS design
- Trigger event
- Coverage collected Checking performed
- Register setup
- Signal source setup
- Propagation delay
- Sampling window
- \( \Delta \)
Applying UVM-MS at IP & SoC Level

Neyaz Khan, Maxim Integrated Products
DUT - Noise Cancelling Receiver

- Main lobe signal carries data + noise
  - Carrier signal is 1-3 GHz
  - Noise modeled by 1-100 KHz small signal
  - Data is short bursts of 30-40 KHz small signal
- Side lobe signal carries noise only
- Digital controls
  - Gain setting for each channel
    - Table of expected gains
  - Side lobe select
    - In “off” setting, mixer takes locally generated frequency (“LO”) - no noise cancellation
    - In “on” setting, mixing side lobe eliminates noise
- Main output checking
  - Lookup table converting from data frequency to voltage

Disclaimer: This is a made-up design for training purposes only
Creating Executable Verification Plan for Analog

Analog Features of interest for Verification

Analog Spec

Neyaz Khan, Maxim Integrated Products
Verification Plan - Planned Analog Coverage

Planned Analog Coverage

Unmapped
Closing the loop - Map Collected to Planned Coverage in vPlan

Neyaz Khan, Maxim Integrated Products
Simulation Setup

Sequencing and Control

Control Agents

Source Agents

DUT Real Number Model

Coverage

Checkers

Data sequence

Main Lobe

Side Lobe

Main channel

Mixer

Frequency converter

Clock

R \_gm

R \_gs

R \_sl

R \_lf

R \_if

LO

ADC

Neyaz Khan, Maxim Integrated Products
DUT Operation: Data Symbols
Extracted from Noisy Signal

Recovered Data Symbols

Carrier

Ch Noise

Data (Freq domain)
Analog Checkers

Check: threshold crossing \([V_{\text{max}}, V_{\text{min}}]\)

Threshold crossing a \(V_{\text{ref}}\)

Neyaz Khan, Maxim Integrated Products
Triggering Checks

HVL Test Bench

Top level sequence

Signal wire uvc

Checker

$g = \frac{A_{out}}{A_{in}}$

$A_{out}$

Monitor wire uvc

Signal source

Monitor

DUT

Signal source

Monitor

Trigger input measurement

Trigger output measurement

Checker comparison

Setup signal source

Circuit stabilization time

Trigger

Setup changed

wait delay

Time

Measurement period

Measurement result

Neyaz Khan, Maxim Integrated Products
Assertion Based Checkers

Check1_Stage2: assert (always
  ({reg_side_sel == 1} |=> {V(side_out) == 0.0}
) @(posedge ctrl_write_clk) );

input_v_check: assert always
  ((V(sig_in)>0.5m) &&(V(sig_in)<10m)
) @(negedge reset);
End-to-End Checks using Scoreboard

Neyaz Khan, Maxim Integrated Products
Achieving Verification Closure - Analyzing Analog Coverage

Coverage column
Reports the percentage of coverage points that have filled, assertions that have completed successfully

Check Column
Reports the percentage of failed and passed

Individual Coverage
Reports individual coverage points that have filled
Conclusion

Applying advanced verification concepts from digital verification realm very helpful for Analog IP verification

- UVM based
  - Reconfigurable and reusable at both IP & SOC level
- Executable verification plan
  - Know up front what’s needs to be verified.
  - Identify Missing specs
  - Prioritize and manage resources and focus where needed
- Analog coverage
  - Provides an impartial metric of design quality
  - Highlights what was verified and more importantly what was not!
- Automated checks for Analog is a must have
  - Too many problems missed by traditional approach of eyeballing…
- Verification environment reusable at many levels
  - Tradeoff speed vs. accuracy: DUT (Verilog-AMS, wreal-model, Spice)

High impact on Quality, Predictability and Productivity

Neyaz Khan, Maxim Integrated Products