Formal For Adjacencies
Expanding the Scope of Formal Verification

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AGENDA

• Motivation
• Formal for Post-Silicon Debugs
• Formal beyond Equivalence
  – Hierarchical Equivalence
  – Schmoo Formal
• Formal Connectivity
• Results
• Conclusion
Motivation

• Bug escapes are expensive
Way-out??

• Embrace the best of technologies
  (FV wherever possible)
  – Pre-Si Formal – Bring Formal Mainstream
  – Post-Si Formal

• Explore Adjacent areas for FV
  – New applications of Sequential Equivalence
  – Connectivity
  – Performance??? (Stay tuned for our next paper)
Post Silicon Debugs

Theory1
- Assertion on signal A

Theory2
- Assertion on signal X

LogicX
- Assertion on signal y
Formal for Post Silicon
Formal saving Post Silicon effort

REDUCTION ACHIEVED IN VERIFICATION TIME
WITH FV METHODOLOGY

Post Silicon FV

Traditional DV  Formal method
Can formal be applied on Adjacencies?

We say, Why not?
Formal Equivalence @ chip ??

• Known application of Sequential Equivalence at the Unit level boundary: Timing fixes, clock gating, chicken bits
  • M AchuthaKiranKumar V, Aarti Gupta, Bindumadhava S S, "RTL2RTL Formal Equivalence: Boosting the Design Confidence"
    (Best paper @ DAC 2015)

• Can Equivalence be scaled up??

• Chip Level boundary: RTL-RTL Sequential Equivalence Checking ?
  – Derivative project, Intended partitions not effected
  – Simulation regression – multiple days
Formal Equivalence @ Chip Level

- Script dividing hierarchical partitions
- Sequential Equivalence
Chip level Equivalence savings

REDUCTION ACHIEVED IN VERIFICATION TIME WITH FV METHODOLOGY

Post Silicon FV
- Traditional DV: 80%
- Formal method: 20%

Hierarchical RTL - RTL
- Traditional DV: 94%
- Formal method: 6%

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SCHMOO FV

- Transactional Equivalence
  - RTL to generate the same output, for different streaming bandwidths
SCHMOO FV contd..,
Schmoo Formal Results

Reduction achieved in verification time with FV methodology:

- Post Silicon FV: 80% (Traditional DV), 20% (Formal method)
- Hierarchical RTL-RTL: 94% (Traditional DV), 6% (Formal method)
- Schmoo RTL-RTL: 84% (Traditional DV), 14% (Formal method)
Connectivity Verification beyond SOC?

- Simple Application applicable on various adjacencies
- Full Chip bring up
- Connecting checkers and trackers at FC
- Delivering sub system to SOCs
- Repeater addition model sanity
- ....many more
Practical application

• Start with a base and scale up the connections
• Use existing features and make formal indispensable
Consolidated Results

REDUCTION ACHIEVED IN VERIFICATION TIME WITH FV METHODOLOGY

<table>
<thead>
<tr>
<th>Category</th>
<th>Traditional DV</th>
<th>Formal method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Post Silicon FV</td>
<td>80%</td>
<td>20%</td>
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<tr>
<td>Hierarchical RTL -RTL</td>
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<tr>
<td>Connectivity Verification</td>
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<td>25%</td>
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</tbody>
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Conclusion

- Formal beyond traditional applications
- Expand Formal into adjacencies
- Proper application of Formal delivers high ROI
- List to keep expanding to the adjacencies
- Formal will keep expanding
- Formal to become mainstream eventually

( Liveness property !!!! )
Questions