Formal For Adjacencies
Expanding the Scope of Formal Verification

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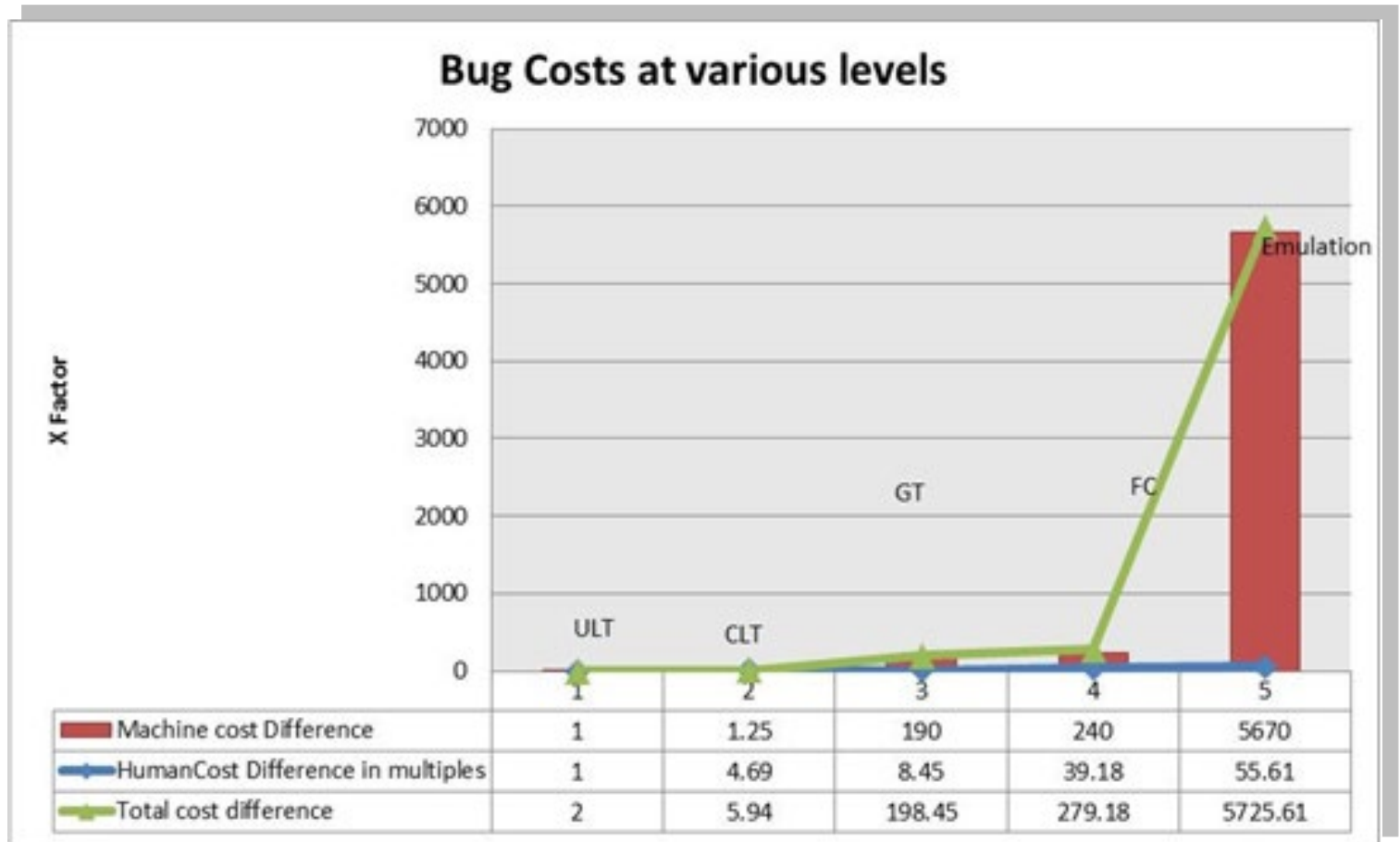**Vichal Verma**

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AGENDA

- Motivation

- Formal for Post-Silicon Debugs

- Formal beyond Equivalence
  - Hierarchical Equivalence
  - Schmoo Formal

- Formal Connectivity

- Results

- Conclusion

Motivation

- Bug escapes are expensive

Bug Costs at various levels

	ULT	CLT	GT	FC	Emulation
Machine cost Difference	1	1.25	190	240	5670
HumanCost Difference in multiples	1	4.69	8.45	39.18	55.61
Total cost difference	2	5.94	198.45	279.18	5725.61

Way-out??

- Embrace the best of technologies
   (FV wherever possible)
  - Pre-Si Formal – Bring Formal Mainstream
  - Post-Si Formal

- Explore Adjacent areas for FV
  - New applications of Sequential Equivalence
  - Connectivity
  - Performance??? (Stay tuned for our next paper)
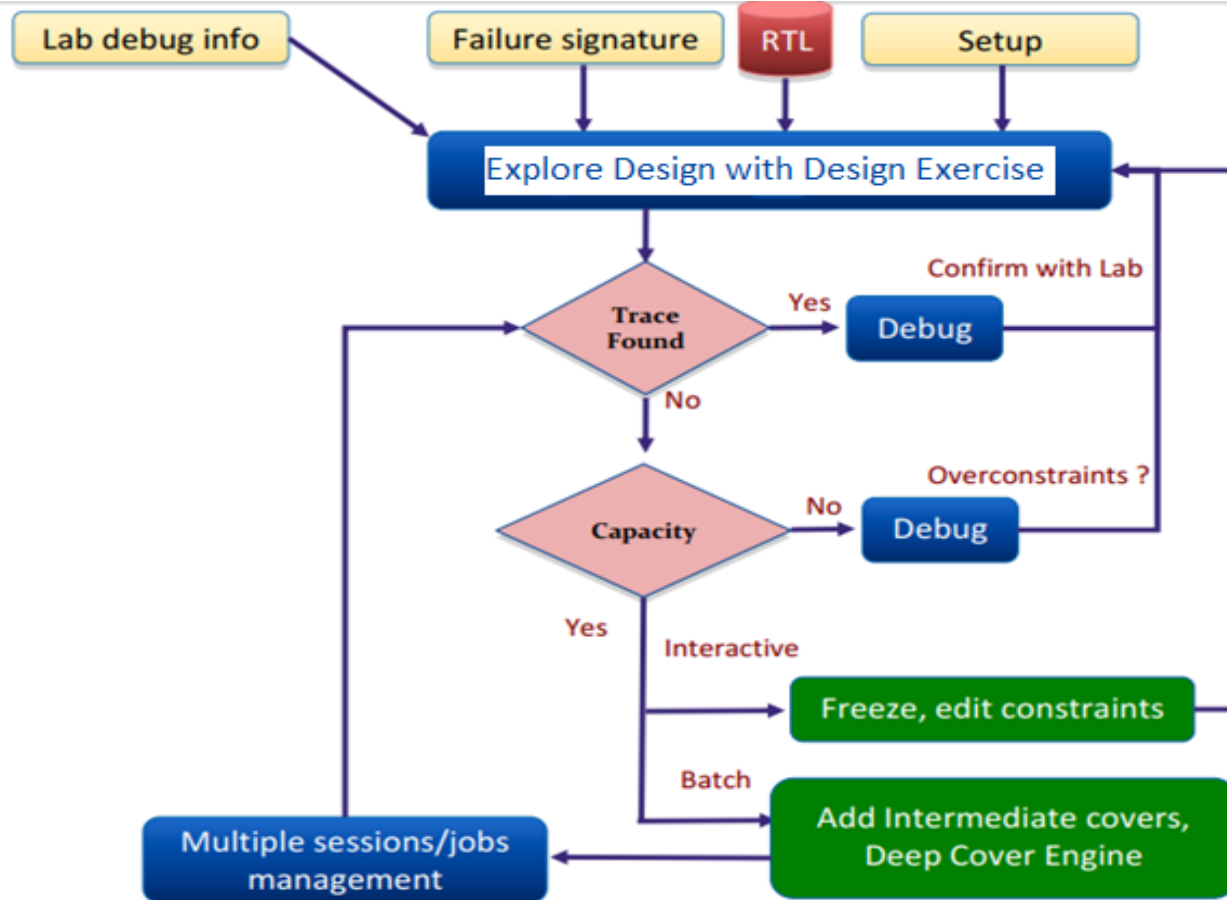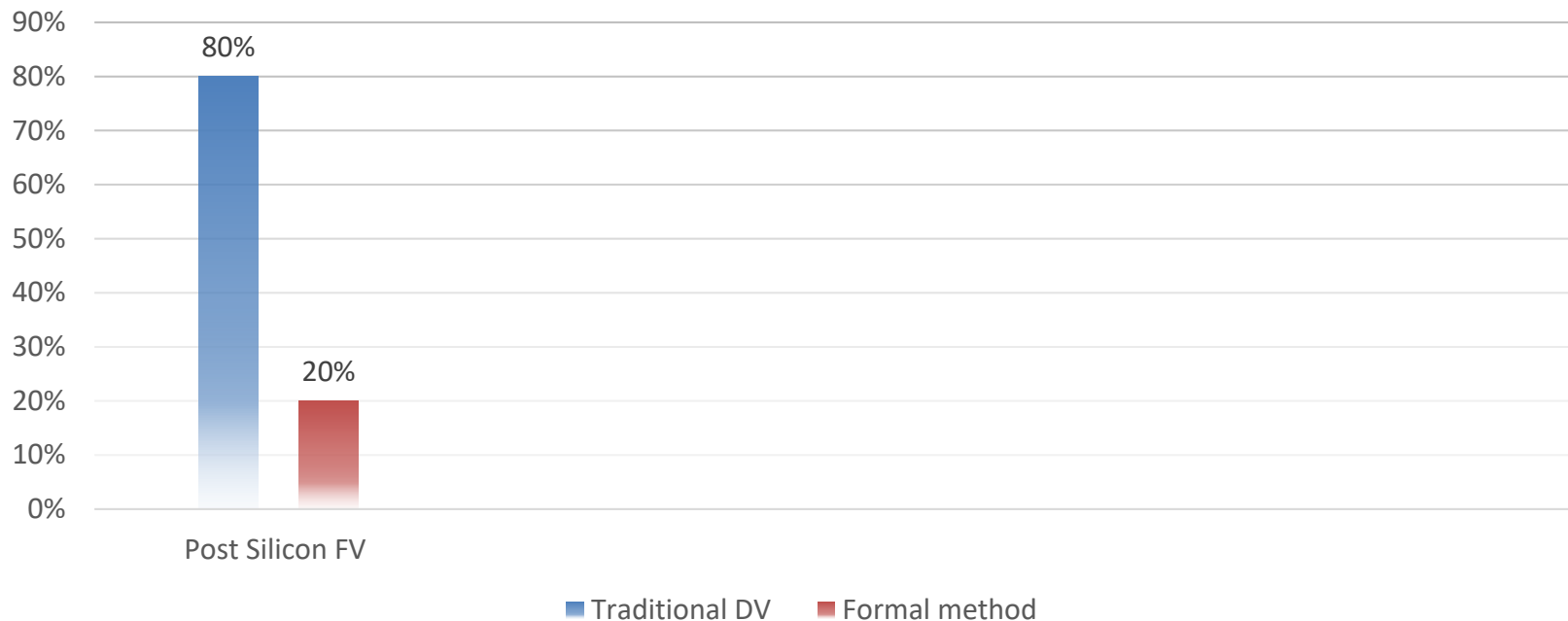
Post Silicon Debugs
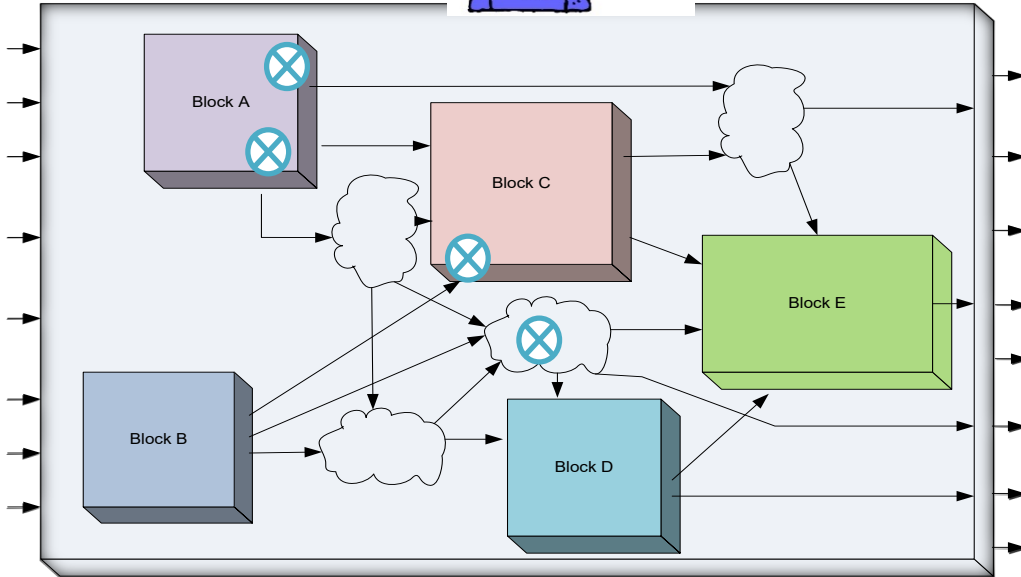
Formal for Post Silicon

Formal saving Post Silicon effort

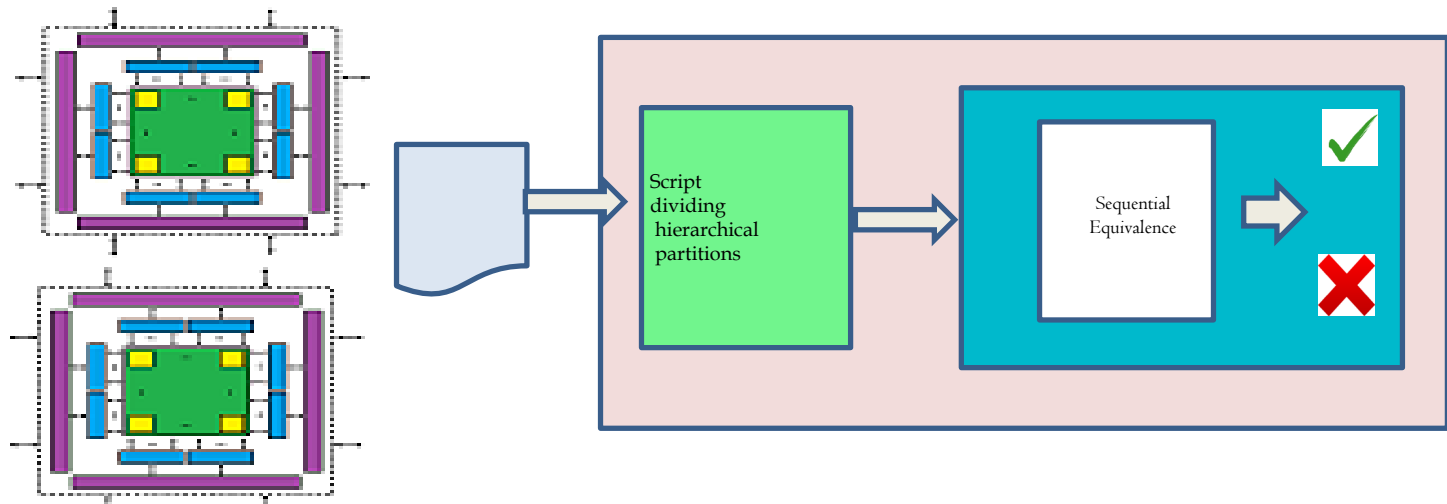**REDUCTION ACHIEVED IN VERIFICATION TIME WITH FV METHODOLOGY**

Can formal be applied on Adjacencies?

We say, Why not?
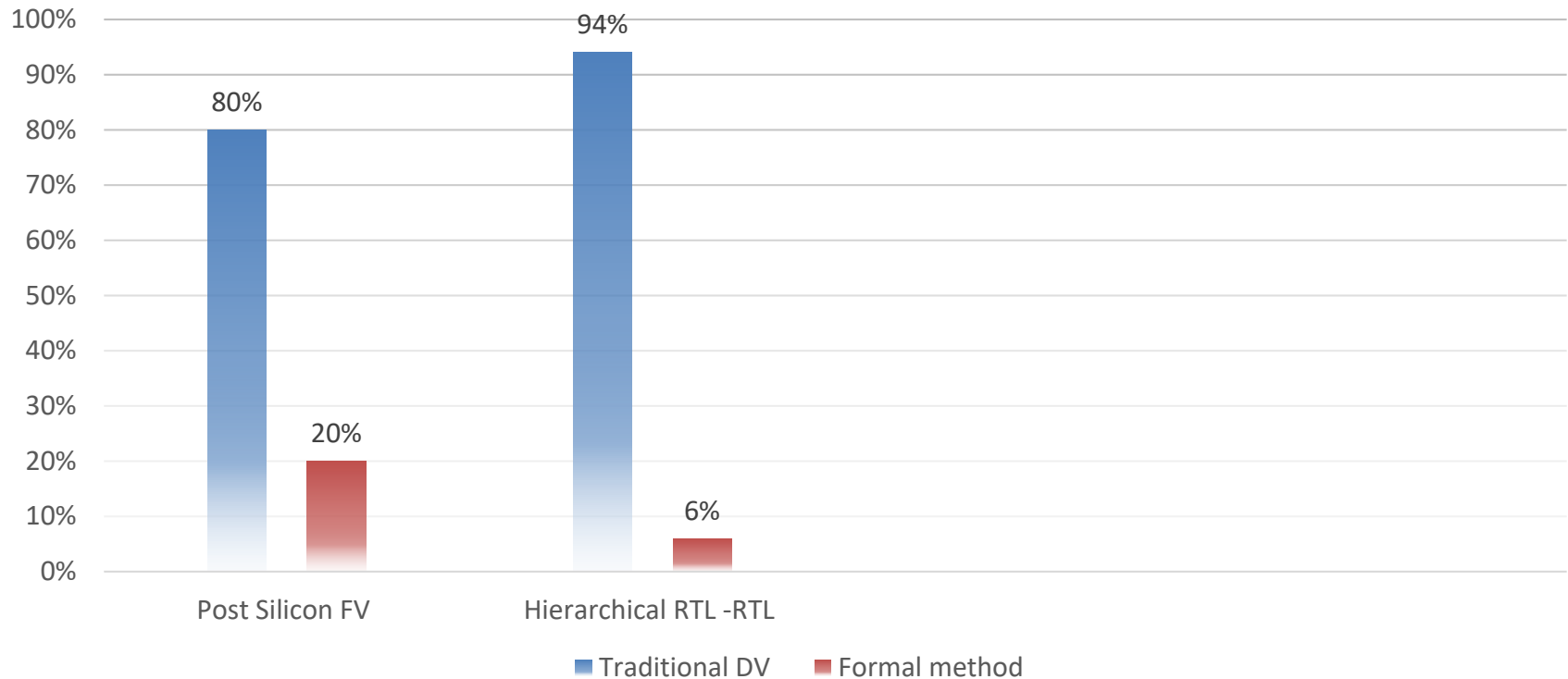
Formal Equivalence @ chip ??

- Known application of Sequential Equivalence at the Unit level boundary: Timing fixes, clock gating, chicken bits

  - M AchuthaKiranKumar V, Aarti Gupta, Bindumadhava S S, "RTL2RTL Formal Equivalence: Boosting the Design Confidence"

    (Best paper @ DAC 2015)

- Can Equivalence be scaled up??

- Chip Level boundary: RTL-RTL Sequential Equivalence Checking ?

  - Derivative project, Intended partitions not effected
  - Simulation regression – multiple days

Formal Equivalence @ Chip Level

Chip level Equivalence savings

REDUCTION ACHIEVED IN VERIFICATION TIME WITH FV METHODOLOGY

Legend: Traditional DV, Formal method

Post Silicon FV: Traditional DV 80%, Formal method 20%
Hierarchical RTL -RTL: Traditional DV 94%, Formal method 6%
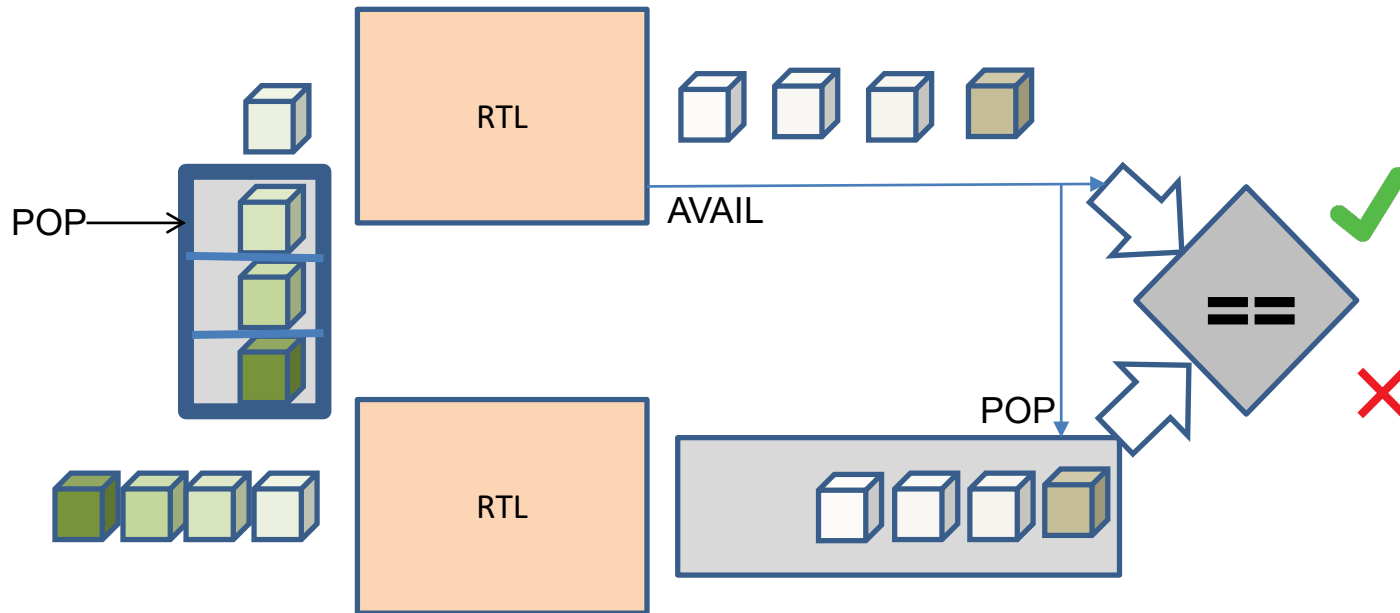
SCHMOO FV

- Transactional Equivalence
  - RTL to generate the same output, for different streaming bandwidths
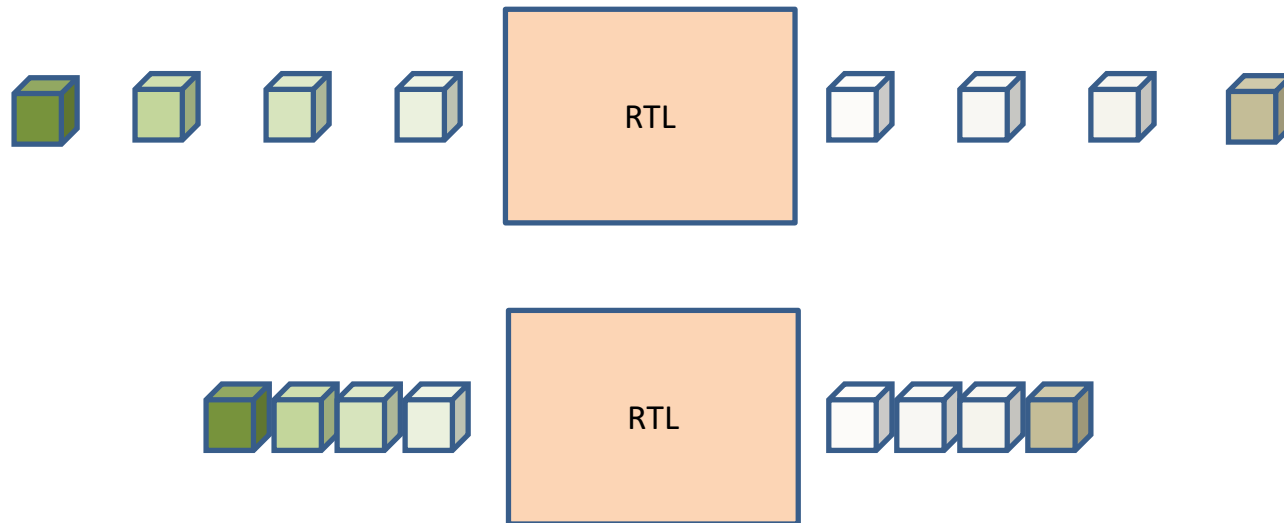
SCHMOO FV contd..,

Schmoo Formal Results

REDUCTION ACHIEVED IN VERIFICATION TIME WITH FV METHODOLOGY

Chart data:

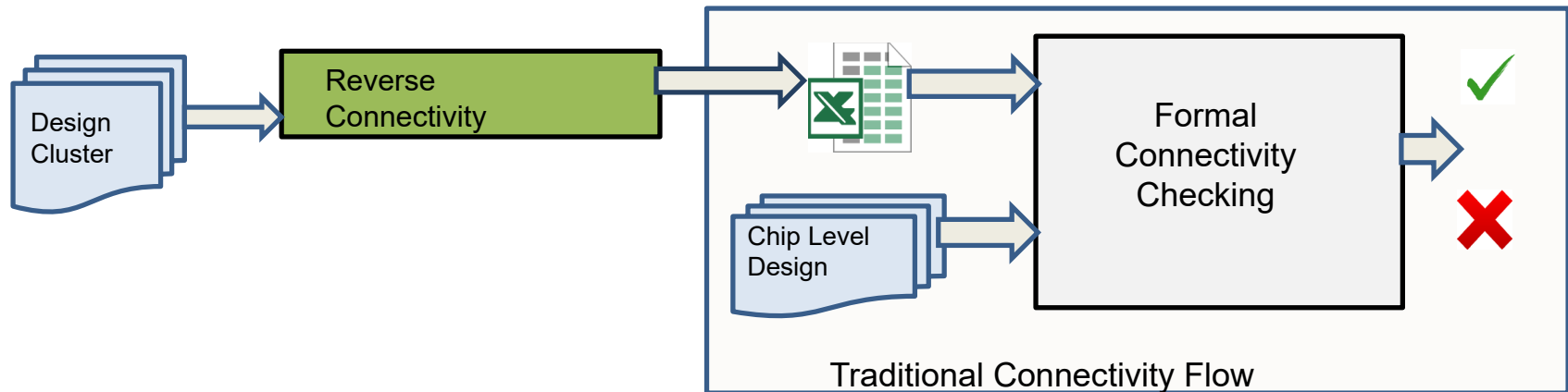| Category	Traditional DV	Formal method
Post Silicon FV	80%	20%
Hierarchical RTL -RTL	94%	6%
Schmoo RTL -RTL	84%	14%
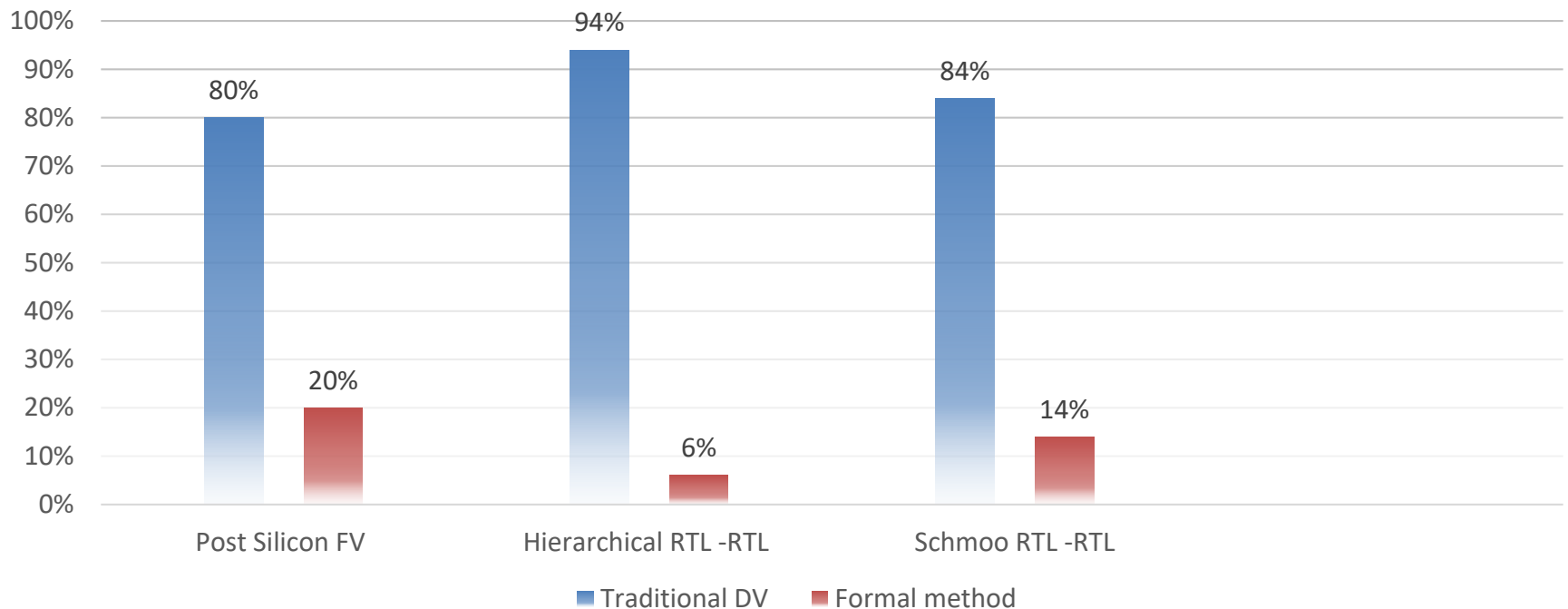
Connectivity Verification beyond SOC?

- Simple Application applicable on various adjacencies

- Full Chip bring up
- Connecting checkers and trackers at FC
- Delivering sub system to SOCs
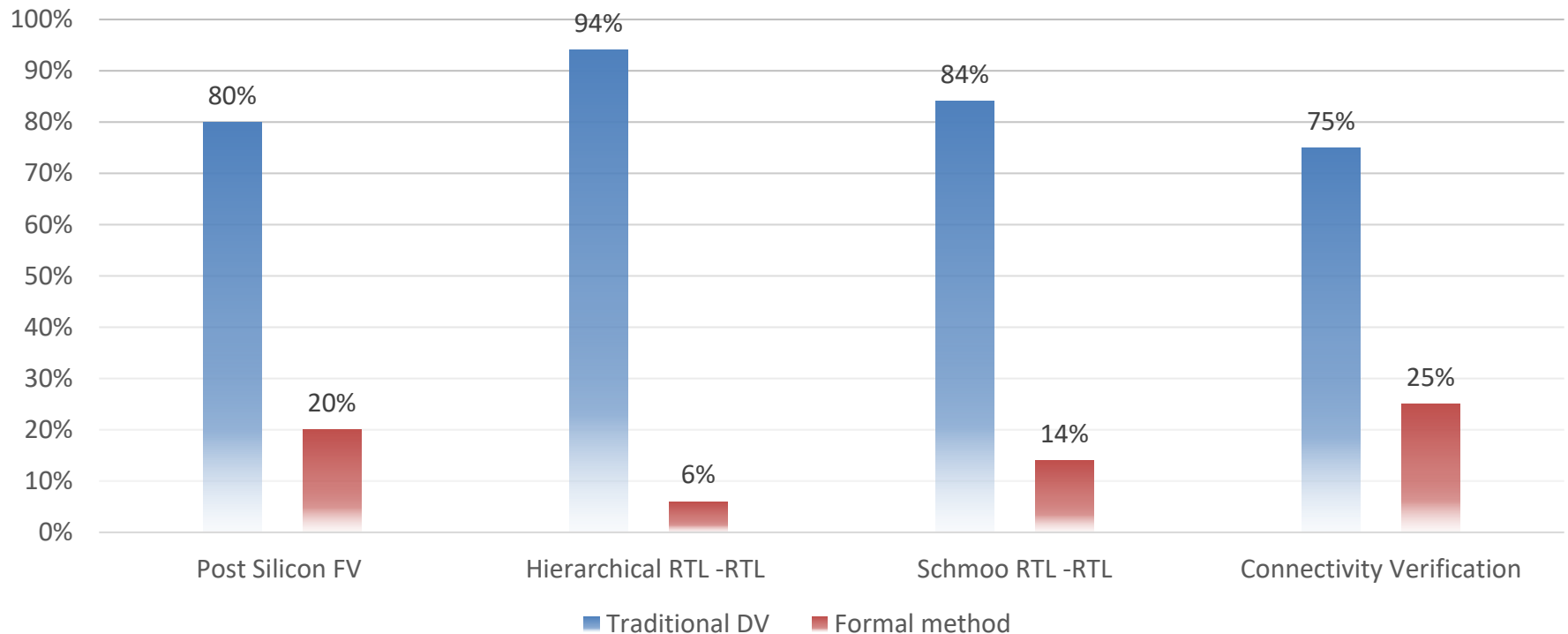- Repeater addition model sanity
- ….many more

Practical application

- Start with a base and scale up the connections
- Use existing features and make formal indispensable

Consolidated Results

REDUCTION ACHIEVED IN VERIFICATION TIME WITH FV METHODOLOGY

Chart showing Traditional DV vs Formal method:
- Post Silicon FV: Traditional DV 80%, Formal method 20%
- Hierarchical RTL -RTL: Traditional DV 94%, Formal method 6%
- Schmoo RTL -RTL: Traditional DV 84%, Formal method 14%
- Connectivity Verification: Traditional DV 75%, Formal method 25%

Legend: ■ Traditional DV ■ Formal method

Conclusion

- Formal beyond traditional applications
- Expand Formal into adjacencies
- Proper application of Formal delivers high ROI
- List to keep expanding to the adjacencies
- Formal will keep expanding
- Formal to become mainstream eventually
 (Liveness property !!!!)

Questions