Metastability captured on a Reset Domain Crossing (RDC) path can cause a chip design to fail.

- Here assertion of reset rst1 near active clock edge of clk1 causes d2 to change in setup and hold time window of clock clk1, leading to metastable output q2.
- In RDC verification such potential issues are analysed. Filtering out noise from Reset Domain crossings can make the process efficient and fast.

### Proposed Methodology (reset assertion)

- The reset generated by Clock and Reset generator block resets rst1, and clock generated goes to clock input of FF2.
- If rst1 asserts near the active clock edge of clk2, the setup and hold time violations of clk2 may cause output of FF2 to become metastable.
- But if the clock and reset are generated in such a way that the generated clock clk2 is always off whenever the generated reset asserts, the metastability at FF2 output gets mitigated.
- Directive helps to convey these design assumptions to the tool.

### Proposed Methodology (reset de-assertion)

- If rst2 de-asserts near active clock edge of clk2, the output q2 may go metastable due to reset recovery and removal time violation of rst2 with respect to clk2.
- But if the generated clock clk2 is always off whenever the generated reset de-asserts, FF2’s input does not get sampled thus mitigating metastability at q2.
- Directive helps to convey these design assumptions to the tool.

### Case Study

- The proposed protocol was run as part of static verification of a real world highly complex SOCs and the filtered results were further validated using functional analysis.

<table>
<thead>
<tr>
<th>Design Size from Real SOCs</th>
<th>Crossings reported without clockoff</th>
<th>Crossings reported with clockoff enabled</th>
<th>Filtered Crossings</th>
<th>Percentage reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A. 1M gate design</td>
<td>4423</td>
<td>8525</td>
<td>5898</td>
<td>40%</td>
</tr>
<tr>
<td>B. 500k gate design</td>
<td>2536</td>
<td>2258</td>
<td>278</td>
<td>11%</td>
</tr>
</tbody>
</table>

Comparison of RDC results on the SOC with and without proposed protocol:

- The tools total runtime was either same or got further reduced after enabling clockoff.
- The implementation also considered the clockoff scenario when the receiver’s clock could be obtained by any combination of clocks specified in constraints.

### Conclusion

- Metastability issues in RDCs are critical, which if not analysed and resolved can prove fatal for a chip.
- The constraints which are specified as part of clockoff protocol are simple which can be extracted from the design itself, no need to review results first.
- If RDC tool does not have this knowledge of clockoff protocol, it will be reporting them as potential RDC issues which need to be further analysed.
- The proposed protocol improves the quality of results obtained via static RDC analysis of a design.
- Overall closure time required for analysing real RDC issues can be reduced, since the noise gets filtered out, only actual RDC issues need to be analysed.

### REFERENCES
