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Fault-Effect Analysis on Multiple Abstraction Levels in Hardware Modeling

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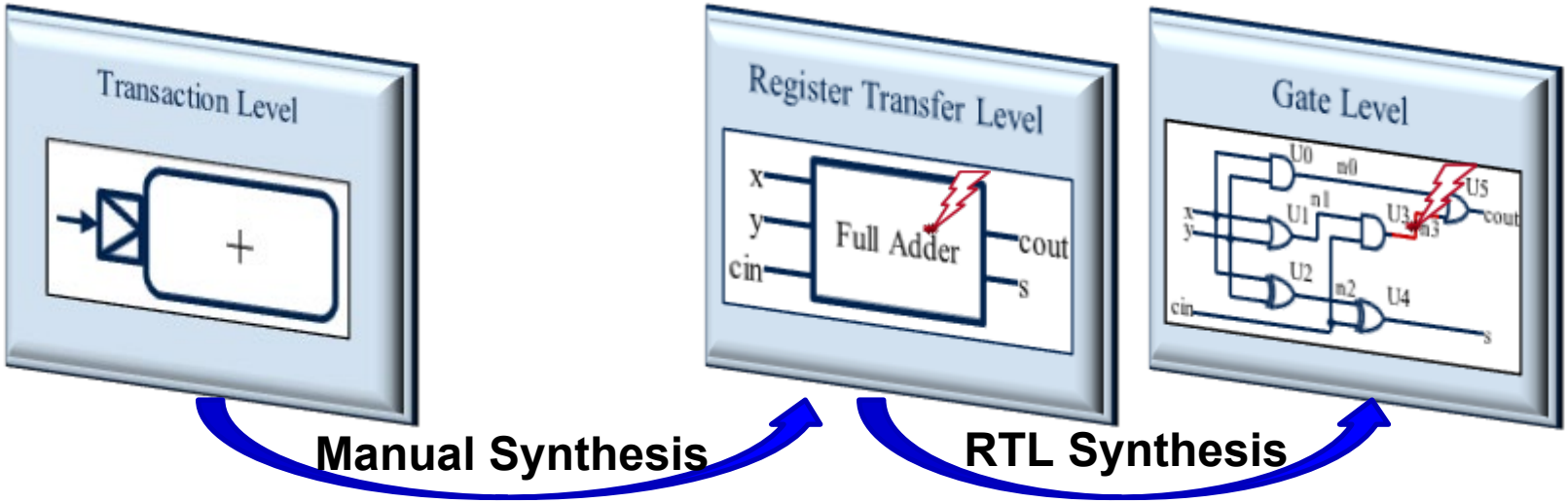
Introduction

ISO 26262

ASIL A B C D

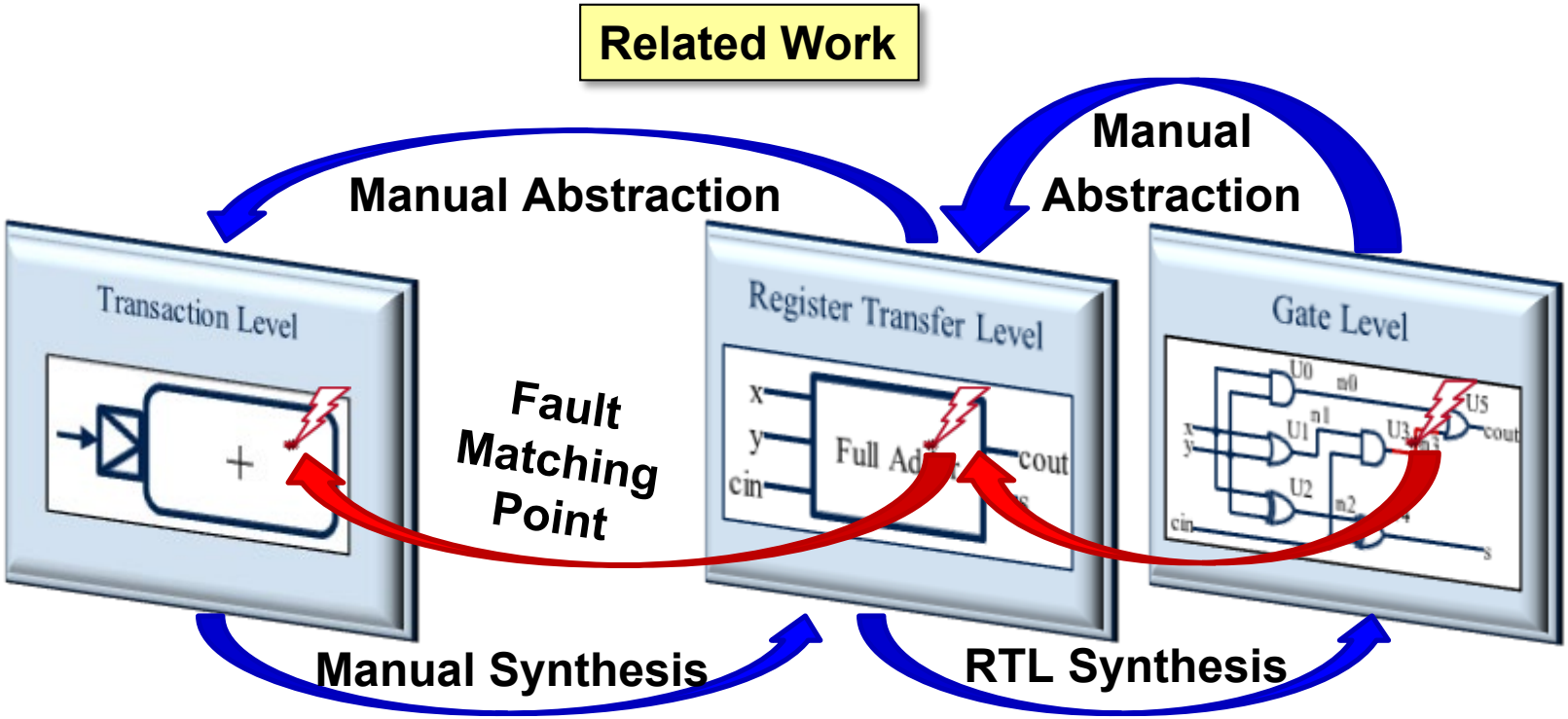
- Failure-Modes Analysis
- Fault Injection
- Fault-Effect Analysis



- ✓ Early availability
- ✓ Fast simulation
- × Less details than RTL or Gate Level

- ✓ High amount of hardware detail
- ✓ Established fault-injection methods
- × Slow simulation speeds
- × Late-stage availability

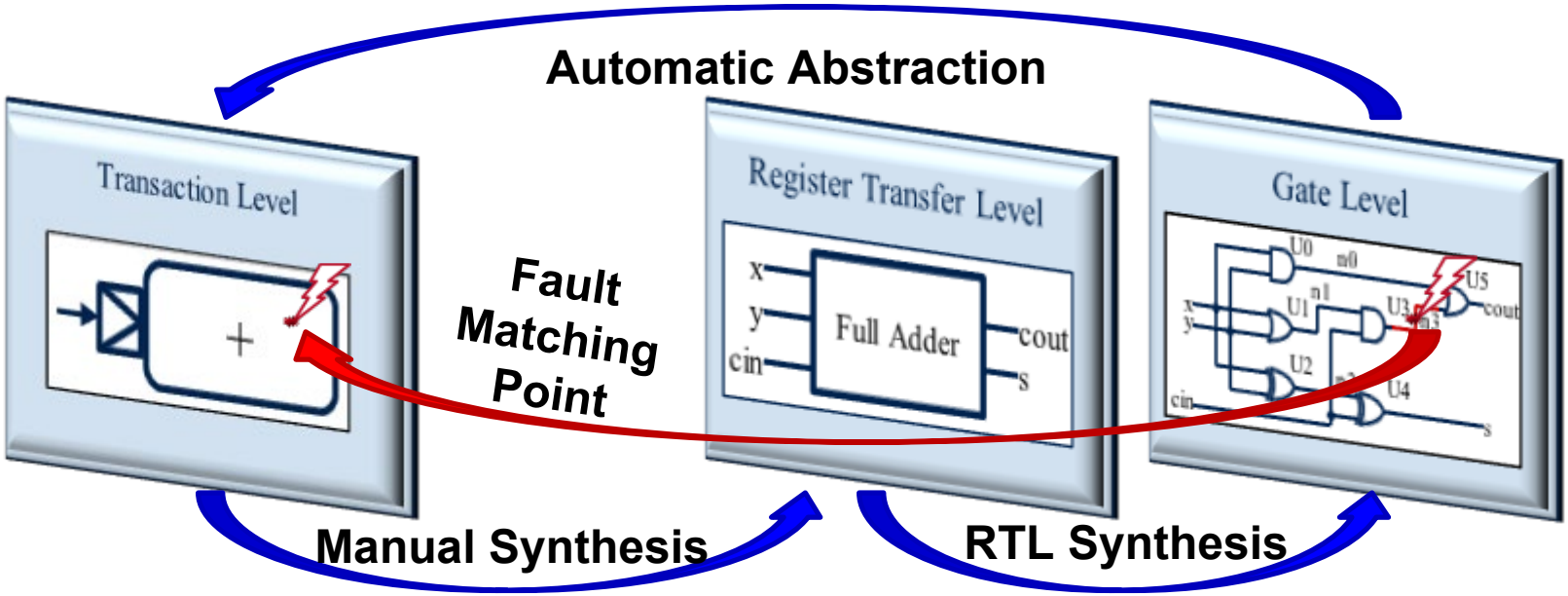
Safety Verification on TLM (I)



- × Manual abstraction
- × Partial RTL or gate-level implementation details
- × No equivalence checking amongst the abstraction levels
- × Fault-injection simulations must be run on all abstraction levels

Safety Verification on TLM (II)

Our Approach



- ✓ **Automatic abstraction**
- ✓ **Gate-level-accurate TL models with all gate-level matching points**
- ✓ **Implicit equivalence checking**
- ✓ **Fault-injection simulation run only on TL abstraction level**

Outline

- Fault Injection into
  - Gate-level-accurate transaction-level (TL) models
  - Generic TL models
- Safety-Verification Platform (SaVer)
- Case Studies
  - Several adder modules
  - MIPS CPU
- Results & Discussion
- Summary

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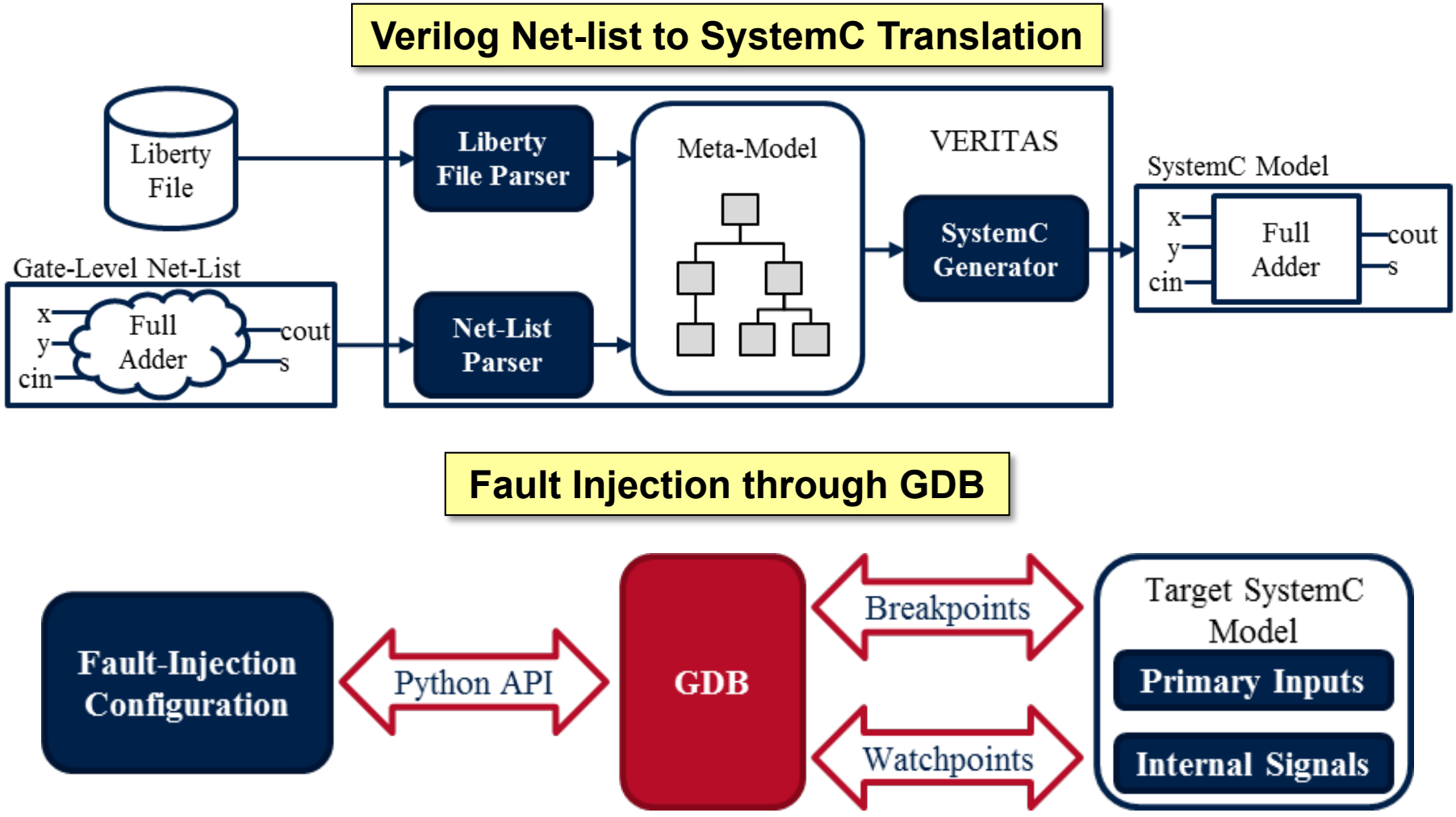
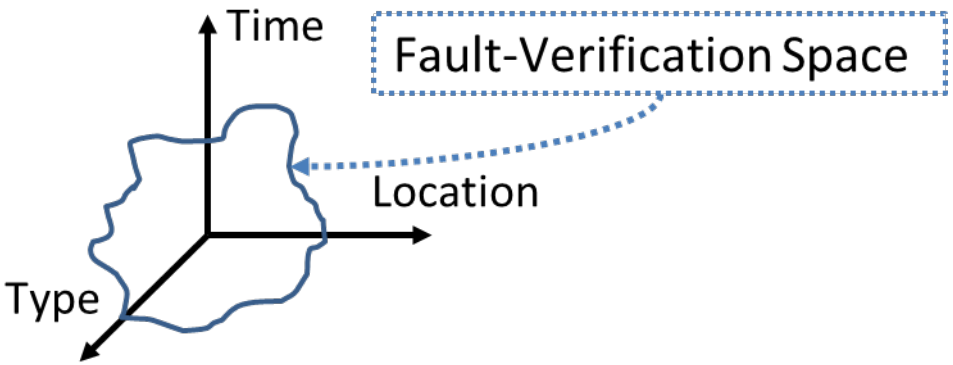
Fault Injection into Gate-Level-Accurate Models (I)



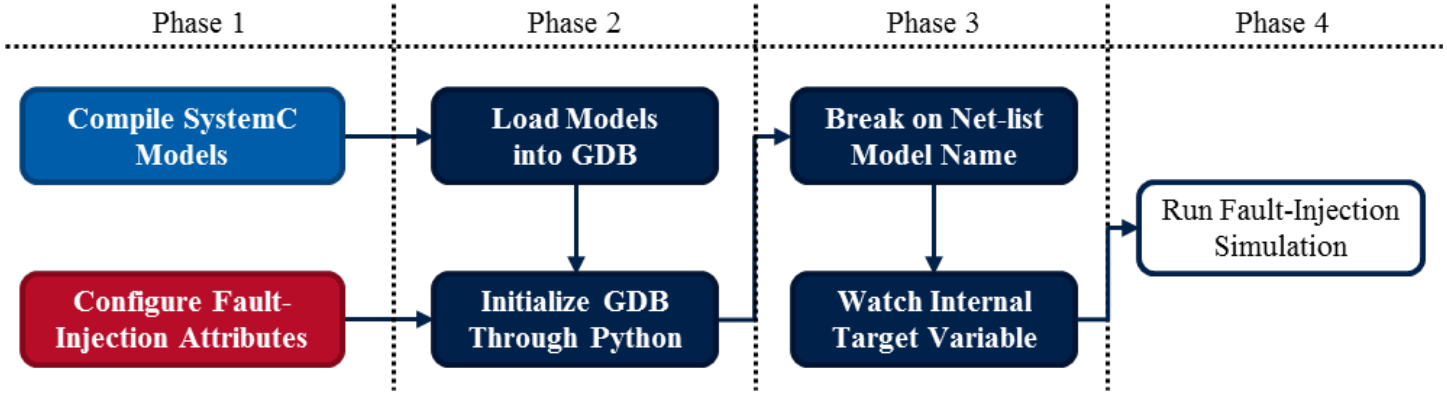
Fault Injection into Gate-Level-Accurate Models (II)

Fault-Verification Space



- ✓ Fault Type
  - ✓ Permanent
  - ✓ Transient
- ✓ Fault-Injection Location
  - ✓ Net-List Wire
- ✓ Fault-Injection Time

Fault-Injection Execution Flow



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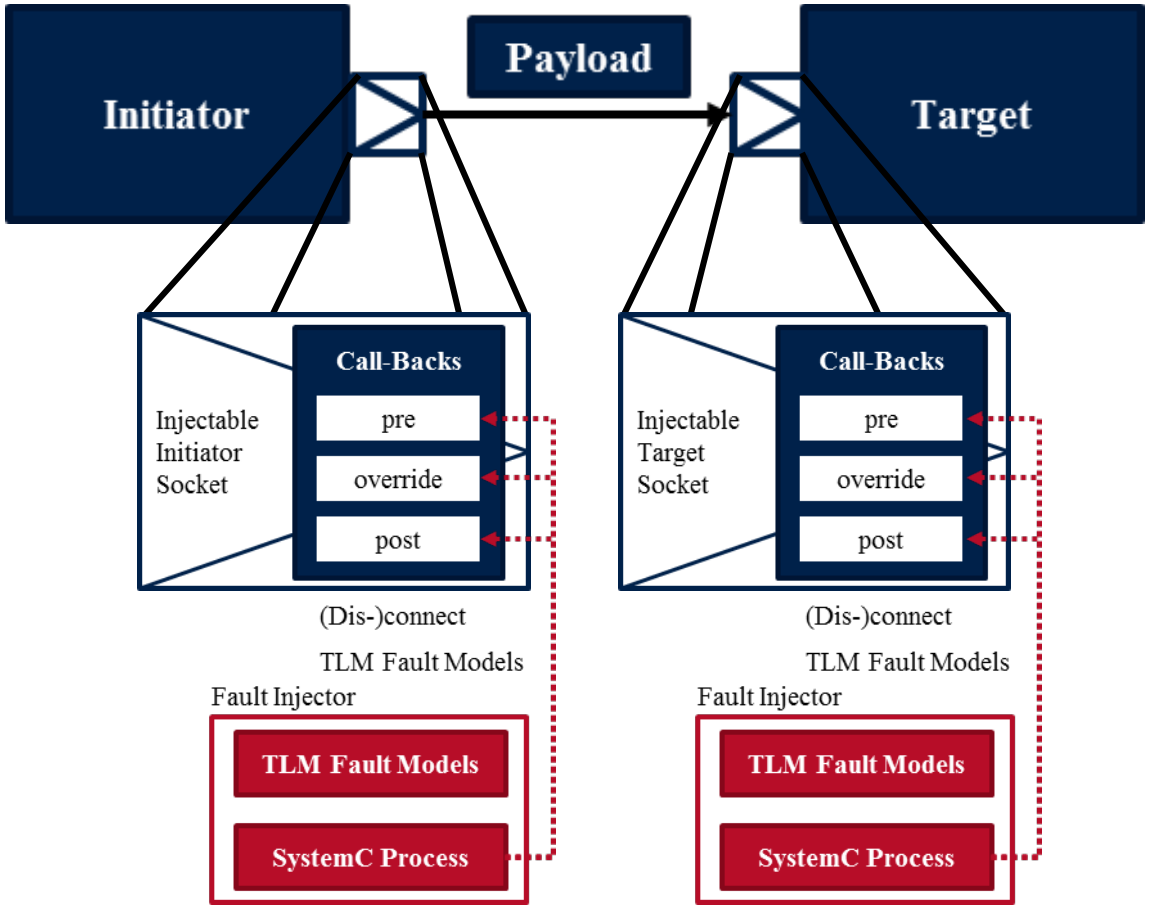
Fault Injection into Transaction-Level Models

Classic TLM Setup

Injectable Initiator and Target Sockets (Zoom In)

Fault-Model Decoupling



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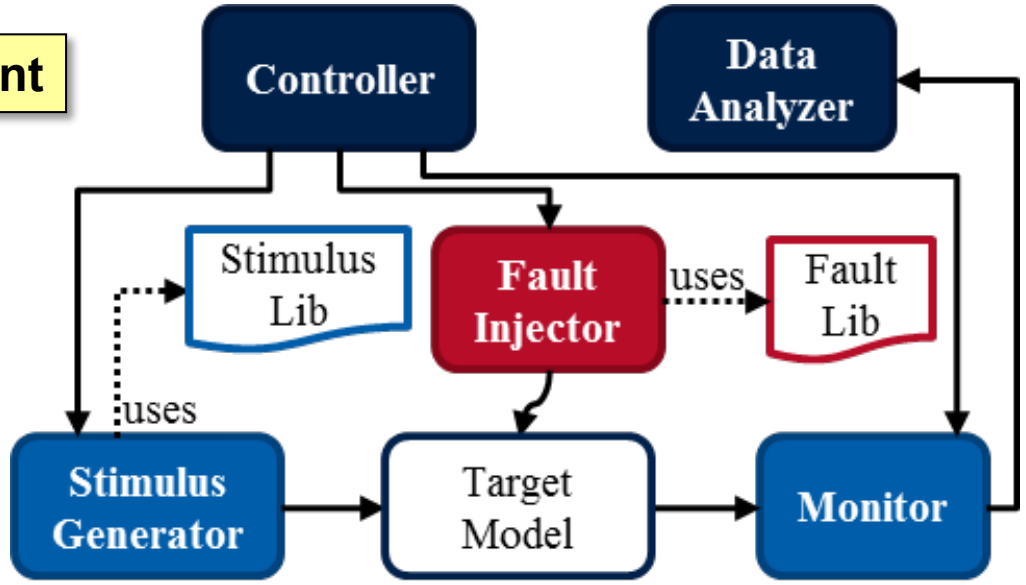
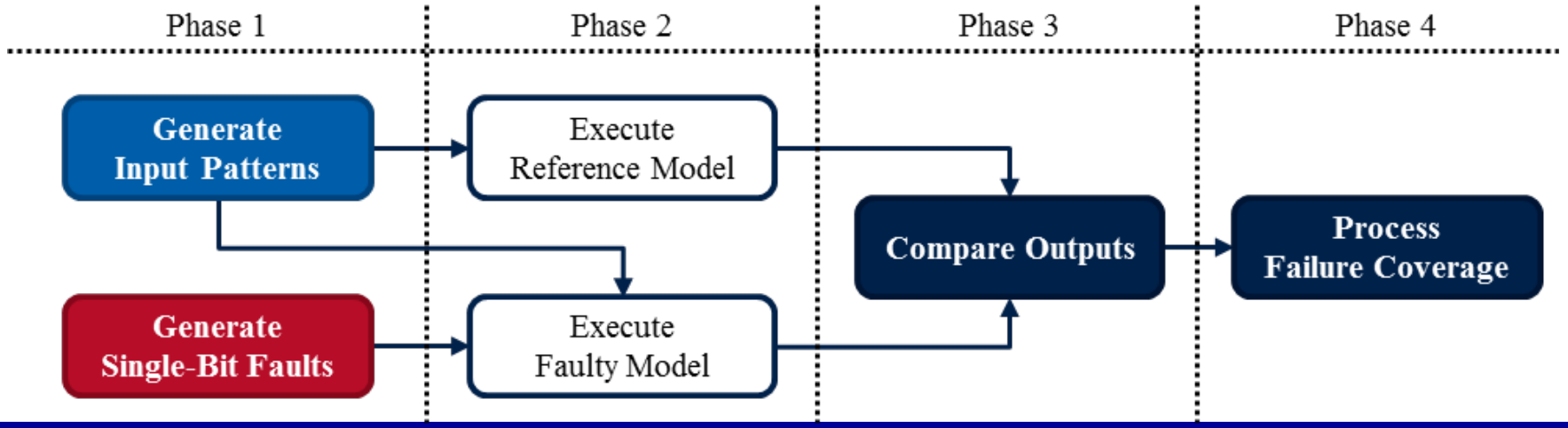
Safety-Verification Platform

Verification Environment



Fault-Injection Flow



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Research Questions

- What are the differences between fault injection into internal states and into the input interface of gate-level and transaction level models?
- What is the probability that single-bit faults lead to multi-bit failures?
  - ISO 26262: common-cause faults
- What is the correlation between gate-level and TLM fault injection?

Experimental Setup

- Models
  - 8, 16, 32 bit adders
  - MIPS CPU
- Monte-Carlo-based fault injection into
  - Internal gate-level signals
  - Inputs of gate-level models
  - Inputs of transaction-level models
  - 10 K, 100 K, 1000 K samples (K = 1000)
- Permanent fault models
  - Stuck-at-0 and stuck-at-1

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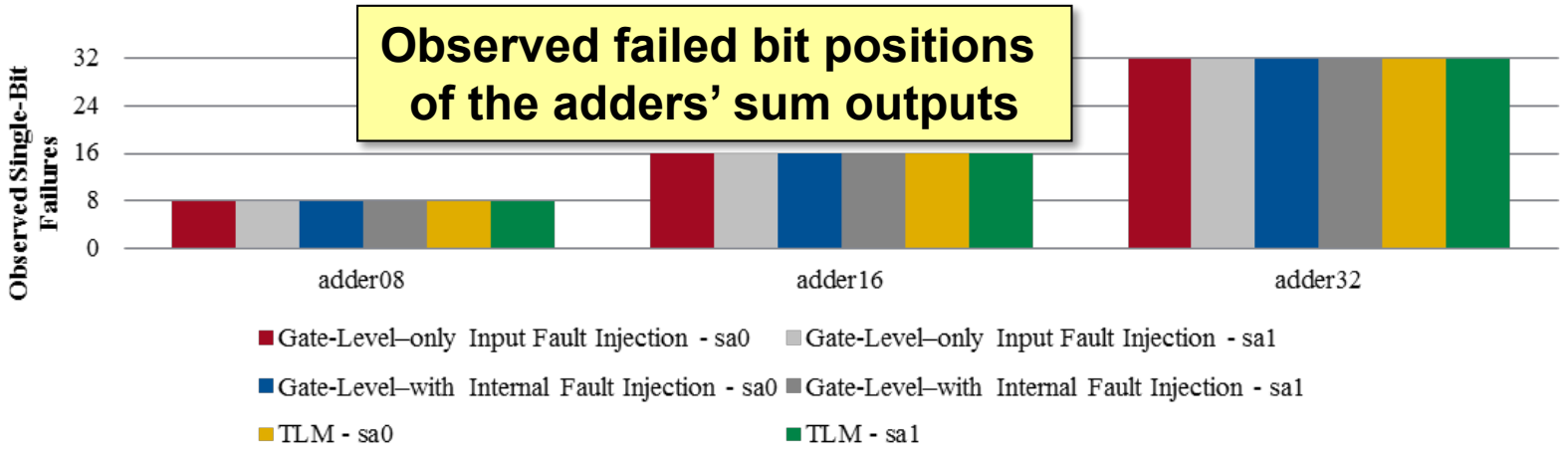
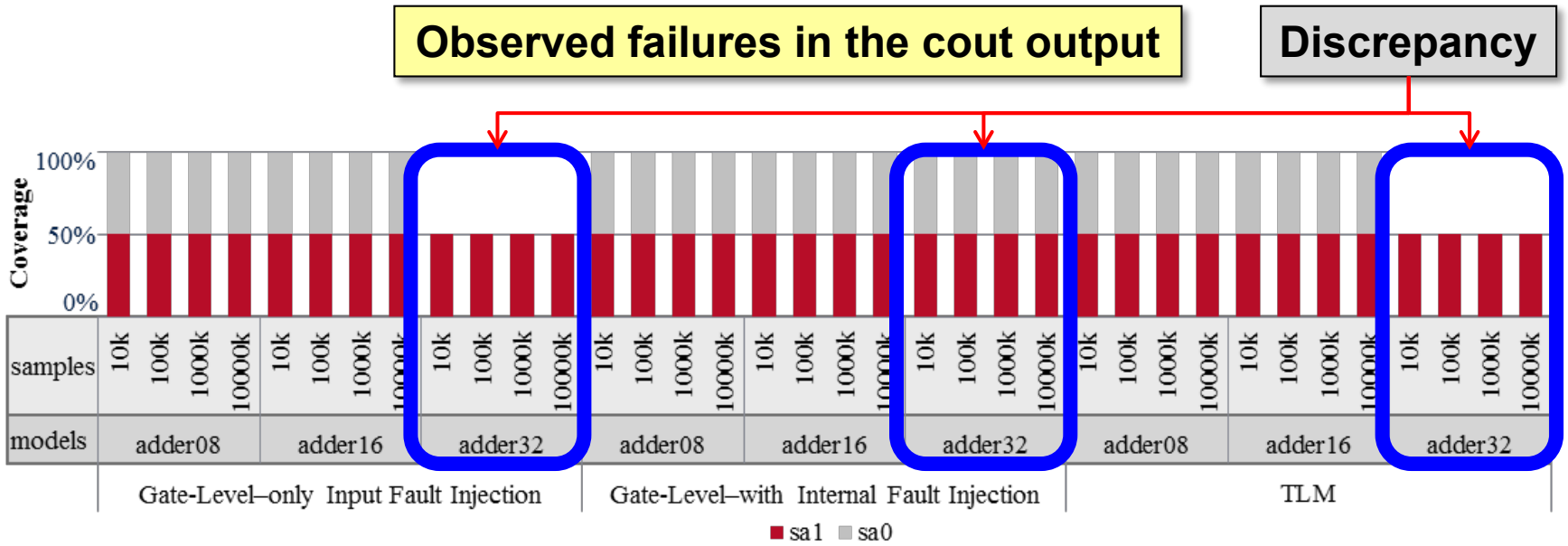
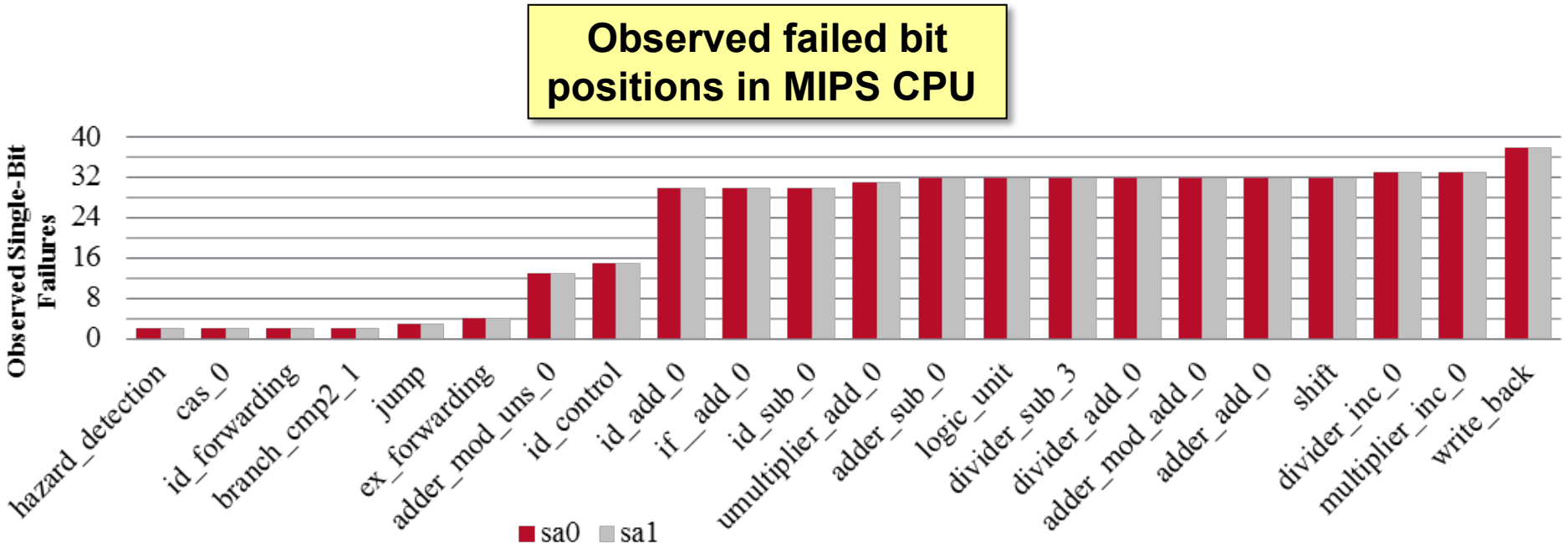
Input Interface vs. Internal Fault Injection – Adders



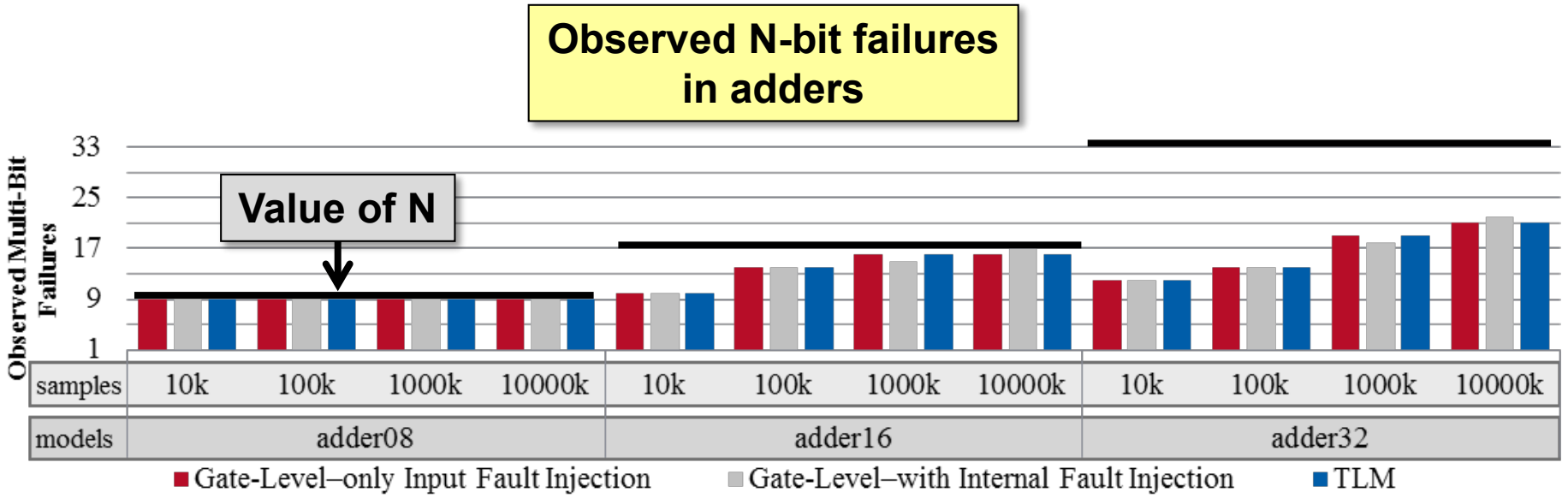


Input Interface vs. Internal Fault Injection – MIPS



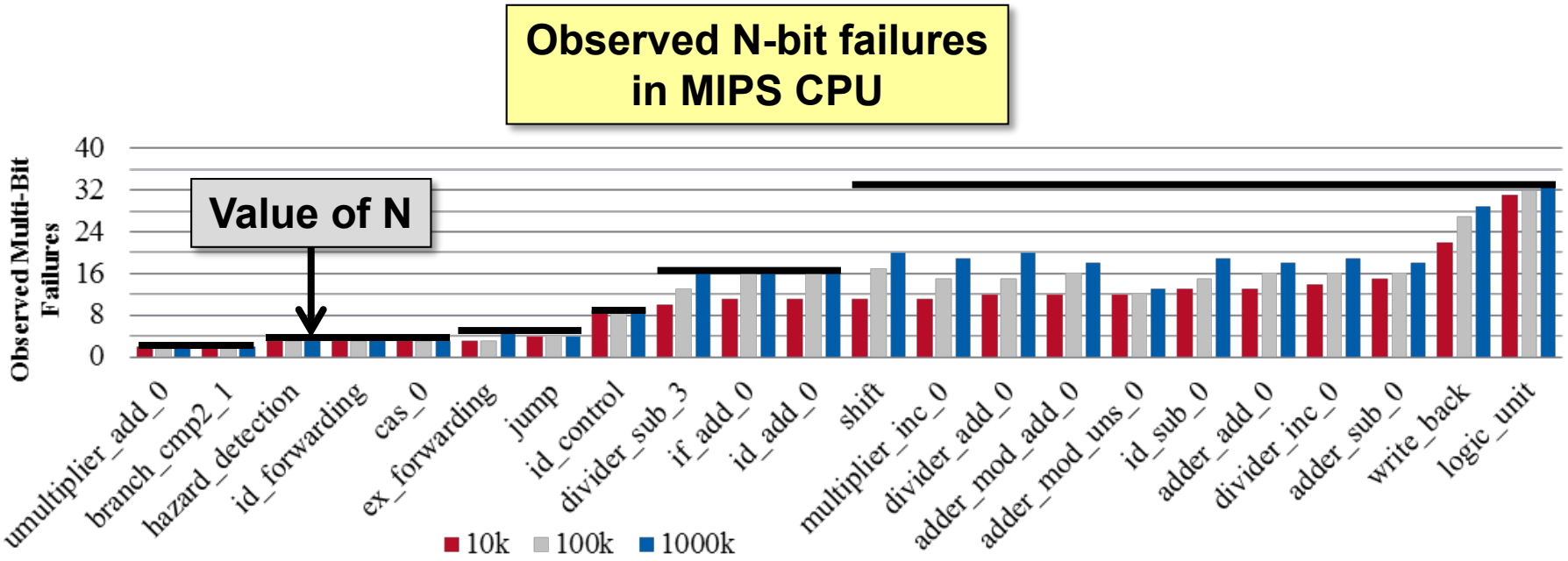
- All single-bit output failures covered
- Identical results for stuck-at-0 and stuck-at-1 faults after 10 000 samples

Single-Bit Fault Injection vs. Multi-Bit Failure Observation (I)



- Very large multi-bit failures (>16 bits) caused by single-bit fault injection are statistically unlikely
- Differences observed amongst gate-level and TLM models are attributed to statistical fluctuations

Single-Bit Fault Injection vs. Multi-Bit Failure Observation (II)



- Unlikely occurrence of large (>16 bits) multi-bit failures after injection of single-bit faults
- Identical results for stuck-at-1 and stuck-at-0 faults
- Identical results for TLM and gate-level models

Simulation Overhead

~2x less overhead for TLM fault injection

GDB-Based Fault Injection

A Model	B Faults Injected	C Reference Simulation Time (s)	D Fault-Injection Simulation Time (s)	E Slowdown Factor (D/C)	F Slowdown Percentage (100*(1-E))
MIPS CPU	0	3.71	3.77	1.016x	1.6 %
MIPS CPU	1	–	4.10	1.105x	10.5 %
MIPS CPU	2	–	4.50	1.213x	21.3 %
MIPS CPU	3	–	4.61	1.243x	24.3 %
			Average	1.144x	14.4 %

Injectable TLM Sockets

A Model	B Faults Injected	C Reference Simulation Time (ms)	D Fault-Injection Simulation Time (ms)	E Slowdown Factor (D/C)	F Slowdown Percentage (100*(1-E))
MIPS CPU	0	248.538	253.706	1.021x	2.1 %
MIPS CPU	1	–	258.934	1.042x	4.2 %
MIPS CPU	2	–	272.149	1.095x	9.5 %
MIPS CPU	3	–	274.137	1.123x	12.3 %
			Average	1.070x	7.0 %

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Take Home Message

- Faults injected into the inputs of a hardware model have the same effects as faults injected into the model's internal signals
- Faults injected into the inputs of gate-level and TLM models have the same effects
- For different input stimuli, stuck-at-0 and stuck-at-1 faults provide the same results
- Random fault injection is sub-optimal for failure-coverage
  - Targeted tests are required to cover corner cases

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Questions?

Thank you!