Regardless what technology is used, whether simulation or formal, when tasked with functional verification project, verification engineers will need qualitative and quantitative measurement of the verification progress. Such metrics are to provide measurement regarding the robustness, completeness, and effectiveness of the verification environment. Fault qualification is an orthogonal mechanism to FormalCore coverage. In this paper, we will discuss how fault qualification provides an additional metric to further improve the formal verification environment to prevent bugs from escaping. It complements other coverage metrics and helps to fast track the formal signoff on the design verification.

Abstract

Coverage Models for Functional Verification Signoff

- Code Coverage
- Functional Coverage
- Assertion Coverage

Coverage Models for Formal Verification Signoff

- Property Density Coverage
- Over-Constraint Coverage
- FormalCore Coverage

Fault Qualification

- Functional Qualification
- Non-functional Qualification

FormalCore Coverage on FIFO

Specifications:
- The count of FIFO asserts the full or empty flag are set when the count reaches 'hf or 'h0.
- Value does not change when there's no push or pop.

Assertions:
- check_full : assert property ( @(posedge clk) cnt == 4'hf |-> full);
- check_empty: assert property ( @(posedge clk) cnt == 4'h0 |-> empty);
- check_no_change: assert property ( @(posedge clk) ~push&~pop |=>
  $stable(cnt));

Fault Injection in FIFO

- Fault Injection: Behavior faults injected into RTL design
- Fault Qualification in a nutshell

Fault Qualification Results

- After 100 FormalCore Coverage
- Potential RTL Bug Can Still Escape!!

Result Comparison Before and After Fault Qualification

- Controller IP FormalCore reached 100% with no more bugs found before fault qualification
- 54 more checkers were added after reviewing fault qualification analysis results
- Additional 5 RTL bugs found!

Conclusion

- Fault qualification in the last stage of formal verification signoff
- Provide additional metric to further improve the formal verification environment
- Provide guidance to the weakness in formal environment
- Shed light on cases of vague or incomplete specification, as well as holes in the verification environment.
- Prevent bugs from escaping, brings closure to fast track the formal signoff on the design verification.