

# Fast Track Formal Verification Signoff





# SYNOPSYS®



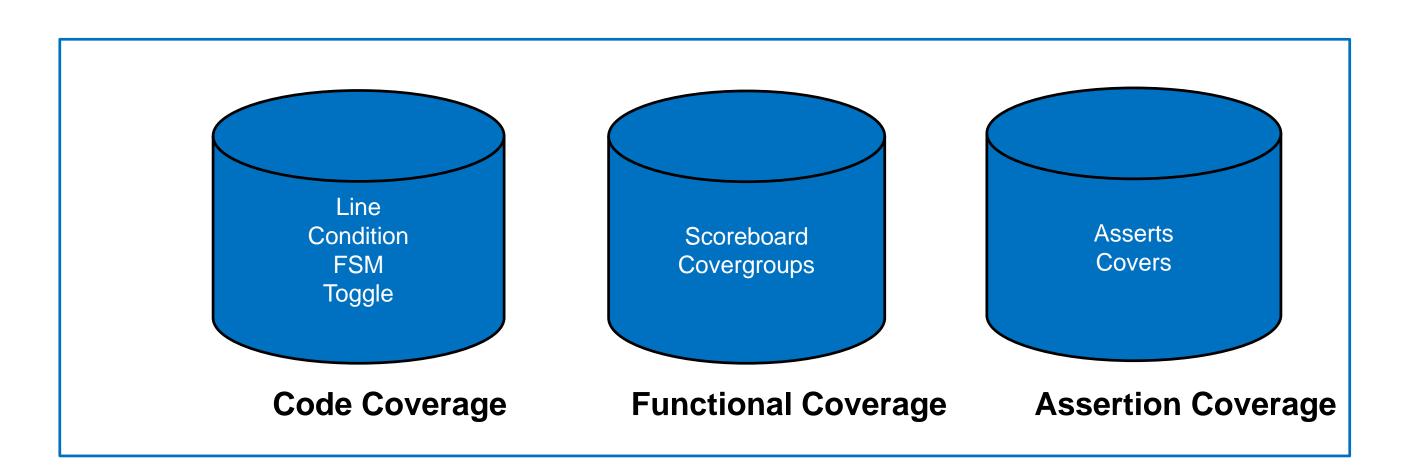




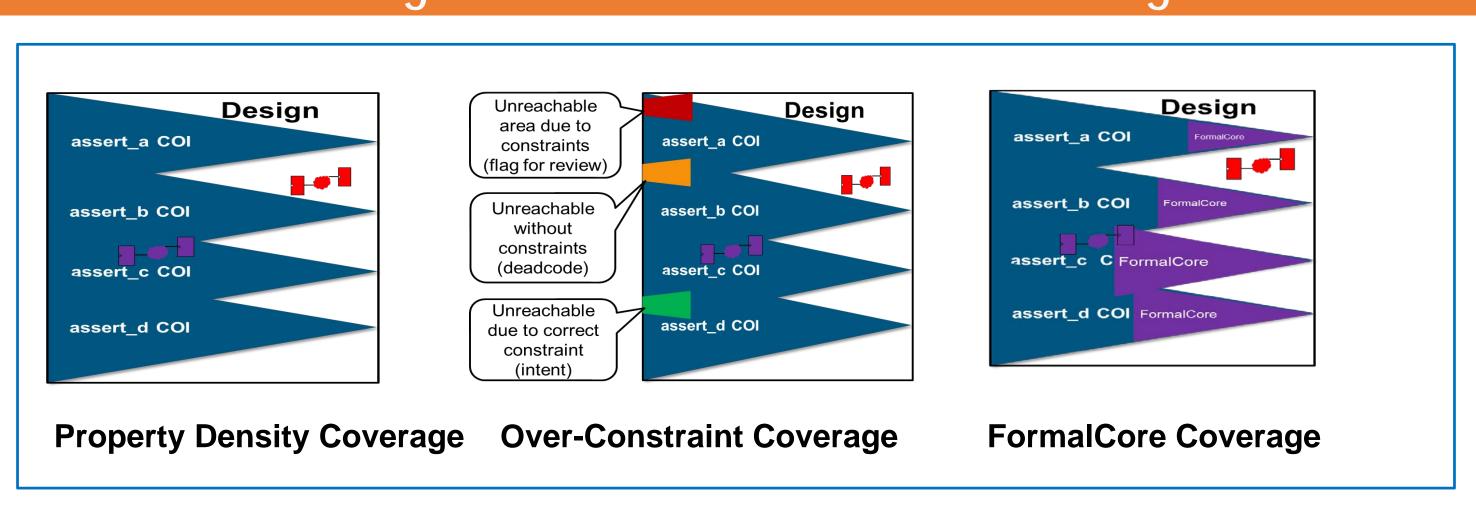
#### **Abstract**

Regardless what technology is used, whether simulation or formal, when tasked with functional verification project, verification engineers will need qualitative and quantitative measurement of the verification progress. Such metrics are to provide measurement regarding the robustness, completeness, and effectiveness of the verification environment. Fault qualification is an orthogonal mechanism to FormalCore coverage. In this paper, we will discuss how fault qualification provides an additional metric to further improve the formal verification environment to prevent bugs from escaping. It complements other coverage metrics and helps to fast track the formal signoff on the design verification.

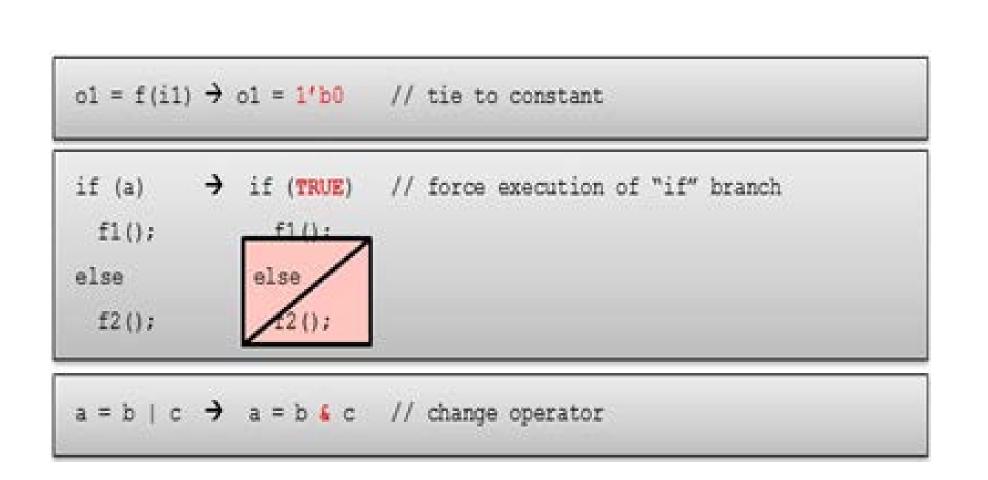
#### Coverage Models for Functional Verification Signoff



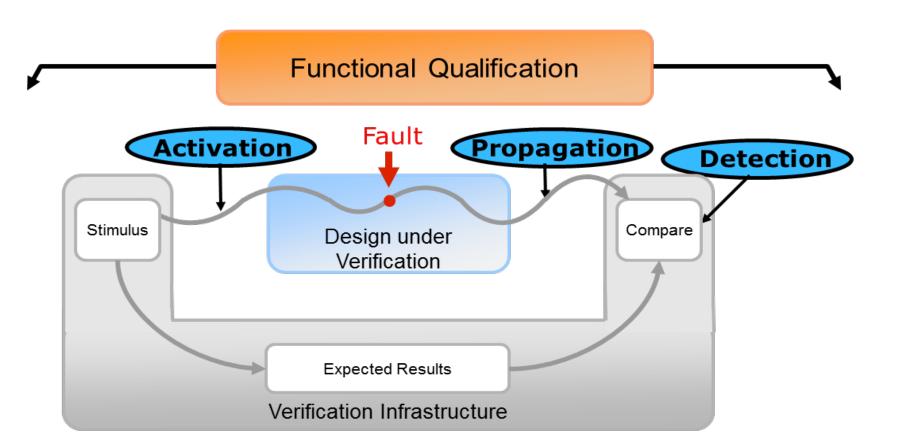
## Coverage Models for Formal Verification Signoff



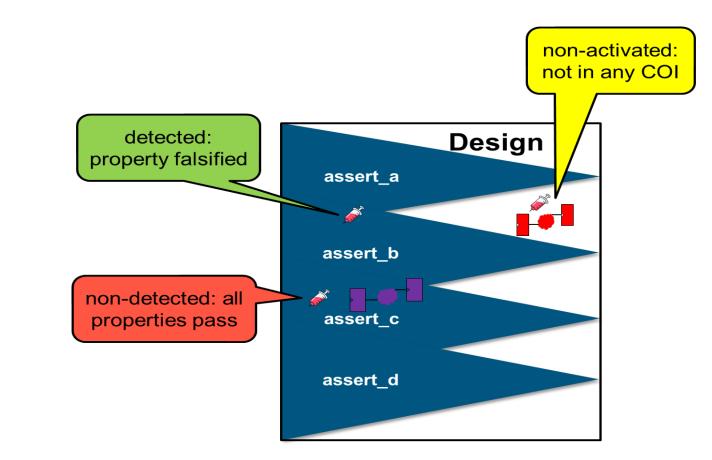
## Fault Qualification



Behavior faults injected into RTL design

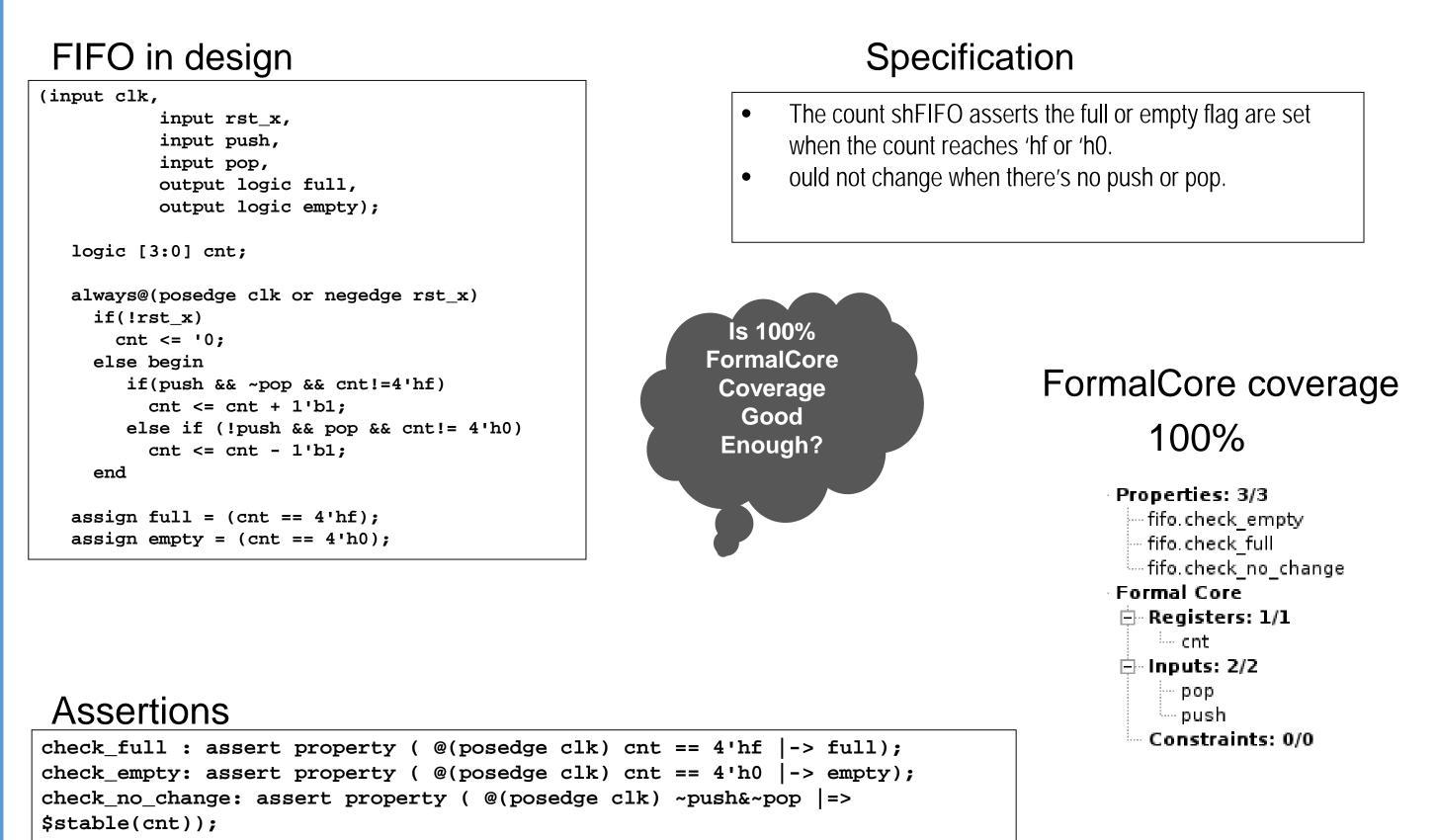


Fault Qualification in a nutshell

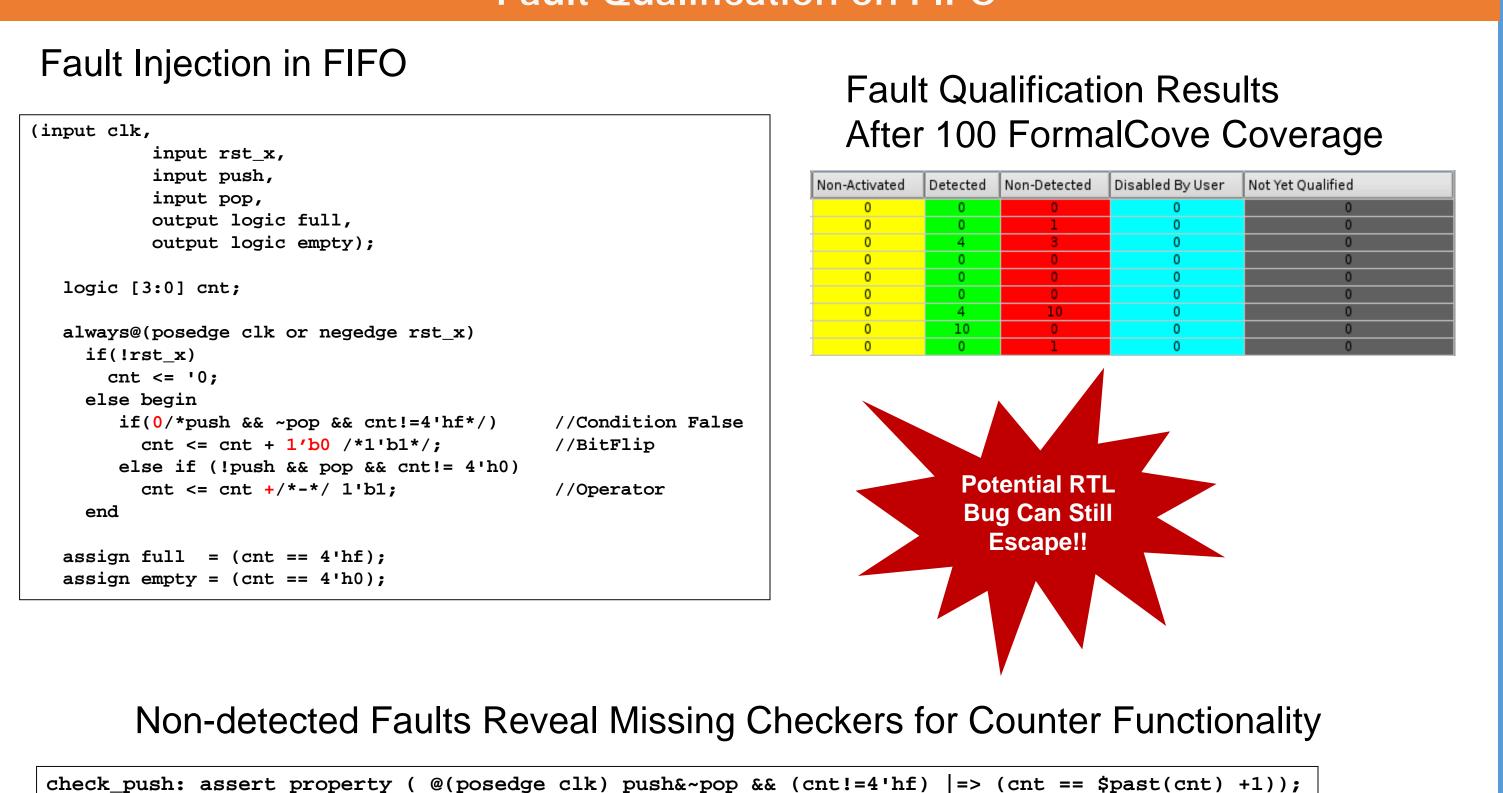


Fault Qualification in formal verification

# FormalCore Coverage on FIFO



# Fault Qualification on FIFO



#### Result Comparison Before and After Fault Qualification

- Controller IP FormalCore reached 100% with no more bugs found before fault qualification
- 54 more checkers were added after reviewing fault qualification analysis results
- Additional 5 RTL bugs found!

Controller IP	Before	After	Missing Properti	ies
Checker properties	208	262	54	Missing properties
New RTL bugs found	0		New RTL ugs found!	proportios

#### Conclusion

Fault qualification in the last stage of formal verification signoff

check\_pop : assert property ( @(posedge clk) ~push&pop && (cnt!=4'h0) |=> (cnt == \$past(cnt) -1));

- Provide additional metric to further improve the formal verification environment
- Provide guidance to the weakness in formal environment
- Shed light on cases of vague or incomplete specification, as well as holes in the verification environment.
- Prevent bugs from escaping, brings closure to fast track the formal signoff on the design verification.