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Eradicating X-bugs and Achieving Higher Design Quality Using Static X-propagation Sign-off

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Overview

- Problem Definition
- Benefits of a Static Solution
- Analysis examples
- Benchmarks
- Conclusion

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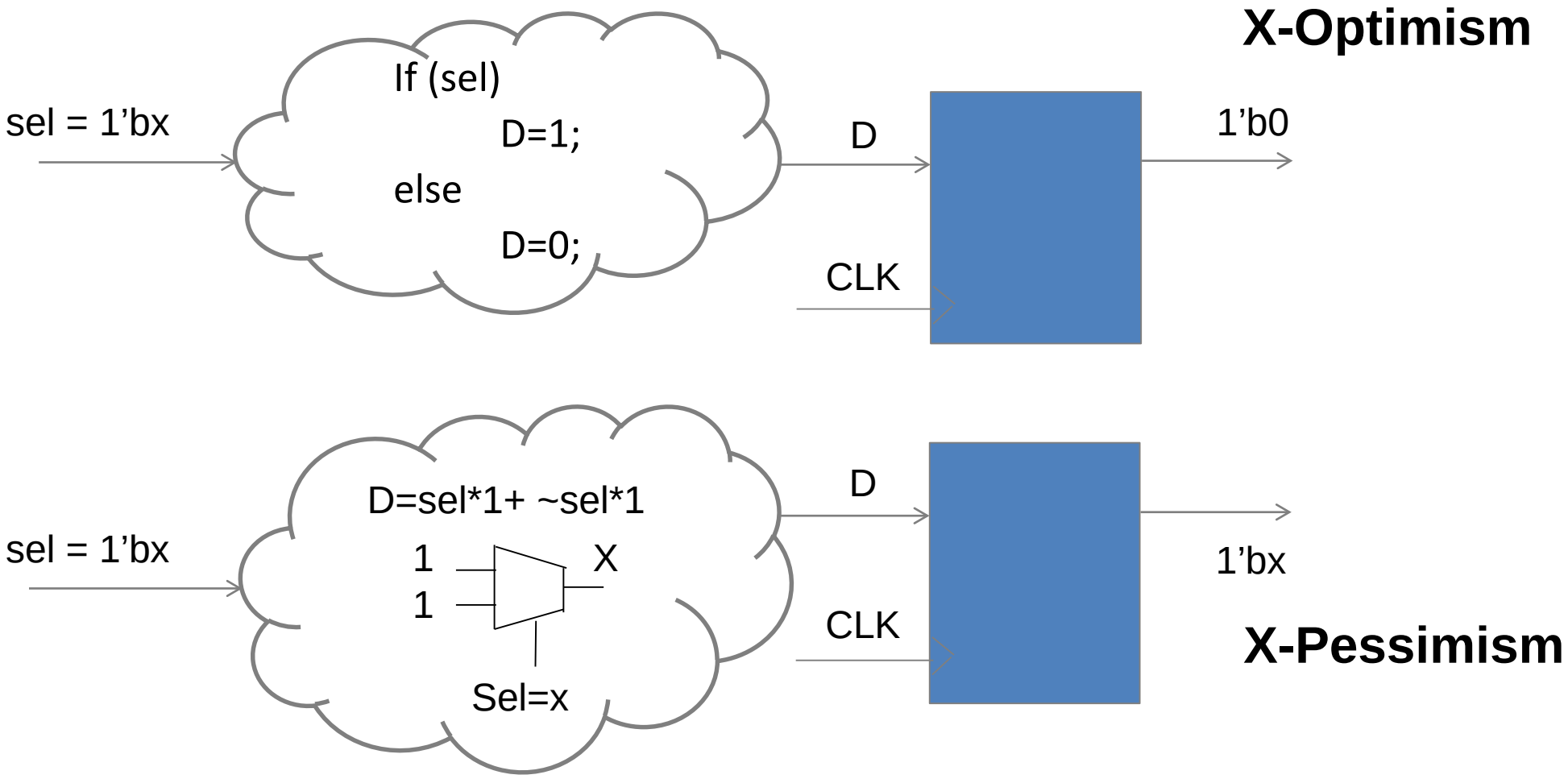
Problem Definition – X-sources

- Design bugs introduce Xs
- Several conditions cause X value in Simulation
- Ignoring X-propagation hides functional bugs

Problem Definition – X-propagation Errors



Problem Definition – X-propagation

Design Impact

- Non-deterministic design behavior similar to CDC/RDC
- Real design problems masked by un-prioritized reporting

Problem Definition – X-propagation

Sign-off Impact

- Entire validation chain is compromised due to X-issues

- Incumbent methodology has a hole with unresolved Xs

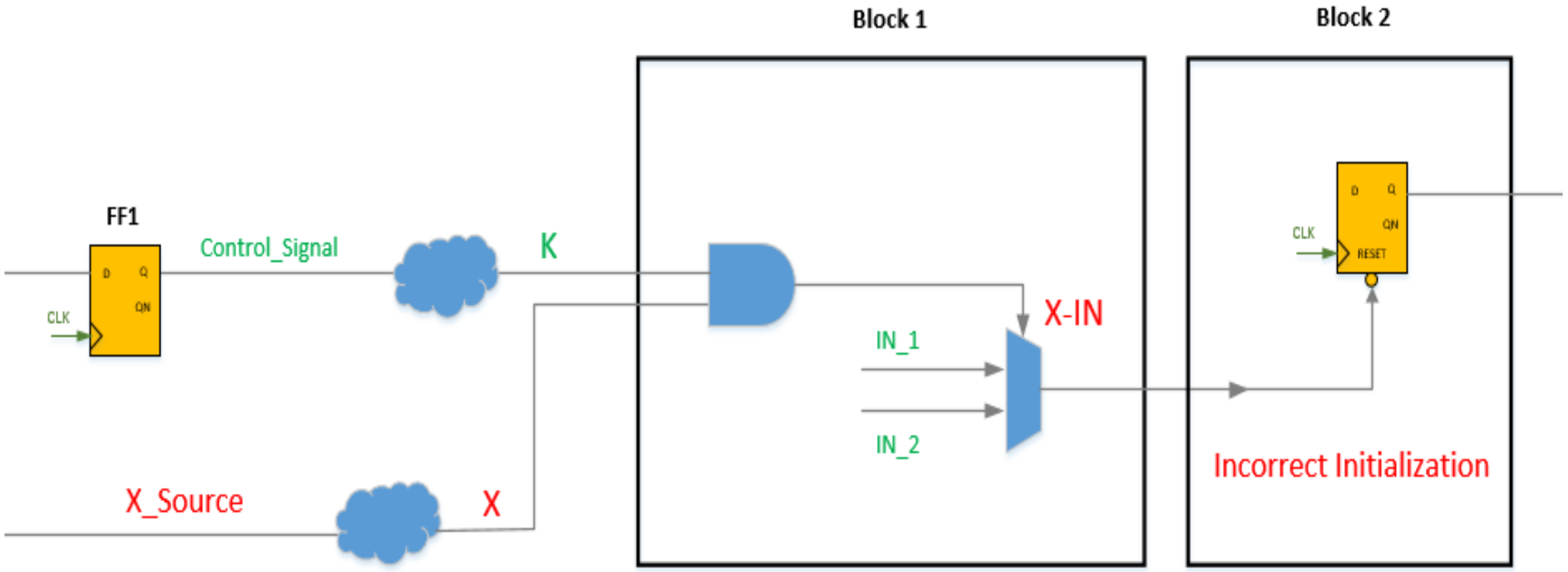
Why a **Static Solution** is Needed

- Relying on simulation is inefficient and can be incorrect
- X-prop simulation can be incomplete

Why a **Static Solution** is Needed

- Assertion-based / RTL Coding Methodology is not enough
- Formal Verification is not practical as the sole solution
- Design quality improvement opportunity missed

Complete X-propagation Sign-off



Report X-Source

Report X-Optimism

Report X-Reset

Initialization Analysis

- Initialization status, reset type, control/data classification for all FFs

X_RESET - List of flops and latches with their resettability information

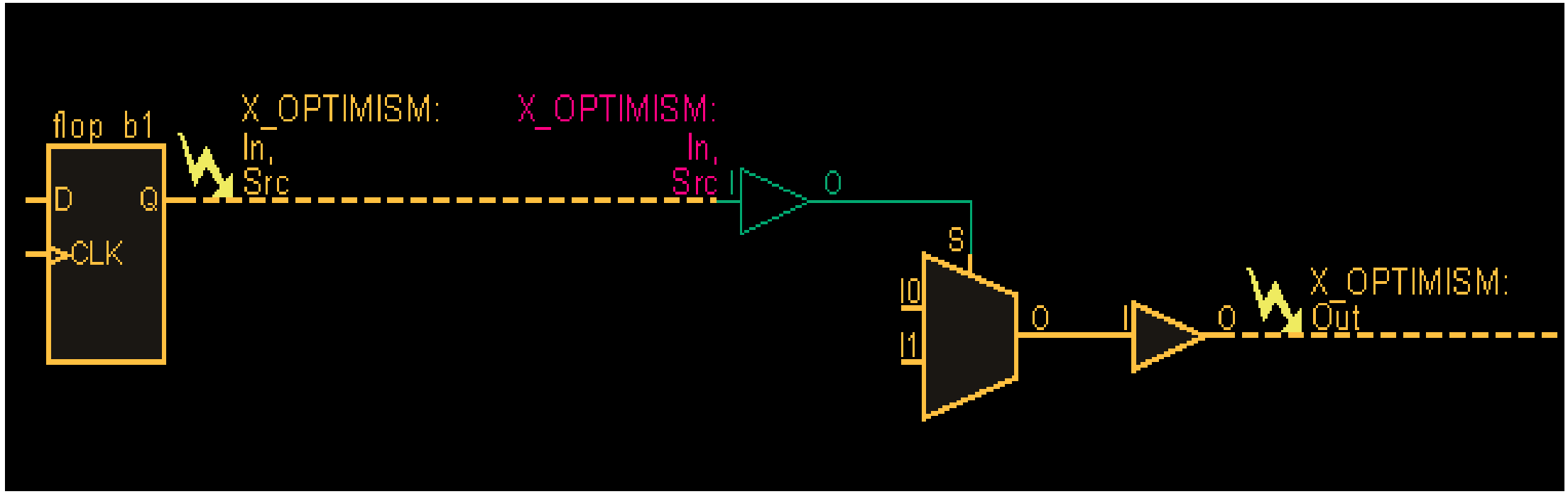
Rows Per Page: 25 | Show/Hide Columns | Commit | Reset | Multi-Column Sort | Total Rows: 16

Selection:

	Command	RuleDataId	ResetScenario	Signal	ResetType	InitializationTime	Value	EngineComments
1	audit_resets	1		flop_b2[7:0]	AsyncReset	0	10101010	DataPath
2	audit_resets	2		flop_b1[7:0]	AsyncReset	0	8{1}	DataPath
3	audit_resets	3		flop_a2[3:0]	AsyncReset	0	4{0}	DataPath
4	audit_resets	4		flop_a3[3]	InitAtTime	10	1	DataPath
5	audit_resets	5		flop_a3[2]	InitAtTime	20	1	DataPath
6	audit_resets	6		flop_a3[1]	InitAtTime	30	1	DataPath
7	audit_resets	7		flop_a3[0]	InitAtTime	40	1	DataPath
8	audit_resets	8		flop_b3[7]	InitAtTime	120	0	DataPath,InitAfterReset
9	audit_resets	9		flop_b3[6]	InitAtTime	130	0	DataPath,InitAfterReset
10	audit_resets	10		flop_b3[5]	InitAtTime	140	0	DataPath,InitAfterReset
11	audit_resets	11		flop_b3[4]	InitAtTime	150	0	DataPath,InitAfterReset
12	audit_resets	12		flop_b3[3]	InitAtTime	160	0	DataPath,InitAfterReset
13	audit_resets	13		flop_b3[2]	InitAtTime	170	0	DataPath,InitAfterReset
14	audit_resets	14		flop_b3[1]	InitAtTime	180	0	DataPath,InitAfterReset
15	audit_resets	15		flop_b3[0]	InitAtTime	190	0	DataPath,InitAfterReset
16	audit_resets	16		flop_a1[3:0]	UnInit	-	4{X}	ControlPath

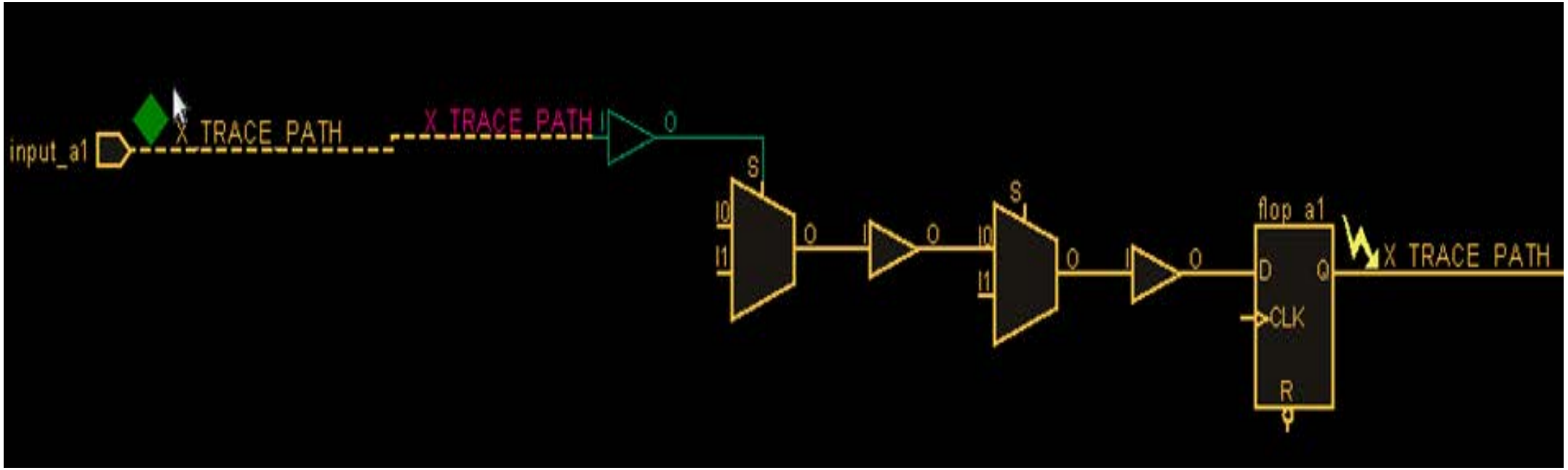
Optimism Analysis

- RTL structures susceptible to Xs, highlighted for root-cause analysis



Reverted-To-X FF Analysis

- Automatically trace RevertedToX FF to an X-source



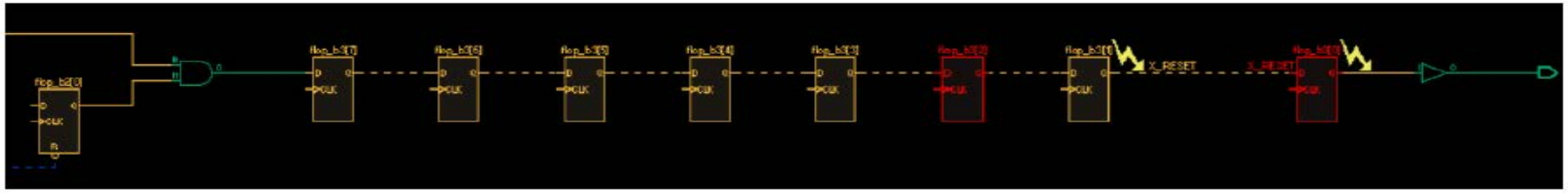
Reset Optimization

- Reports information for improving initialization time, area, power

	Command	Signal	ResetType	Initializ	Value	ResetStatus
1	optimize_resets	flop_a1[0]	NeedsReset	0	0	NoChange
2	optimize_resets	flop_a1[1]	WillBeInit	20	0	RemoveReset
3	optimize_resets	flop_a1[2]	WillBeInit	10	0	RemoveReset
4	optimize_resets	flop_a1[3]	NeedsReset	0	0	NoChange

Initialization Time Improvement

- Desired initialization time specified as optimization goal



Static Analysis Flow Benefits

- Early, Comprehensive, Efficient and Precise
- Root-cause Resolution and not just a band aid
- Single static run for analysis and debug

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Public Domain - RISC-V Design Example Initialization Analysis

- 586191 equivalent gates, 4 black-boxes, 3 minutes runtime
- 1570 Asynchronous reset and 7 uninitialized signals
- Formal analysis certified that uninitialized FFs were harmless

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Proprietary - Network Design Example Optimism Analysis

- Harmful X-sources missed in X-prop simulation flow
- Debug required several months of effort
- Made obvious the risk to other designs
- Static solution quickly identified all X-propagation issues

Benchmark 1 Results

Block Name	Gate Count (NAND2 Equivalent)	Functional Analysis Run-time
Design-1	250 K	1 minute
Design-2	743 K	7 minutes
Design-3	3 Million	21 minutes
Design-4	5.3 Million	51 minutes

- **Optimism Analysis Results Using Real Intent MRXV**

Benchmark 2 Results

Block Name	Gate Count (NAND2 Equivalent)	Cores-Used/Formal Analysis Run-time
Design-1	33.6 Million	4/~5 hrs.
Design-2	27.3 Million	4/~5.30 hrs.
Design-3	4.9 Million	8/~20 minutes

- **Initialization Analysis Results Using Real Intent MRXV**

Conclusion

- Even a few harmful Xs can cause silicon failures
- Focus on X-issues for complete verification methodology
- Address RTL Xs proactively for design reliability and productivity
- Use Static solution for unique comprehensive analysis and debug