Equivalence Validation of Analog Behavioral Models

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VERIFICATION PLANNING

- Behavioral models of analog IPs are used for SoC simulation
- SPICE representation of analog IPs go to Silicon
- Critical to ensure equivalence between behavioral models and implementation (SPICE)

Verilog Model
- EqVC
- Stimuli
- SPICE

Waveform comparison method
- Continuous waveform comparison
- Quick setup time
- Works for both AoT and DoT verification
- TestPlan specifies signals to compare and tolerances
- Report generated and exception/waivers captured

A Library of SystemVerilog Assertions
- Assertions work on both Model and netlist DUV
- Expertise in assertions language and ABV required

Advanced Verification
- UVM constrained random stimulus for analog properties.
- Increased verification coverage
- Compatible with ABV