# Enhancing Productivity in Formal Testbench Generation for AHB based IPs

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## Problem Statement/Introduction

### Formal verification for an IP

- Studying the Design features or Design changes
- Modify FPV/FRV checker manually or adding new checkers
- For AHB Based IP FRV checker can have a distinct structure

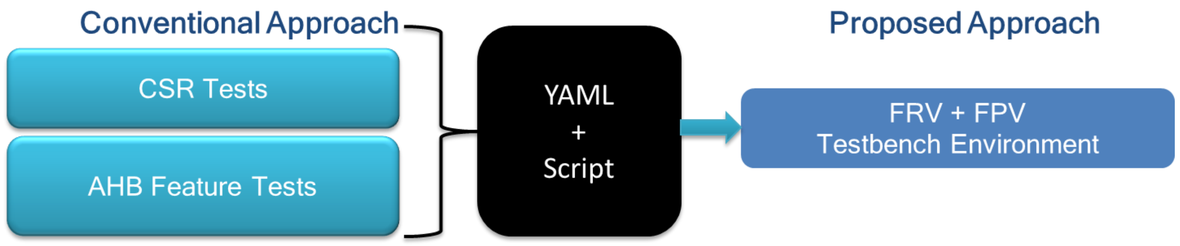
### Problem statement

- For Large number of FPV/FRV checkers, this modification can be laborious and time consuming
- Testbench changes can scale from
  - Signal additions/removal,
  - Assertion additions/removal
  - New test additions/removal
- Manual work is prone to errors

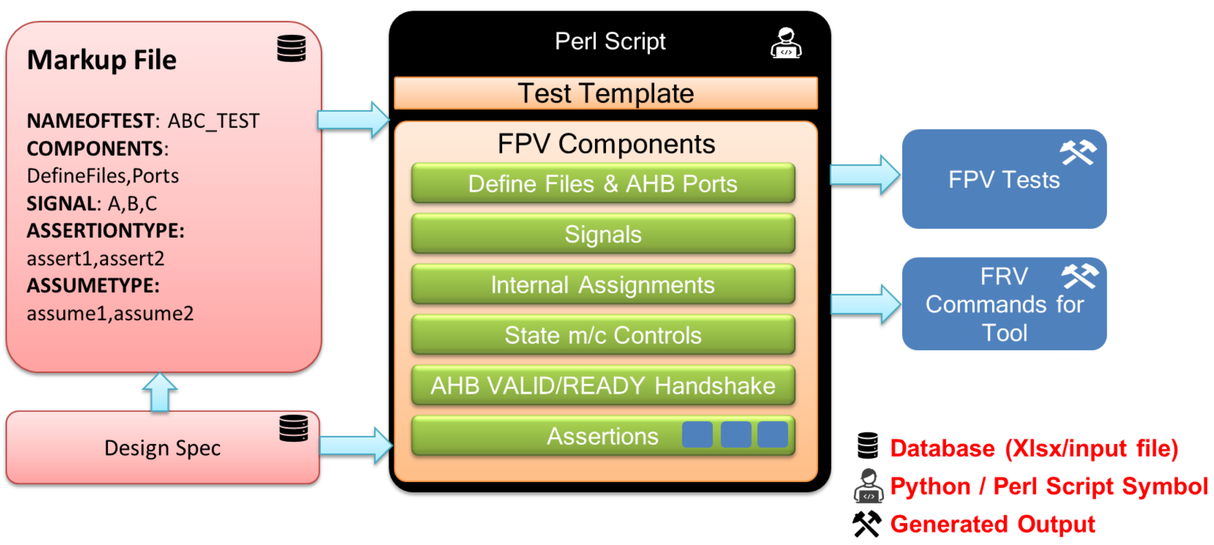
## Proposed Methodology/Advantages

### Proposed approach consist of

- Registers verification through FRV although autogenerated, still needs environment setup enablement which are to be automated
- FPV checkers are categorized and automated through YAML and script

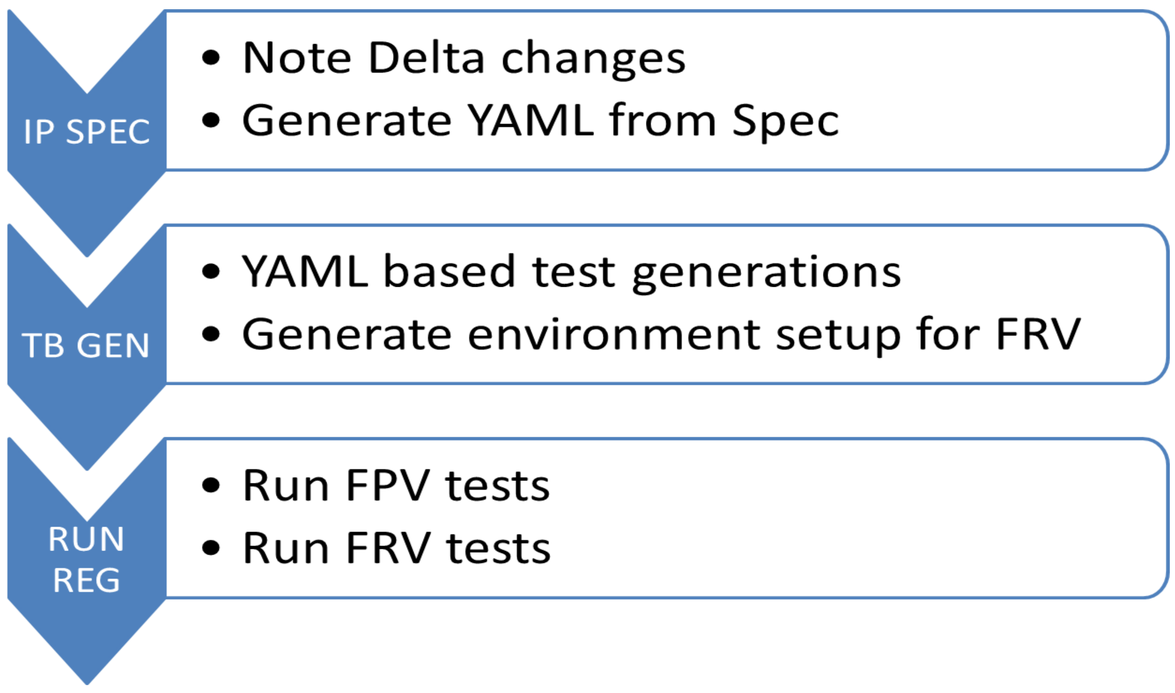



## Implementation Details/Diagram



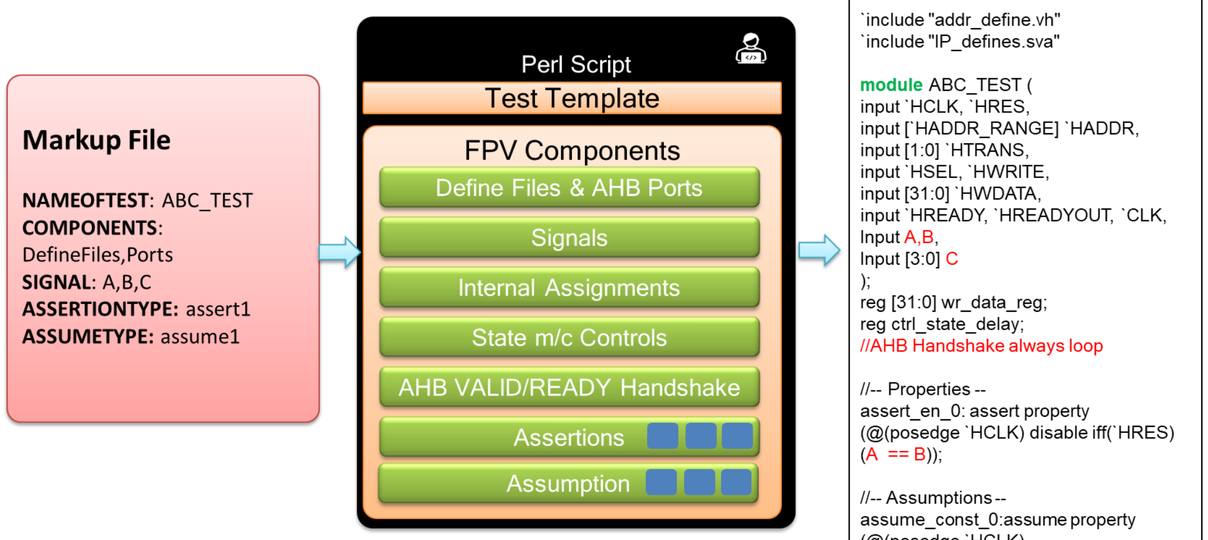

- All tests required infra is available in input.yml.
- YML dependent infra-API is implemented in Perl.
- Perl script will take test infra information from input.yml and required design input will be taken from design spec.

## Implementation Details/Flow Chart




## Demo

The following image shows Demo file generated from script + YAML




```
//This file is autogenerated

`include "addr_define.vh"
`include "IP_defines.sva"

module ABC_TEST (
input `HCLK, `HRES,
input [`HADDR_RANGE] `HADDR,
input [1:0] `HTRANS,
input `HSEL, `HWRITE,
input [31:0] `HWDATA,
input `HREADY, `HREADYOUT, `CLK,
Input A,B,
Input [3:0] C
);
reg [31:0] wr_data_reg;
reg ctrl_state_delay;
//AHB Handshake always loop

//-- Properties --
assert_en_0: assert property
(@(posedge `HCLK) disable iff(`HRES)
(A  == B));

//-- Assumptions --
assume_const_0:assume property
(@(posedge `HCLK)
(C<= 1));

endmodule   // ABC_TEST
```

## Conclusion

- ✓ Entire IP is verified through formal without manual interventions.
- ✓ More Extensive and Exhaustive verification for IP core.
- ✓ Automation removes the scope of manual error in modifying/writing testbench.
- ✓ Overall, there will be a left shift in milestone along with improvement in quality of verification.