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Enabling Digital Mixed-Signal Verification of Loading Effects in Power Regulation using SystemVerilog User-Defined Nettype

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***Abstract*—This paper presents an implementation of Cadence's EEnet structured SystemVerilog User-Defined Nettype (UDN) for electrical modeling that has been used to create real-number (RNM) models of drivers and loads part of the analog circuit involved in power regulation of power management systems. Structured UDN overcomes the natural limitations in modeling loading effects imposed by scalar Verilog-AMS wreal nettypes. This modeling technic enables verification teams to run Digital Mixed-Signal (DMS) simulations with loading effects in power regulation circuits, previously only possible in expensive Analog Mixed-Signal (AMS) simulations. The new capability along with the benefits of a significant improvement in simulation performance enables development teams to execute simulation-based concept studies, wide range of scenario variations and early sign off of the regulation circuits without the need of AMS simulations.**

Keywords—Digital Mixed-Signal Verification; Real-Number Modeling, SystemVerilog User-Defined Nettype , EEnet, UVM, Power Regulation, Loading Effects

I. INTRODUCTION

Behind every embedded processor there is a power management system that must work reliable and efficient for the integrity of the whole system. The complexity of power management systems continues to grow not only to meet the demanding performance and safety requirements in the market but also to support new low-power design techniques, multiple power domains and diverse operation modes. To guarantee correct system functionality, an exhaustive functional verification must be performed to cover e.g. startup sequences, low-power transitions, interdependencies with other infrastructure blocks, and the robustness against load jumps caused by system activities. All of them involve close interaction between the analog and digital circuits given the mixed-signal nature of the power management circuits. Verification environments need to handle analog and digital circuits in a mixed-signal simulation, should have affordable simulation runtimes, be reusable across several hierarchies and follow state-of-the-art verification flows like the Universal Verification Methodology (UVM).

A. Mixed-Signal Simulation: Runtime matters

Analog Mixed-Signal (AMS) simulations use spice models to represent the analog circuits. They are accurate but the performance impact is significant when the circuit involves hundreds of elements and nodes interacting with each other. The analog part becomes often the bottleneck in simulation performance. These runtime penalties might lead to:

- an increased need of simulation computational resources,
- a compromise on quality of the verification by reducing the number of functional tests,
- an over-simplification of the whole analog part which does not represent properly its structure.
- or to an extension of cost and project schedule.

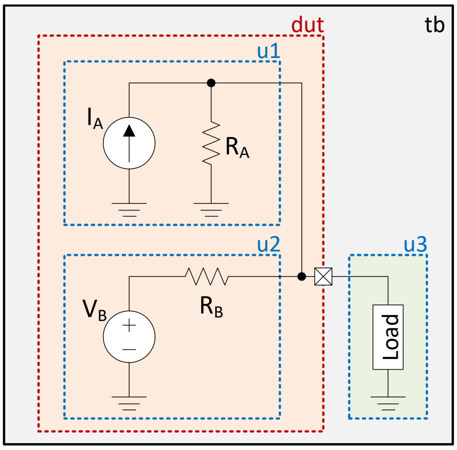
In order to speed up the simulation at the cost of accuracy, Digital Mixed-Signal (DMS) simulations use time-discrete real-number (RNM) behavioral models of the analog circuits that run on event-driven digital simulators. Eliminating the need of slow analog simulation and convergence issues allows simulation of whole big scale SoC designs in less time.

B. Challenges in Real-Number Modeling

Most of the RNM modeling nowadays is made in Verilog-AMS wreal net type. This scalar net type includes resolution functions for the multiple drivers, something that is not possible with real variables in Verilog. Scalar representation is enough to represent signal properties as either voltage or current, but not both [1]. This is a big limitation when modeling loading effects which require voltage, current and impedance, suggesting the need of a structured net type. Figure 1 shows an example for such a circuit.

A clear and simple practical example of a circuit functionality requiring modeling of loading effects is charging an off-chip capacitor through diverse drivers inside the device like a pull-up resistor and a low dropout (LDO) voltage regulator, all of them driving the same net but spread across different design hierarchies.

Figure 1 Example of a circuit modeled hierarchically requiring a structured net type for load modeling.



Structured net types are available in VHDL RNM; however, the language has limitations with the coercion of wire to wreal and with the connectivity from real to electrical types [2]. These limitations have been overcome by the introduction of the User-Defined Nettype (UDN) and the explicit interconnects in SystemVerilog IEEE 1800-2012 [3].

This methodology offers the capability to model all drivers and loads involved in the power regulation of a power management system to enable interaction of the multiple drivers and loads. This fills the gap in verification only covered before by expensive AMS simulations.

II. Modeling Loading Effects with SystemVerilog UDN

A. EEnet, a SystemVerilog UDN for Electrical Equivalence

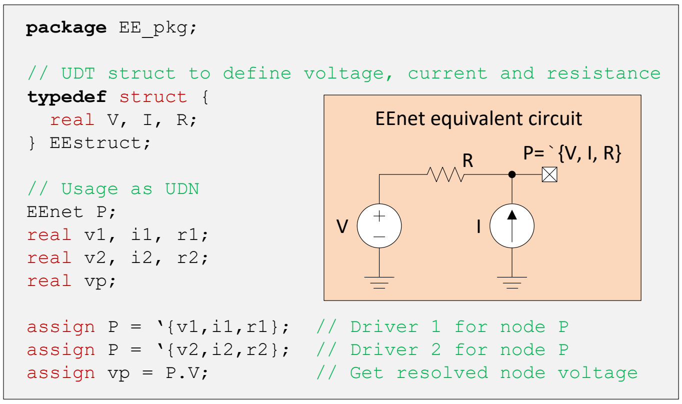
Cadence introduced the EEnet package with the EEnet SV-UDN that combines the structured User-Defined Type (UDT) *EEstruct* with three fields: voltage, current and series resistance; and the User-Defined Resolution (UDR) function *res_EE* that resolves the multiple drivers on the same net by following Kirchhoff's law. The circuits are modeled using a combination of Thevenin and Norton equivalents for each EEnet driver. Some of the benefits and applications of EEnet modeling have been presented in [2] and [4].

Figure 2 shows the representation of the EEnet equivalent circuit and the SystemVerilog code for the UDT and its usage. Depending on the values of the different fields, it results in real or ideal current or voltage sources or a resistive load.

The EEnet package was selected because it fulfills all requirements for the selected modelling approach. Nonetheless, it is fully compliant with SystemVerilog 1800-2012 and the same principle can be followed to create a custom UDN.

The modelling approach was used in [5] to create power-aware EEnet models of common building blocks involved in voltage regulation like capacitors, inductors, load currents, charge pumps, LDO's and Power FET's. All of these circuits are then modeled as Thevenin and Norton equivalents.

Figure 2 Representation of the EEnet equivalent circuit.



```
package EE_pkg;

// UDT struct to define voltage, current and resistance
typedef struct {
  real V, I, R;
} EEstruct;

// Usage as UDN
EEnet P;
real v1, i1, r1;
real v2, i2, r2;
real vp;

assign P = '{v1,i1,r1};  // Driver 1 for node P
assign P = '{v2,i2,r2};  // Driver 2 for node P
assign vp = P.V;         // Get resolved node voltage
```

B. *Known Limitations of EEnet*

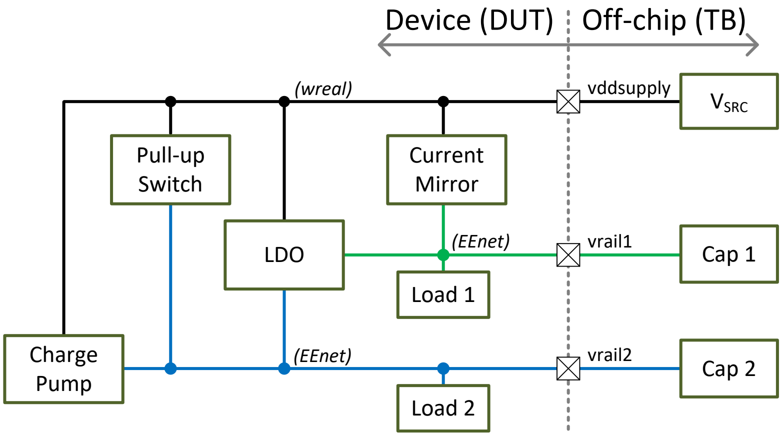
Known limitations of the EEnet package are:

- Best suited for node to ground representations but with restrictions for node to node connections.
- In case of feedback loops, changes in the contributors need to be clocked or have some tolerance in order to reach convergence and avoid infinite iterations in the resolution function.
- Automatic insertion of connect modules for interaction with other net types is up to the simulator vendor. In case that they are not available, custom connect modules have to be created and placed manually in the design.

C. *Case Study of a Power Regulation Circuit and EEnet Models*

Figure 3 shows the block diagram of two power rails in a generic power management system. This will serve as the case study to show the EEnet models and provide a context for the verification environment.

Figure 3 Sample block diagram of a power regulation circuit.

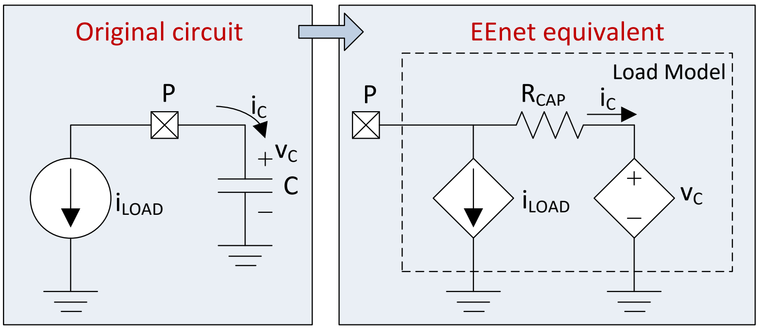


1) Load Model: System Load and External Capacitor

The load model is made of a passive and an active load. The passive load represents a big off-chip capacitor to be loaded with current from the system. The active load represents current consumption caused by the activity of the components supplied by the rail. The load model is placed in the testbench to monitor the rail voltage and to emulate the system load.

Figure 4 shows the EEnet model of the load. The active load is a current source and the capacitor is modeled as a voltage source depending on the discrete integration of its current.

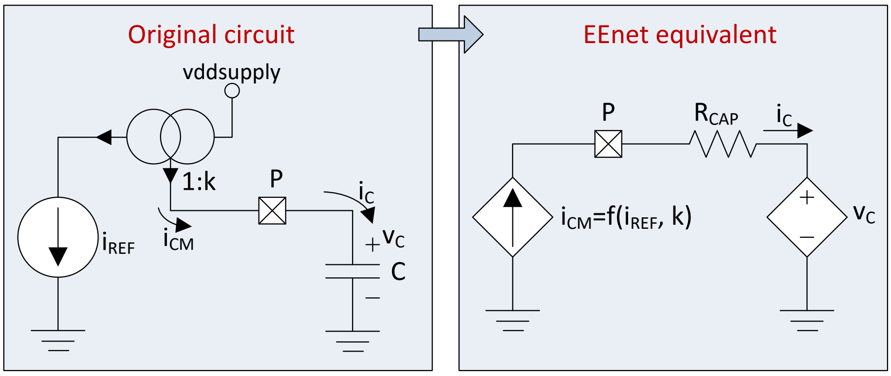
Figure 4 Electrical circuit and equivalent EEnet representation of the system load and the external capacitor.



2) Current Mirror

The current mirror is used to load a big capacitance up to the supply voltage. It is simply modeled as an EEnet current source as shown in Figure 5. Nonlinearities like reducing the current when reaching the supply voltage need to be considered and can be implemented in EEnet without any problem.

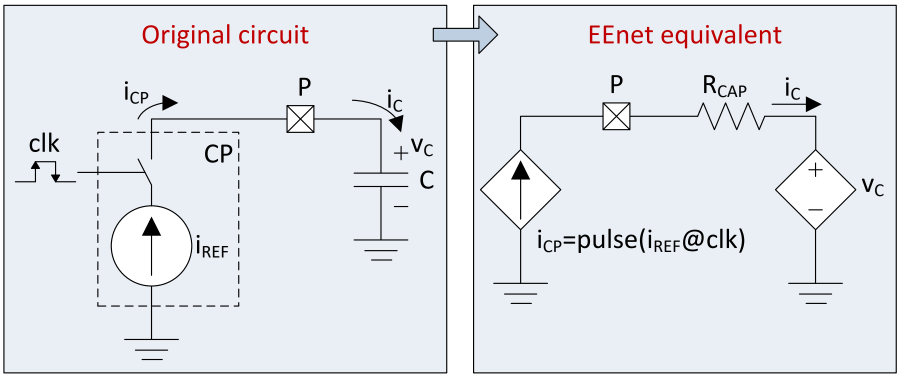
Figure 5 Electrical circuit and equivalent EEnet representation of the current mirror.



3) Charge Pump

The charge pump is also a current source used for loading a big capacitance but beyond the supply voltage by generating short pulses of current. The EEnet equivalent as shown in Figure 6 is a current source with a fixed pulse after each toggling of the control input.

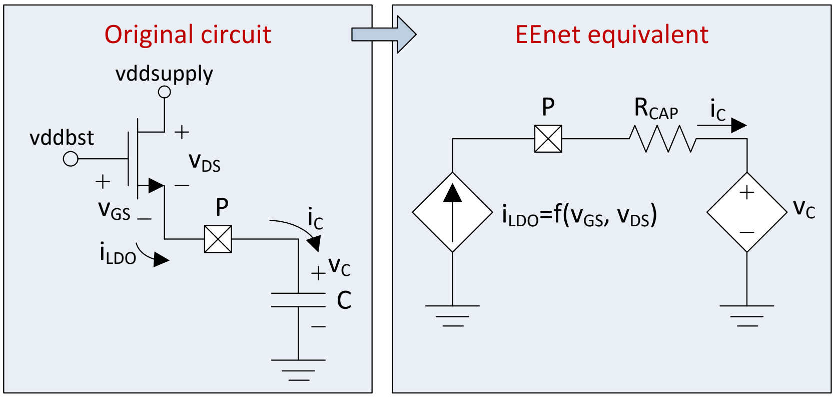
Figure 6 Electrical circuit and equivalent EEnet representation of the charge pump.



4) LDO

The LDO is a DC linear voltage regulator. The LDO output current depends not only on the supply voltage and the gate voltage but also on the LDO output voltage itself coming from the external capacitor. This feedback of the generated output voltage needs to be considered in the EEnet model. To avoid unlimited recurrence in the resolution function a voltage and a current tolerance needs to be established. Figure 7 shows that the EEnet equivalent is reduced to an ideal current source depending on the other voltages. The non-linear dependency between the current and the other voltages can be modeled with an equation or with a table model.

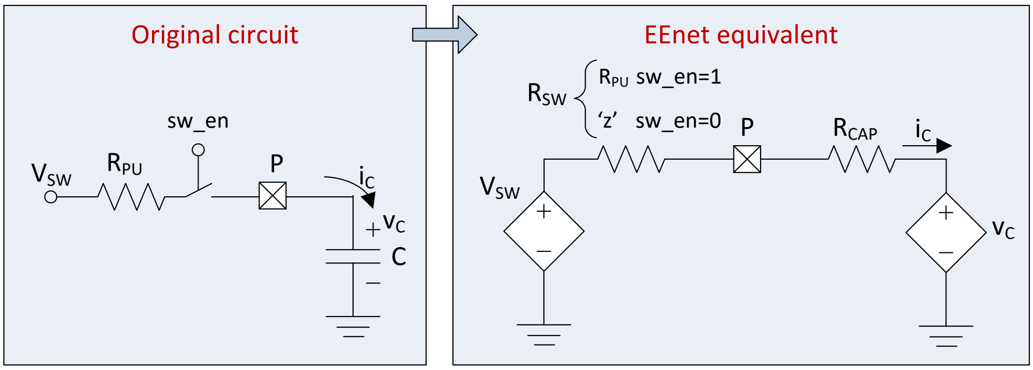
Figure 7 Electrical circuit and equivalent EEnet representation of the LDO.



5) Pull-up Switch

The pull-up switch is used in this circuit for fast charging of an external capacitance up to the supply level. The driver is modeled as a voltage source with series resistance controlled by the switch enable signal as shown in Figure 8.

Figure 8 Electrical circuit and equivalent EEnet representation of the pull-up switch.



III. The Mixed-Signal Verification Environment

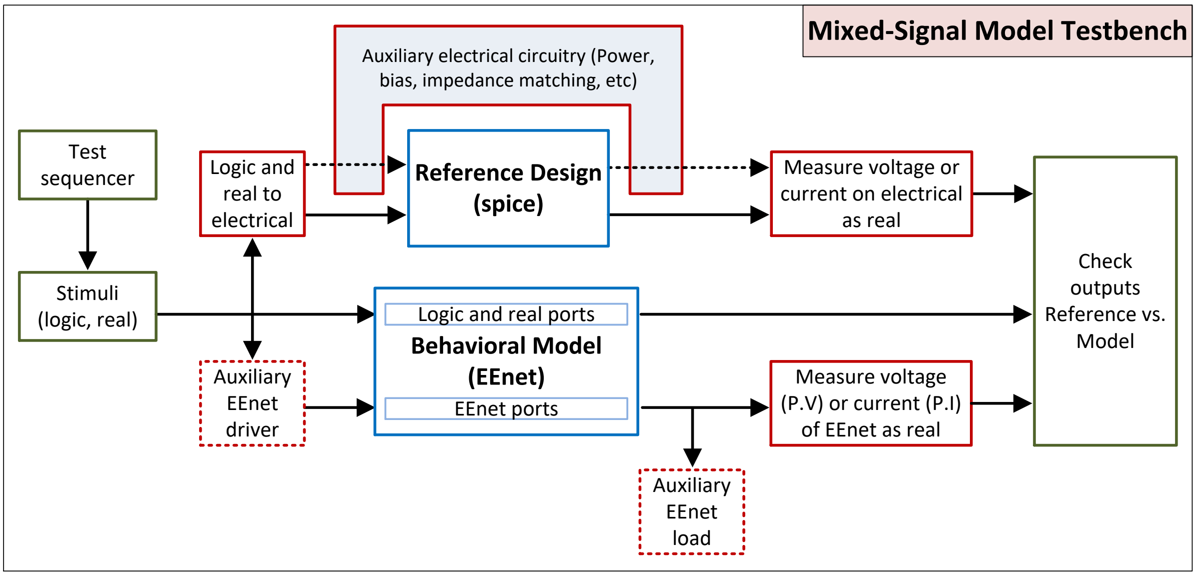
A. Model Verification

The correct functionality of newly developed models gets pre-verified in standalone AMS model testbenches. Each model is compared against the transistor-level analog circuit to guarantee a reasonable quality of the individual sub-circuits against the expected behavior.

Figure 9 shows the structure of these mixed-signal testbenches instrumented with auxiliary blocks to not only handle the classical electrical, logic and real signals but also the EEnet signals. All this thanks to wire coercion and to the proper connect module instantiation.

The combined circuit functionality of the models gets verified within the higher level verification environment which is also used for the later sign off of the overall circuit.

Figure 9 Block diagram of a mixed-signal model testbench to validate the EEnet model against the reference design.


Mixed-Signal Model Testbench
Auxiliary electrical circuitry (Power, bias, impedance matching, etc)
Test sequencer
Logic and real to electrical
Reference Design (spice)
Measure voltage or current on electrical as real
Check outputs Reference vs. Model
Stimuli (logic, real)
Logic and real ports
Behavioral Model (EEnet)
EEnet ports
Auxiliary EEnet driver
Measure voltage (P.V) or current (P.I) of EEnet as real
Auxiliary EEnet load

B. *Mixed-Signal UVM Testbench for IP/SoC*

The verification environment was developed in SystemVerilog UVM [6]. It offers different mixed-signal configurations for low-power DMS, AMS and AMS co-simulation, combined with RTL and gate-level sources.

The verification components use real signals to control the drivers for the supply voltages and the rail loads, as well as the monitors for the voltage rails, reference voltages and reference currents. The testbench does not need to directly manipulate EEnet signals; this happens only over the EEnet load models.

For exhaustive verification the testbench randomizes supply voltages and load scenarios. It also emulates different system power states and creates system state transitions and events. The verification environment is fully reusable over several simulation modes and allows fast sign-off of the design circuit via regressions runs.

IV. Conclusion

The capacity to simulate load jumps and driver interaction in DMS and the faster bring up of simulations compared to AMS helped to reach higher quality in shorter development time, especially for big scale designs like mixed-signal microcontrollers. On the one hand, it helped digital and analog designers to proof concepts and find integration issues much earlier than before. On the other hand, it enabled the verification team to extend functional coverage by checking more scenarios in DMS thus reducing effort and time for AMS, leaving only a selective number of tests to check over corners.

Key benefits:

- Enormous speedup of simulation time compared to AMS simulations.
- Load modeling with SV EEnet enabled novel simulation of interactions between different types of drivers and loads in a power management system.
- Methodology improved quality of the product by extending functional coverage in DMS and facilitating proof of concepts in an early stage.
- Methodology also reduced overall project development time by leveraging AMS effort into the DMS domain.

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