

Efficient Standard Co-Emulation Modeling Interface (SCE-MI) Usage to Accelerate TBA Performance

Ponnambalam Lakshmanan

Analog Devices, Bengaluru, India





- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion





- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion





- Hardware assisted acceleration offers better performance over software simulation.
- Hardware assisted acceleration techniques:
 - Signal Based Acceleration (SBA)
 - Transaction Based Acceleration (TBA)
 - Embedded testbench
 - Vector Based Acceleration (VBA)
 - In-circuit Emulation (ICE)



Transaction Based Acceleration

- Traditional testbench is split into two domains
 - Non-Synthesizable domain
 - Runs on simulator
 - Synthesizable domain
 - Runs on emulator





- Various factors directly affect the emulator performance
 - Inefficient usage of SCE-MI
 - Behavioral constructs (Not purely-synthesizable)
 - Memory Handling
 - Amount of code running on simulator and emulator
 - Simulator Emulator synchronizations



- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion





- Standard Co-Emulation Modeling Interface (SCE-MI) is an Accellera standard
- Communication interface between BFM and proxy
- Different types of SCE-MI use models:
 - SCE-MI Pipe based interface
 - SCE-MI Direct memory interface (DMI)
 - SCE-MI Function based interface



- Salient Features:
 - Unidirectional
 - Batching
 - Buffering
 - Flushing
 - Data shaping



- Blocking and Non-Blocking constructs



- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion



Initial Architecture Challenges



2017

RENCE AND EXHIBITION

UNITED STATES

DESIGN AND VERIFIC



- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion





Optimizing SCE-MI Pipe Usage

• Merging SCE-MI pipes

Challenge		Solution
Behavioral evals with every SCE- MI access	•	Send data via a single SCE-MI pipe. Static SCE-MI pipe - Bit vectors Dynamic SCE-MI pipe - Array of data







Synchronous access

	Challenge	Solution
•	Asynchronous mode creates significant behavioral evals	Synchronous mode of SCE-MI pipe IS_CLOCKED_INTF = 1

Code Snippet scemi input pipe #(.BYTES PER ELEMENT (20), .PAYLOAD MAX ELEMENTS(1), VISIBILITY MODE(2). .IS CLOCKED INTE(0)) inbox (clk);

Code Snippet scemi input pipe #(.BYTES PER ELEMENT (20), .PAYLOAD MAX ELEMENTS(1), VISIBILITY MODE(2). .IS CLOCKED INTF(1)) inbox (clk);



• Optimized data transfer

Challenge	Solution		
Accessing more than one element per access results in behavioral evals	If the intention is to access 5 Bytes per call then set		
 PAYLOAD_MAX_ELEMENTS = 5; BYTES_PER_ELEMENT = 1; 	 PAYLOAD_MAX_ELEMENTS = 1; BYTES_PER_ELEMENT = 5; 		





Minimal Synchronization

Challenge	Solution
 Frequent data transfer causes the emulator to halt frequently Results in degraded acceleration 	 Accumulate multiple bytes of data and transfer at once Try to buffer the elements Avoid unnecessary flush() usage

Code Snippet

scemi_input_pipe #(
.BYTES_PER_ELEMENT(20),
.PAYLOAD_MAX_ELEMENTS(1),
.BUFFER MAX ELEMENTS (10) ,
.VISIBILITY_MODE(2),
.IS_CLOCKED_INTF(1)) inbox (clk);



Clearing the pipe

	Challenge		Solution
•	Discarding buffer contents on reset No inbuilt functions Increase in step-count	• (Use the fastest clock available to synchronously fetch data from pipe

Code Snippet : Before			
always@(posedge clk, posedge rst) begin if(rst) begin // Statements			
<pre>for(int i=0, i<20), i++) inbox.receive(1,ve,data,eom);</pre>			
end			
else begin			
// statements			
end			
end			

```
Code Snippet : After
always@ (posedge fst_clk, posedge rst) begin
if(rst) begin
rst_buff = 1;
// statements
end
else begin
if(rst_buff && !eom)
inbox.receive(1,ve,data,eom);
else
rst_buff = 0;
end
end
```



- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion





- Software side interface to perform backdoor read/write operations on hardware side memories
- Types of interfaces
 - Block interface
 - Word interface
- Performance Improvement:
 - HW-SW synchronizations reduced by ~50%
 - TBA run time decreased by >25%



SCE-MI Direct Memory Interface

UNITED STATES

DESIGN AND VERIFICATION

2017





- Adopts SystemVerilog Direct Programming Interface (DPI) concept.
- End user is required to implement all the functions
 No built in functions
- Used to configure BFM registers



DVCONFERENCE AND EXHIBITION SCE-MI Function Based Interface





- Factors
 - Increase in effort and time to implement complex functionality in a synthesizable format.
 - Increase in area occupied by the BFM on the emulator.
- Implement complex functionality that is utilized occasionally as a method in the C membrane and import/invoke from the BFM.



- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion









- Acceleration Concept
- Introduction to SCE-MI and SCE-MI Pipes
- Testbench Architecture and Existing Challenges
- Optimizing SCE-MI pipe usage
- SCE-MI Direct Memory and Function Based Interface
- Optimized Architecture
- Results and Conclusion



• TBA Performance improvement

land been such that	TBA properties				
Implementation	Gate count	Bevals	HW-SW Sync	TBA Time	
Pipe only	~2 M	18,299,173	4,728,998	~60 min	
Pipes only	~2 M	2 850 320	1 284 765	~35 min	
(Optimized)		2,009,020	1,204,703	~33 mm	
DMI + Function	~1 5 M	210	0.971	~1 min	
based Interface	~1.5 10	210	9,071	~4 11111	

Simulation v/s TBA run-time comparison for usecase

Simulation Time	TBA Time
~360min	~8min





- SCE-MI has multiple interfaces for different use cases
 - SCE-MI DMI used for backdoor read/write operation
 - SCE-MI Function Based Interface used to write into registers
 - SCE-MI Pipes are intended for streaming, variable length messaging, etc.
- HW-SW sync and Bevals could greatly deteriorate the performance of emulator.



- Efficient usage of SCE-MI helps in leveraging maximum performance from emulator resulting in handsome SPEED-UP.
- HW-SW syncs generated using vendor proprietary implementation
 - Number of syncs are kept to minimum.





- Porting to SOC environment and analyze the performance
- Explore UVM registers support decribed in SCEMI v2.3





- David Brownell, ADI
- Anilkumar T. S, Cadence
- Dr. Hans van der Schoot, Mentor Graphics





Questions



Ponnambalam Lakshmanan, Analog Devices