DESIGN & VERIFICATION DVCON 2014 CONFERENCE & EXHIBITION

Efficient SoC Level Mixed Signal Frontend Verification using Wreal Models

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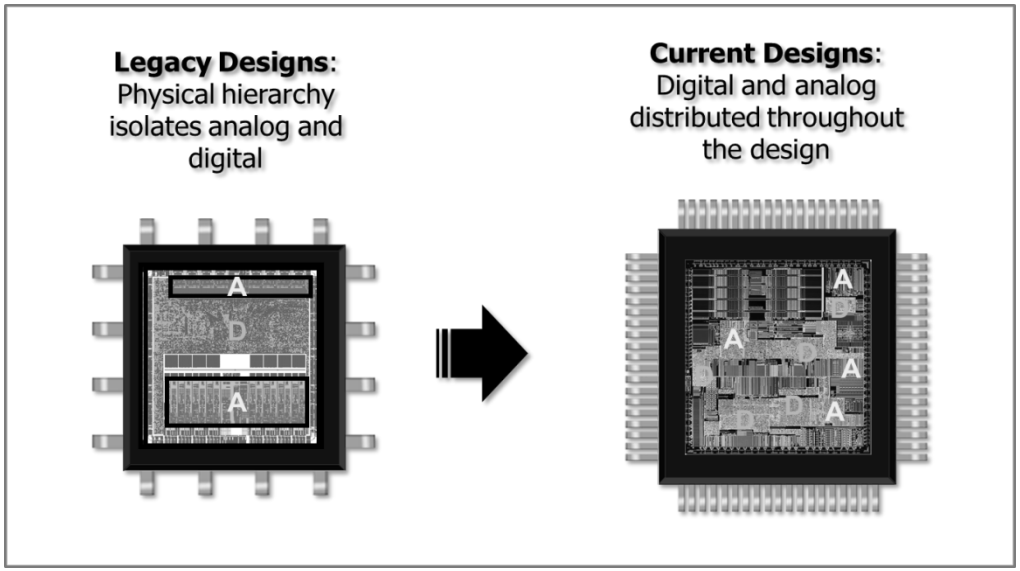
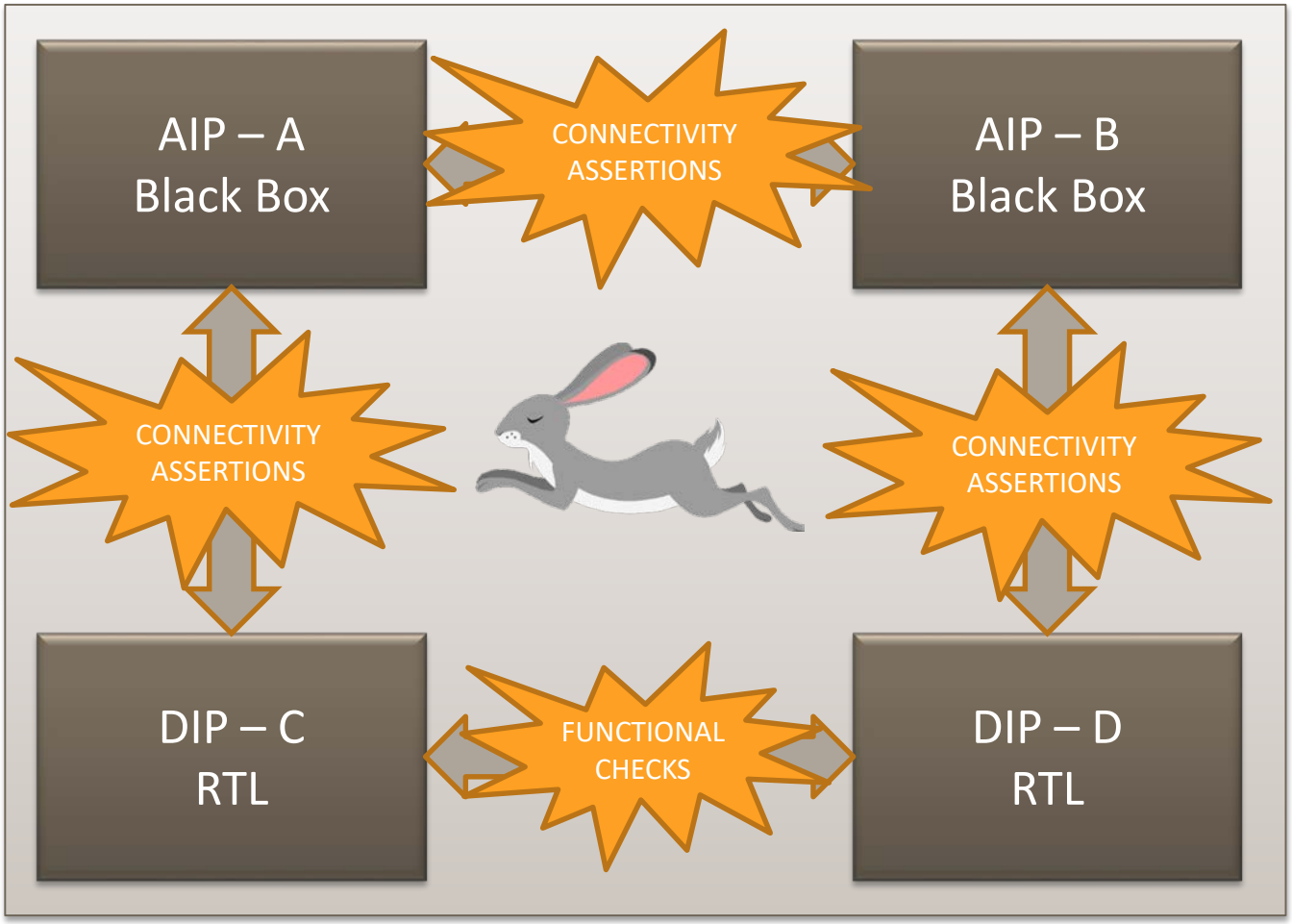
Introduction



- Tightly coupled Analog and digital blocks
- Mixed Signal SoC verification is becoming challenging
- Conventional black box/digital model verification → Inaccurate but fast!
- Conventional AMS verification → Accurate but too slow!
- WREAL based verification → +

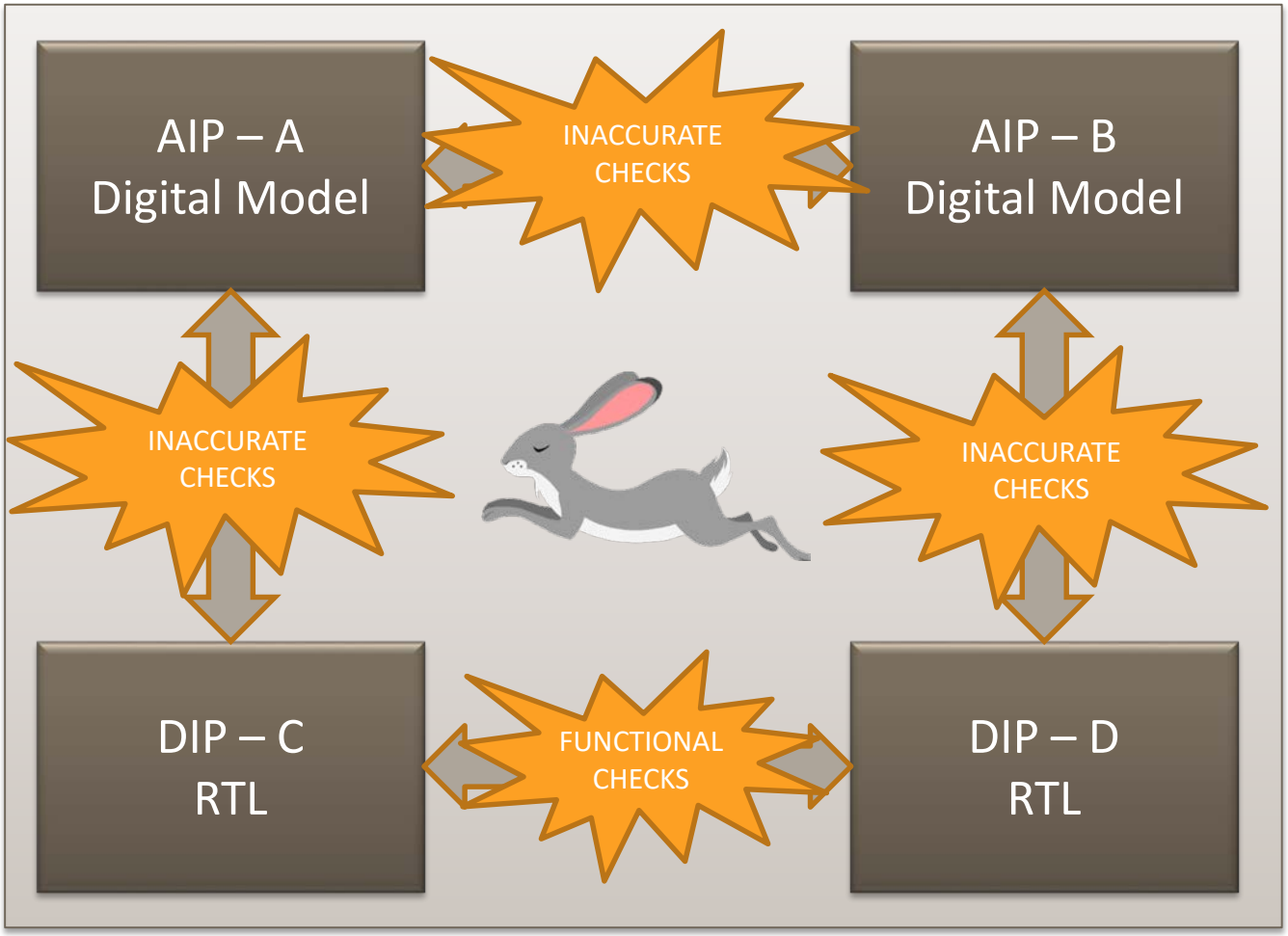
Conventional Methods (1/3)

- *Black Box Approach:* Analog modules are replaced with black boxes. Only connectivity assertions/checks are done.



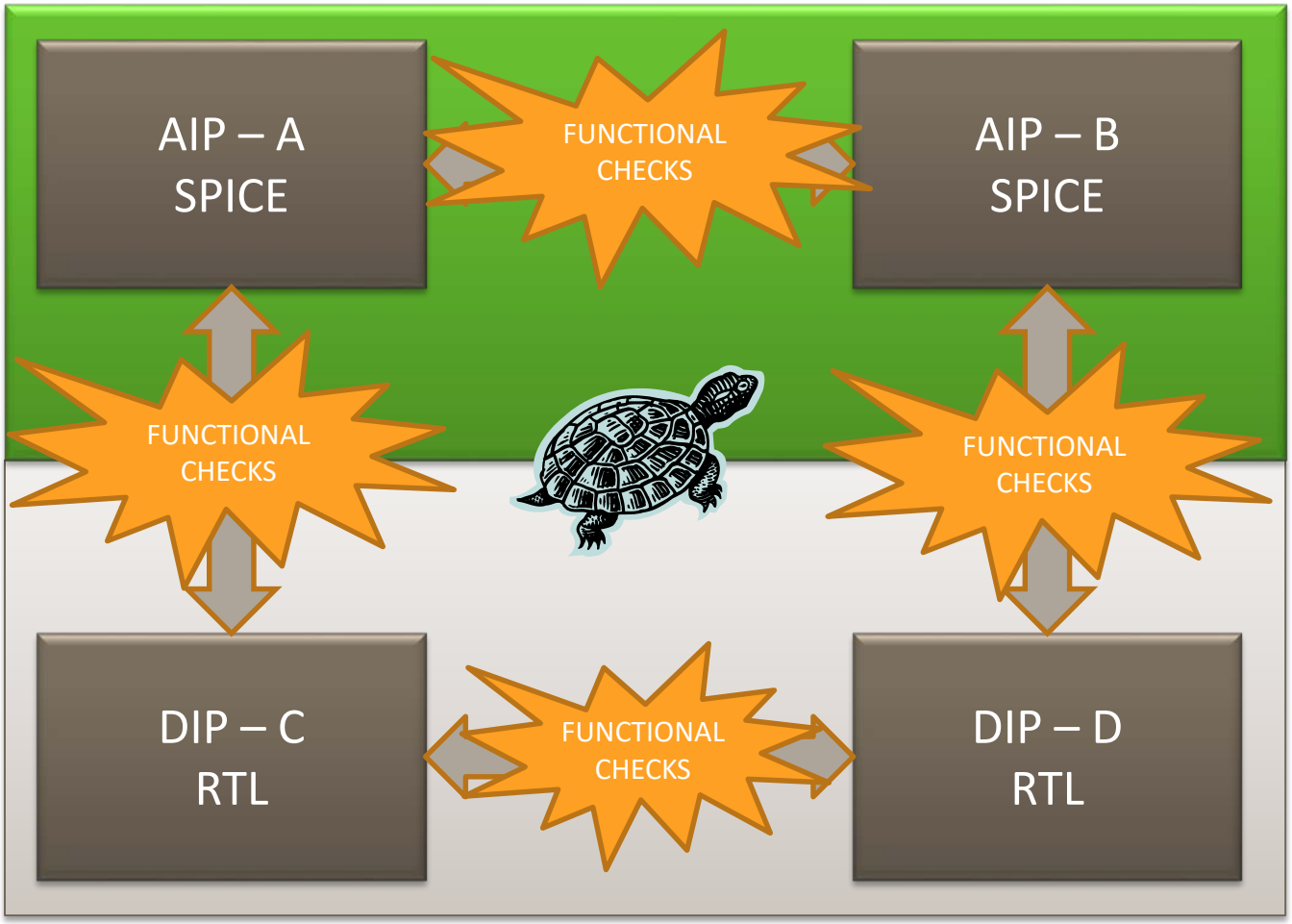
Conventional Methods (2/3)

- *Digital modeling:* Inaccurate models sufficient for very basic checks. There are no automated checks/verification possible.



Conventional Methods (3/3)

- *AMS Approach:* Very accurate mixed signal simulation with very high simulation times and extra license cost for the analog simulator



RVM (Real Value Models)

- Verilog/Verilog-AMS/VHDL
- RVM borrows concepts from analog and digital simulations
- The values are continuous like analog world
- Time is discrete like digital world
- Only digital engine solves the RVM system
- Higher simulation performance
- Interoperability with HVLs – SV and e language

Wreal Models

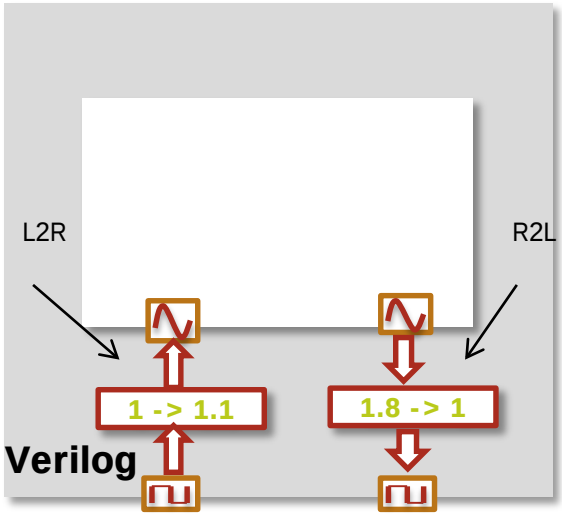
- RVM models coded in Verilog-AMS language
- Verilog-AMS supports a truly real-valued net/wire called "wreal.”
- Digital Mixed Signal (DMS) Verification

```
module A (i);
  input i;
  wreal i;
  real no;
    initial begin
     while (no < 10.0) begin
      #1 no = no + 0.1;
     end
    $stop
    end
  assign i = no;
endmodule
```

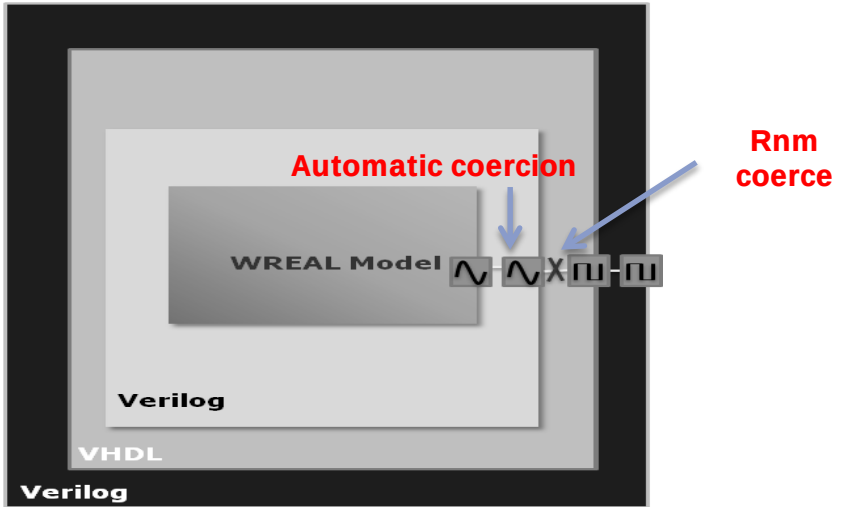
Sample wreal model code snippet

Key Wreal Features (1/2)

- Connect real to logic nets using automatically inserted Real2Logic-Logic2Real (R2L-L2R) connect modules.
- Automatic Wreal Coercion between Verilog and Wreal module to enable connecting wreal with logic
- Disabling coercion using rnm_coerce

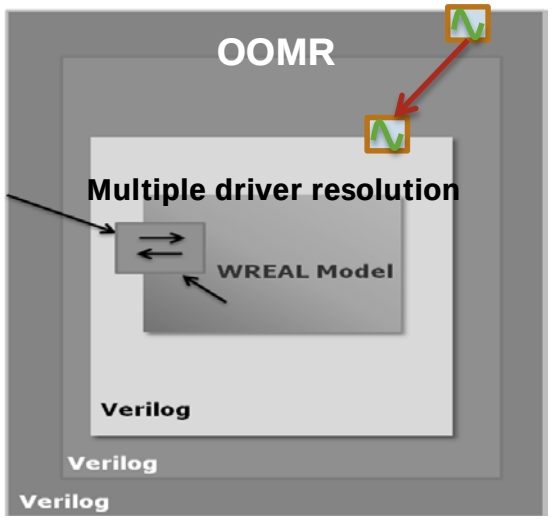


Multiple connect modules insertion



Key Wreal Features (2/2)

- Out Of Module Reference - OOMR
- WREAL multiple driver resolution
- Tracing drivers using TCL
- Support for wreal X and Z states
- Support for wreal arrays



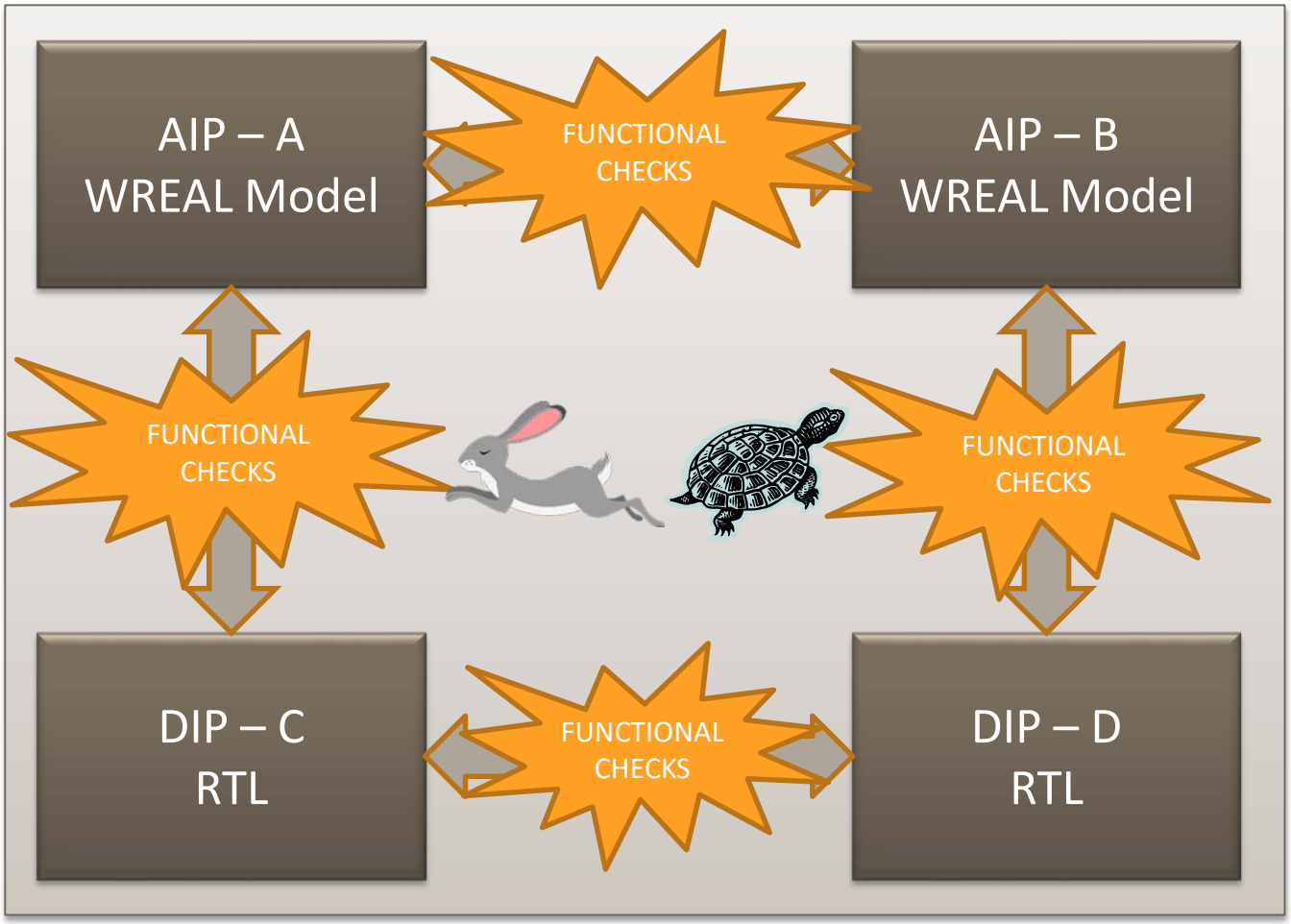

```
module ams_tb;
    wreal y[3:2];
    sub_design d1(y);
    initial begin
    #10 $display("%f,%f",y[2],y[3]);
    end
```

```
module top();
    wreal s;
    real r;
    foo f1 (s);
    initial begin
        #1 r = 1.234;
        #1 r = `wrealZState;
        #1 r = 3.2;
        #1 r = `wrealXState;
        #1 r = -4.2;
        #1 $stop;
    end
    assign s = r;
endmodule
```

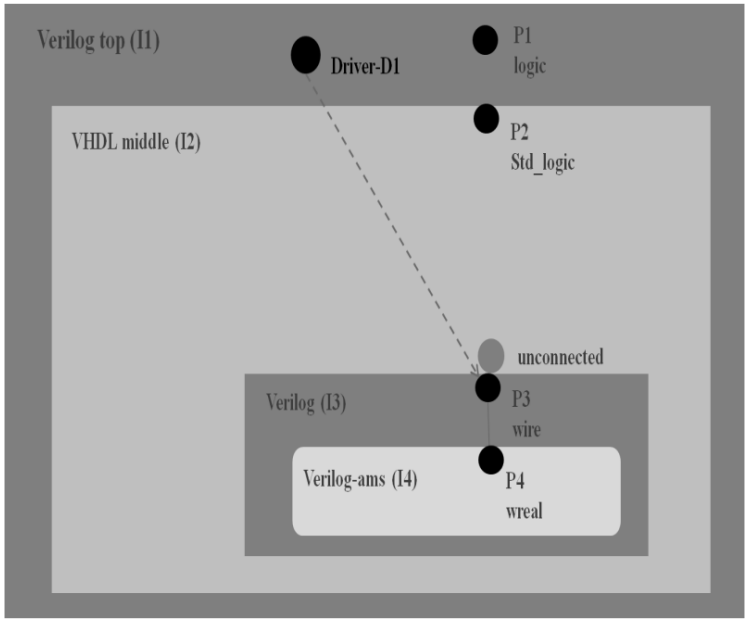
Benefits of using Wreal Model

- Generated/Coded and verified by the Analog IP team
- Models can be generated from the tool like - Virtuoso schematic model generator
- Ease of integration in SoC RTL sims
- Facilitates exhaustive verification of Analog – Digital interface
- Aids Test vector development for ATE (Automatic Test Equipment)
- Used seamlessly for GLS (Gate level Simulation) and PAGLS (Power-aware GLS)
- Nightly regression runs like digital simulations

Mixed Signal sims using WREAL



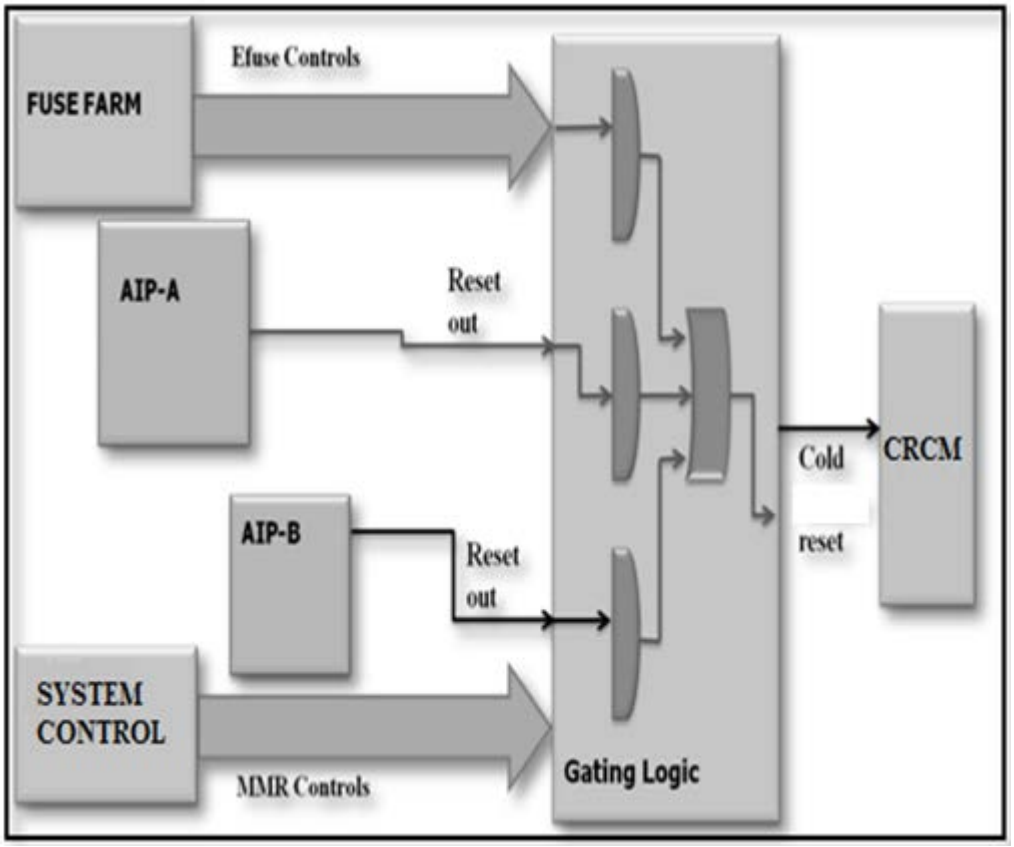
Wreal Based SoC Verification Setup



- Auto-coercion and connect modules enables easy setup
- ‘real’ voltages were driven to Analog IPs directly from the testbench using OOMR
- Complete module functionality including power up sequencing verified

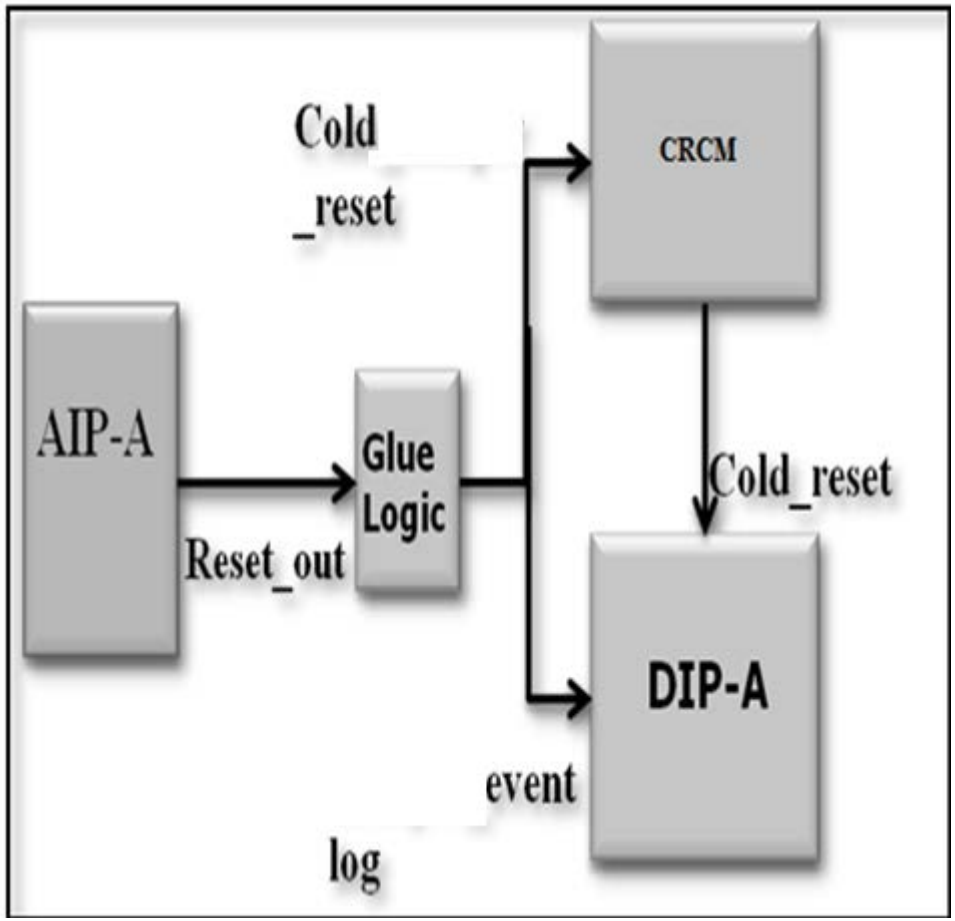
Key Bugs Found (1/3)

Bug: *Device will not boot if reset applied without power cycling. AIP_A reset_out sticky to chip Power on reset.*



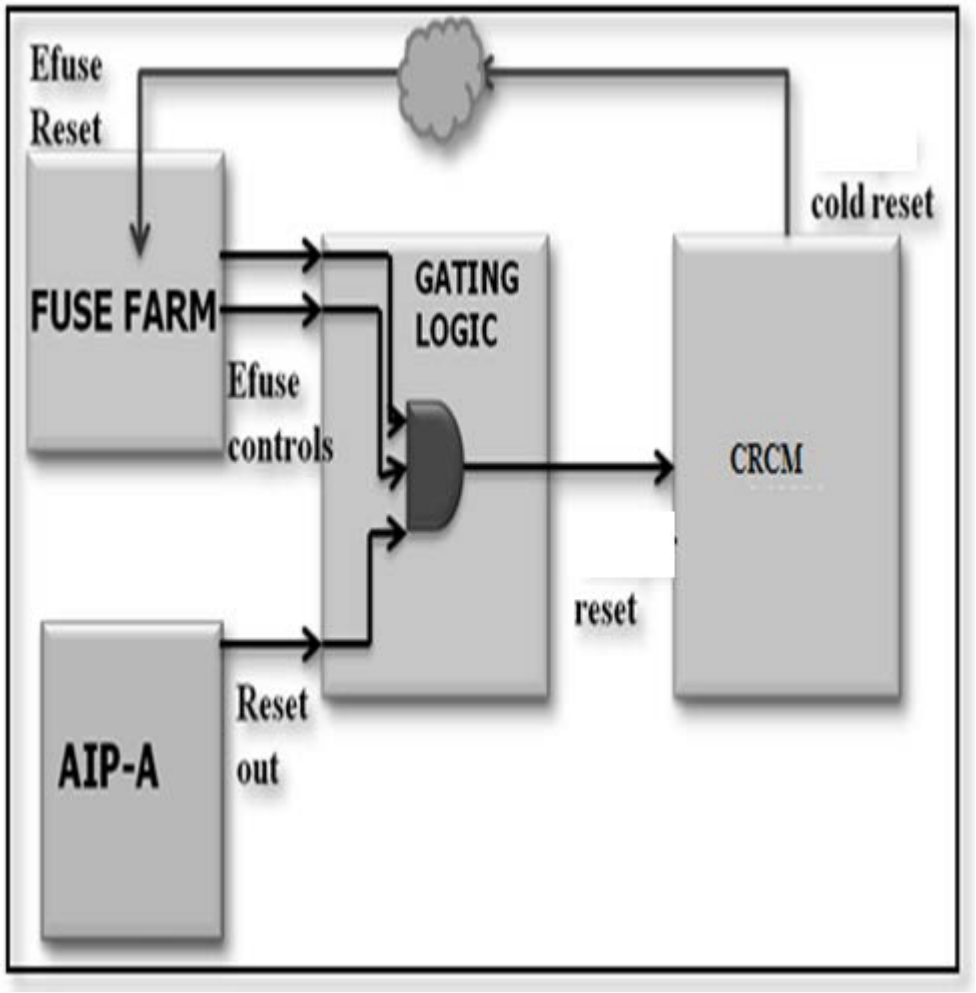
Key Bugs Found (2/3)

Bug: *Missing critical event logging leading to loss of key functionality*



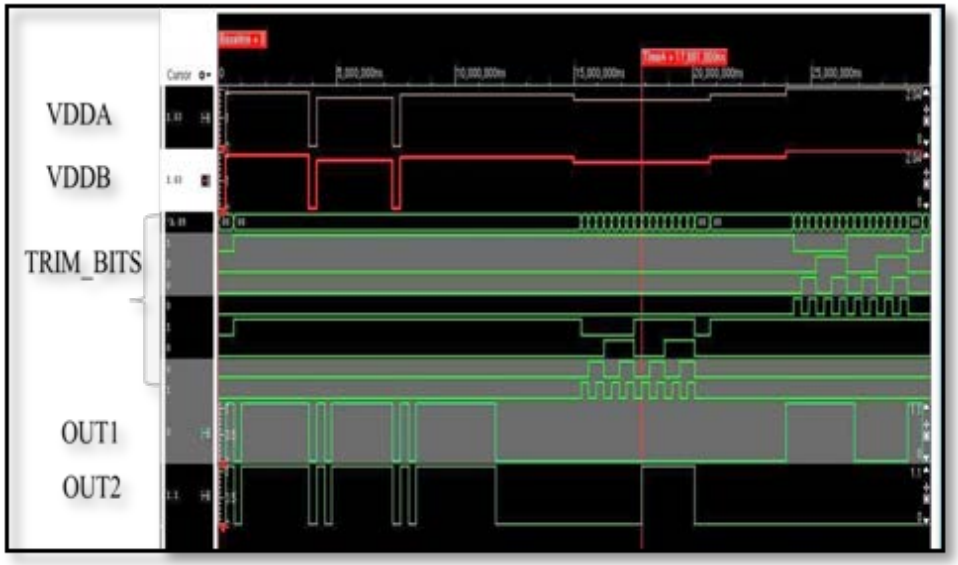
Key Bugs Found (3/3)

Bug: *Incorrect implementation of gating logic*

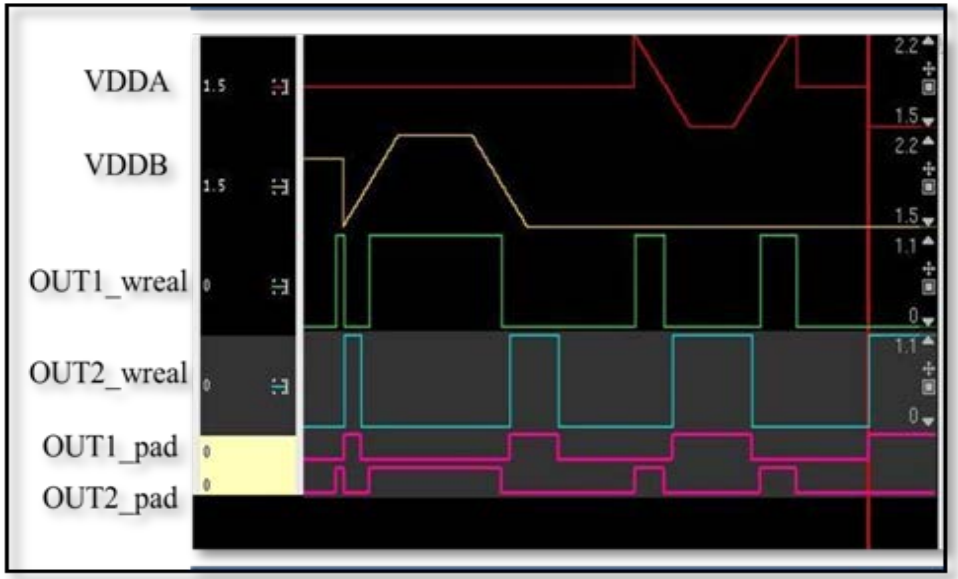


DFT verification

- **Analog Trimming:**
  - Trimming can be simulated with WREAL models



- **Threshold measurements:**
  - Measures output response to voltage ramps
  - Ramps Possible in a wreal verification environment.



Conclusion

- Seven bugs were caught on SoC early using these models
- 30% of DV test suite for a mixed signal subsystem used WREAL IP for functional verification
- Around 150 high quality test vectors were developed for analog DFT verification
- Efficient and easy solution for thorough mixed signal SoC verification
- Better quality of DV & DFT verification without significantly impacting the simulation speed

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THANK YOU