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DVCon Europe 2020

Welcome Message from DVCon Europe General Chair,
Joachim Geishauser
General Chair - NXP Semiconductors

A warm welcome to DVCon Europe 2020!

I am very pleased to welcome you to DVCon Europe 2020! This seventh edition of our well-established and expanding event centered around Design and Verification is indeed special - this year the venue is online and thus virtual!

As the steering team is driven by engineers, our aim is to provide attendees with a similar experience to a real-life conference, by introducing technologies such as virtual reality and 3D rendered venues. The experience will be different from attending a regular online conference, where you sit in front of your computer watching video streams with some verbal interaction, because we are introducing a 3D world where you 'walk around', listen in to some of the discussions in the hallways or have a talk to somebody at a (virtual) coffee machine.

The setup of this 3D virtual world was an interesting exercise. Despite the fact that there are many exciting interactive 3D games out there, there are a limited number of platforms that support virtual conferences in 3D. In the end we selected open source technology to extend our online conference with some novel virtual reality experience. This new challenge also showed that the steering team is assembled from true engineers, who like to explore new things, following the theme "from users for users".

Considering the overall virtual conference setup, the risk assessment on a 3D-only setup showed weaknesses and thus, in order not to put the conference in danger, a parallel setup was chosen. This means the papers, keynotes, panels and tutorial tracks run in a web-based framework and the virtual 3D world is running in parallel for the networking aspects and chats during the coffee breaks – we did not want to put the valuable work of our authors and presenters at any potential risk!

We hope the format will excite attendees (in the same way the steering team got excited) and will allow us to further expand the DVCon Europe family. We are proud that we have achieved this, together with you!

On the program side, a web-based setup allowed us to get more variety into the program by, for example, showcasing four key notes instead of two. We are proud that the DVCon Europe 2020 program hosts four luminary industry speakers from ARM, Intel, Veriest and Volkswagen, providing their perspectives on the digital transformation our industry is facing. This digital transformation continues to gain momentum and is changing our daily lives, changing the way we work, collaborate, communicate and commute.

As a common theme across the keynotes you will hear about how to develop and verify exciting new products, combining innovative hardware and software architectures. This requires unprecedent parallel hardware and software development, with a close interaction between the teams. The keynote speakers will be sharing their insights into the adoption of new methodologies and verification approaches and will discuss how the formerly separated disciplines of hardware and software are adapting to a new 'system thinking'.

Beside the keynotes, the 7th edition of DVCon Europe again offers a fully packed two-day technical program including tutorials, panels, posters, papers, and an attractive virtual 3D world to enable networking and interaction.

The SystemC Evolution Day is using the same framework as DVCon Europe, and thus is virtually co-located this year. The SystemC Evolution Day will happen one day after the DVCon Europe conference and will extend the topics into the SystemC space. More details can be found at the Accellera website.

The DVCon Europe steering committee and Accellera wish you a warm welcome at the virtual venue and an enjoyable DVCon Europe 2020!

Joachim Geishauser DVCon Europe 2020 General Chair

SYSTEMS INITIATIVE

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing

partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

» Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.

» Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.

» Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.

» Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.

» Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.

» Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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CONFlux Platform

This platform will be used for the following:

» Display DVCon Europe Schedule with live Zoom links to sessions

» Provide an attendee page and opportunity to contact fellow attendees

» Exhibit pages for all sponsors & exhibitors

» Live session recordings will be posted on the platform for viewing after the sessions take place
  • Posters will be displayed throughout the conference

» There will be opportunities to ask questions on presentations asynchronously so authors can respond throughout the conference

» Opportunities for chat sessions related to specific topics

» The platform will be accessible to registrants through November 23, 2020

Virtual Experience Rooms

DVCon Europe 2020 will bring you a true virtual experience by introducing Virtual Experience Rooms! These virtual rooms rendered in 3D are well known in the gaming industry, but not very popular yet to run conferences.

DVCon Europe 2020 will use these Virtual Experience Rooms for the poster session and to enable interaction, collaboration and networking during the 'coffee breaks' and encourage 'chatting' and discussing topics amongst the conference participants outside of the presentation sessions.

You can visit the following Virtual Experience Rooms during the event opening hours:

» SystemC Virtual Experience Room

» UVM Virtual Experience Room

» Portable Stimulus Virtual Experience Room

» Functional Safety Virtual Experience Room

» IP-XACT Virtual Experience Room

» Analog-Mixed-Signal Virtual Experience Room

» IP Security Assurance Virtual Experience Room

» SystemVerilog Virtual Experience Room

DVCon Europe will host the Virtual Experience Rooms on our own servers to guarantee performance. The URL to visit the Virtual Experience Rooms will be announced before the conference starts.

Visit this page for more information.

TIME (CET)	Stream 1	Stream 2	Stream 3	Stream 4	Other Events
8:30 - 9:00	**Opening & Welcome**				
9:00 - 10:00	**Keynote: I Like Being Surrounded by Good Ideas: Any Good Ideas We Can Borrow from the Software World?** Moshe Zalcberg, Chief Executive Office, Veriest Solutions				
10:00 - 10:30	**Virtual Coffee Break** Meet us in the Virtual Experience Rooms				
10:30 - 11:30	T1.1 Hybrid System Simulation Standards (I)	T2.1 C-S²QED: Gap-free Formal Verification of Processor Cores	T3.1 Cross-Level Compliance Testing and Verification for RISC-V	T4.1 Automotive Virtual Prototypes	
11:30 - 12:30	T1.2 Hybrid System Simulation Standards (II)	T2.2 Congestion Prediction: Deep Learning on Chip Design Enabling System	T3.2 Introduction to AI – Practical Overview to Get Started		
12:30 - 13:30	**Virtual Lunch Break** Meet us in the Virtual Experience Rooms				Virtual Experience Rooms & Virtual Exhibitors
13:30 - 14:30	**Panel: Assessing the Needs and Solutions for a Secure IC Supply Chain** Moderator: Paul Dempsey, Tech Design Forum				
14:30 - 15:30	**Keynote: The Benefits of Hardware DevOps** Victoria Mitchell, Vice President Systems Engineering, ARM				
15:30 - 16:00	**Virtual Coffee Break** Meet us in the Virtual Experience Rooms				
16:00 - 17:00	T1.3 Application Optimized HW/SW Design & Verification of a Machine Learning SoC Thank You to Our **Sponsor:** Mentor	T2.3 Meeting ISO 26262 Functional Safety Targets Through Static and Dynamic Fault Analysis Thank You to Our **Sponsor:** OPTIMA	T3.3 Beyond Bug Hunting: Verification Coverage from Safety to Certification Thank You to Our **Sponsor:** onespin		
17:00 - 18:00	T1.4 Boost your Productivity in FPGA/ASIC Design and Verification Thank You to Our **Sponsor:** Sigasi;	T2.4 Using Simulation Acceleration to Speed Block and Platform Level IP Verification Thank You to Our **Sponsor:** SYNOPSYS Silicon to Software	T3.4 Using Models to Shift-Left Verification and Enable Verification IP Re-use Throughout the Design Flow Thank You to Our **Sponsor:** MathWorks	T4.4 Analysis and Verification of safety critical E/E systems and circuits	
18:00 - 18:30	**Closure Day 1 & Outlook Day 2**				

TIME (CET)	Stream 1	Stream 2	Stream 3	Stream 4	Other Events
9:00 - 9:15	**Opening & Welcome**				
9:00 - 9:15	**Keynote: Challenges of a Sustainable Innovative Automotive Computing Architecture** Dr. Matthias Traub, Head of Architecture & Technologies, Volkswagen				
10:15 - 10:30	**Virtual Coffee Break** Meet us in the Virtual Experience Rooms				
10:30 - 11:00	P1.1 Does it pay off to add portable stimulus layer on top of UVM IP block test bench?	P2.1 A Methodology to Verify Functionality, Security, and Trust for RISC-V Cores	P3.1 Boosting Mixed-signal Design Productivity with FPGA-based Methods Throughout the Chip Design Process	P4.1 Enhancing Quality and Coverage of CDC Closure in Intel's SoC Design	
11:00 - 11:30	P1.2 Make your Testbenches Run Like Clockwork!	P2.2 Build Reliable and Efficient Reset Networks with a Comprehensive Reset Domain Crossing Verification Solution	P3.2 SOBEL FILTER: Software Implementation to RTL using High Level Synthesis	P4.2 Static Analysis of SystemC/SystemC-AMS System and Architectural Level Models	
11:30 - 12:00	P1.3 A Comprehensive Verification Platform for RISC-V based Processors	P2.3 Model-based Automation of Verification Development for automotive SOCs	P3.3 Single Source System to Register-Transfer Level Design Methodology Using High-Level Synthesis	P4.3 Bit density-based pre-characterization of RAM cells for area critical SOC design	Virtual Experience Rooms & Virtual Exhibitors
12:00 - 13:00	**Virtual Lunch Break** Meet us in the Virtual Experience Rooms				
13:00 - 14:00	**Poster Session** Virtual Experience Poster Rooms				
14:00 - 15:00	**Panel: Verification Challenges of an Exascale Supercomputer** Moderator: Jean-Marie Brunet - Mentor, A Siemens Business				
15:00 - 15:30	**Virtual Coffee Break** Meet us in the Virtual Experience Rooms				
15:30 - 16:00	P1.4 Mutable Verification environments through Visitor and Dynamic Register map Configuration	P2.4 Discovering Deadlocks in a Memory Controller IP	P3.4 Mixed Electronic System Level Power/ Performance Estimation using SystemC/TLM2.0 Modeling and PwClkARCH library	P4.4 Temporal assertions in SystemC	
16:00 - 16:30	P1.5 Facilitating Transactions in VHDL and SystemVerilog	P2.5 How To Verify Encoder And Decoder Designs Using Formal Verification	P3.5 Timing-Aware high level power estimation of industrial interconnect module	P4.5 Accelerating and Improving FPGA Design Reviews Using Analysis Tools	
16:30 - 17:00	P1.6 Lean Verification Techniques: Executable SystemVerilog UVM Defect Table For Simulations	P2.6 Using Formal to Prevent Deadlocks	P3.6 Clock Controller Unit Design Metrics: Area, Power, Software flexibility and Congestion Impacts at System Level	P4.6 Accelerating Automotive Ethernet validation by leveraging Synopsys Virtualizer with TraceCompass	
17:00 - 18:00	**Keynote: The Future of Compute: Verification in the Era of Heterogeneous Design** Dr. Mike Mayberry, Chief Technology Officer, Intel Corporation				
18:00 - 18:30	**Closing Session & Best Paper Awards**				

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Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design and Mixed-Language Simulation (VHDL, Verilog, SystemVerilog/UVM), FPGA-based Hardware-Assisted Verification, SoC and ASIC Prototyping, Emulation, Design Rule Checking, Clock Domain Crossing, VIP Transactors, Requirements Lifecycle Management, Embedded Development Kits, High-Performance Computing/Acceleration, DO-254 Functional Verification and Military/Aerospace solutions.

AMIQ EDA

AMIQ EDA provides tools – DVT Eclipse IDE, DVT Debugger Add-On, Verissimo Linter, and Specador Documentation Generator - that enable design and verification engineers increase the speed and quality of new code development, simplify legacy code maintenance, accelerate language and methodology learning, and improve source code reliability. Working with 100+ companies in 30+ countries, AMIQ EDA is recognized for its high quality products and customer service responsiveness.

CiRCUITSUTRA
TECHNOLOGIES

Reduce the Cost and Time to Market for your next SoC design. Visit CircuitSutra Virtual DVCon Europe 2020. Learn about advanced ESL methodologies for hardware-software co-design & co-verification

CircuitSutra is an Electronics System Level (ESL) design IP and services company, headquartered in India, having its offices at Noida, Bangalore and Santa Clara (USA). It enables customers to adopt advanced methodologies based on C, C++, SystemC, TLM, IP-XACT, UVM-SystemC. Its core competencies include Virtual Prototype (development, verification, deployment), High-Level Synthesis, Architecture & Performance modeling, SoC and System-level co-design and co-verification.

CircuitSutra's mission is to accelerate the adoption of ESL methodologies in the Industry.

CircuitSutra has the capability to setup world-class ESL project teams, to work as an extension of the customer's R&D team, either remotely through offshore development centre (ODC) model or onsite at customer location. We provide re-usable modeling IP & methodology, that helps customers to quick start their modeling projects. We also provide specialized SystemC trainings that helps customers to groom non-SystemC professionals to become virtual prototyping experts.

CircuitSutra is developing modelling infrastructure for the RISC-V ecosystem.

OneSpin Solutions is a leading provider of certified IC integrity verification solutions for functionally correct, safe, secure, and trusted integrated circuits. Headquartered in Munich, Germany, we partner with developers worldwide to assure the integrity of SoCs, ASICs, and FPGAs for automotive and industrial applications; defense; avionics; artificial intelligence and machine learning; consumer electronics; and communications. OneSpin's advanced solutions are based on our widely-used formal verification technology and are ideal for developing heterogeneous computing platforms, using programmable logic, and designing and integrating processor cores, such as RISC-V. OneSpin's commitment to our users' success fuels our mutual growth. OneSpin: Assuring IC Integrity.

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Optima Design Automation represents the next generation in automotive safety verification. The company has pioneered a new fault analysis technology for accelerated semiconductor development that enables a 1,000X performance improvement over traditional fault simulation. This platform powers the Optima Safety Platform that targets Hard and Soft Error analysis, essential in certifying the safe operation of automotive semiconductor devices to the ISO 26262 safety standard.

Qualcomm is the world's leading wireless technology innovator and the driving force behind the development, launch, and expansion of 5G. When we connected the phone to the internet, the mobile revolution was born. Today, our foundational technologies enable the mobile ecosystem and are found in every 3G, 4G and 5G smartphone. We bring the benefits of mobile to new industries, including automotive, the internet of things, and computing, and are leading the way to a world where everything and everyone can communicate and interact seamlessly.

Qualcomm Incorporated includes our licensing business, QTL, and the vast majority of our patent portfolio. Qualcomm Technologies, Inc., a subsidiary of Qualcomm Incorporated, operates, along with its subsidiaries, substantially all of our engineering, research and development functions, and substantially all of our products and services businesses, including our QCT semiconductor business.

Qualcomm has a Global Technology Centre in the beautiful harbour city of Cork located in the Republic of Ireland. This centre opened its doors in August 2013 and now has 300+ employees and growing. Qualcomm Cork has several teams across IT, HR and Engineering. Engineering teams work on Analog Mixed Signal, Security, Artificial Intelligence, Modelling, Validation, Design Automation, Automotive and Physical Design in parallel with other Qualcomm sites worldwide.

Live presentation from Qualcomm, 28th Oct, 12:00 to 13:00 CET:

Qualcomm Technologies Ireland – Success story and opportunities ahead

Sigasi;

Sigasi redefines digital design. Our design entry tool Sigasi Studio drastically improves hardware designer productivity by helping to write, inspect and modify digital circuit designs in the most intuitive way. Advanced features such as intelligent autocompletes and code refactoring make VHDL, Verilog and SystemVerilog design easier and more efficient.

Sigasi, founded in 2008 and headquartered in Belgium, has formed partnerships with FPGA and EDA companies including Altera, Xilinx and Aldec. The Sigasi Studio XPRT platform is used worldwide by industry leaders in the fields of healthcare, consumer electronics, industrial automation, telecom, aerospace and defense.

Veriest

Veriest is an international design house providing a range of professional engineering services. Veriest's client portfolio includes the full spectrum of globally-established industry leaders, defense companies, and early-stage startups developing high-end chip technology. Veriest's engineering teams in Israel, Serbia and Hungary include expert engineers in ASIC design, design verification, FPGA design, virtualization, embedded software and other technical domains.

For more information, please see the company's website at www.VeriestsS.com or info@ VeriestS.com and the company's Facebook and LinkedIn pages.

Jade
design automation

Jade Design Automation's mission is to accelerate the System-on-Chip (SoC) development for Internet of Things (IoT) applications. Addressing the key problems of hardware level device security, standard based on-chip buses and the increasing complexity of IP integration that companies need to get right for their IoT devices. We provide scale-able solutions from constrained IoT devices to rich IoT nodes to accelerate the time-to-market and time-to-security for SoC designers. Within the semiconductor industry we are working with blue-chip SoC companies covering the whole process from system architecture to board bring-up as well as design service companies offering system integration or full ASIC solutions and IP companies providing high quality IPs to SoCs.

8:30 – 9:00
Opening & Welcome

8:30 – 18:30
Virtual Experience Rooms & Virtual Exhibitors

09:00 – 10:00

Keynote: I Like Being Surrounded by Good Ideas: Any Good Ideas We Can Borrow from the Software World?

Speaker: Moshe Zalcberg
CEO of Veriest Solutions

Abstract: Many industries are undergoing a major transformation in the last years, but it seems the verification practice is still basically where it was decades ago, with very minor improvements since. On the other hand, new bigger projects enabled by the on-going Moore's law race, pose increasingly harder verification challenges – that our industry is struggling to keep up with.

It seems that our friends in the Software industry also face big challenges, but they have been introducing many and different approaches, methodologies, technologies to do things better.

This keynote presentation will discuss the challenge and review some possible ideas we may be able to borrow from our neighbors – and maybe some things we can contribute to them.

Biography: Moshe Zalcberg is CEO of Veriest Solutions, an international design house providing a range of professional engineering services. Veriest's engineering teams in Israel and Europe include experts in ASIC & FPGA design, functional/formal verification, virtualization, embedded software and other technical domains. Moshe has more than 20 years of experience in the semiconductor and design automation industries, having spent over 12 years of his career at Cadence Design Systems, as General Manager Israel, and European Director of Professional Services. He also served as GM Israel and VP of Business Development with Presto Engineering, a product engineering services company. Moshe is an Electrical Engineering graduate of the Technion Israel Institute of Technology and holds an MSc in Electronics and an MBA, both from Tel Aviv University.

10:00 – 10:30
Virtual Coffee Break
Meet us in the Virtual Experience Rooms

10:30 – 12:30
Tutorial Sessions

Tutorial 1.1 & 1.2: Hybrid System Simulation Standards (Workshop) Purposes, Practices, and Challenges for Interoperable Simulations

Time: 10:30 – 12:30 | Stream 1

Organizer:

Dr. Mark Burton, GreenSocs

As complexity increases, the requirements on simulation technology is broadening, especially in terms of interoperability.

This workshop is aimed at furthering the understanding of the different simulation standards used across various industrial domains and identifying the main challenges to ensure their interoperability.

Towards that goal, the workshop will provide an overview of the industrial usage and requirements of simulation in practise, and present the technical standards supporting them. This workshop will also be an opportunity to share our views and concerns about simulation standards and simulation interoperability, and to identify actions that could be taken collaboratively to address the challenge of Interoperable Simulation.

Agenda:

Introduction: **Mark Burton** (GreenSocs)
Accellera standards: **Martin Barnasconi** (NXP)
SMP standards: **Rachid Atori** (SpaceBel)
VHTNG/Airspace: **Jean Casters** / **Oliver Fourcade** (Airbus)
FMI/FMU: **Jean-Marie Gauthier** (Samares)
OpenADX: **Andreas Riexinger** (Bosch)
General discussion and Q&A
Conclusion: **Mark Burton** (GreenSocs)

Speakers:

Dr. Mark Burton, GreenSocs

Martin Barnasconi, NXP

Rachid Atori, SpaceBel

Jean Casters, Airbus

Oliver Fourcade, Airbus

Jean-Marie Gauthier, Samares

Andreas Riexinger, Bosch

Tutorial 2.1: C-S²QED: Gap-Free Formal Verification of Processor Cores

Time: 10:30 – 11:30 | Stream 2

Organizer:

Keerthikumara Devarajegowda, Infineon Technologies AG

In today's computer age, processor cores are ubiquitous in every electronic device. Electronic device suppliers build processor cores with a wide range of target applications. Some of these processors are custom built to target specific applications such as signal processing, graphics processing or central processing units that control the operations of a system. Recently, there has been a spike in the design and verification of highly customized processors to address the demands placed by internet-of-things (IoT), artificial intelligence (AI) and other advanced applications.

The processor cores perform computations (by executing instructions), store results and interact with the peripherals devices as specified by an application or a program. The circuitry of processor cores is highly optimized to meet non-functional metrics such as throughput, area and power consumption. Due to the complex nature of these processor cores, ensuring the functional correctness at pre-silicon stage becomes an enormous challenge. Formal verification (FV) exhaustively analyses the design state space and helps to find all logic bugs. However, ensuring that the design space is completely analyzed with a set of properties requires high formal verification expertise and involves laborious manual efforts. As a result, processor verification in industrial practice heavily relies on simulation-based methods, including software and hardware-assisted simulation.

Speaker:

Keerthikumara Devarajegowda, Infineon Technologies AG

Mohammad Rahmani Fadiheh, Technische Universität Kaiserslautern

Tutorial 3.1: Cross-Level Compliance Testing and Verification for RISC-V

Time 10:30 – 11:30: | Stream 3

Organizers:

Vladimir Herdt, DFKI GmbH Bremen

Daniel Große, Johannes Kepler University Linz

Eyck Jentzsch, MINRES® Technologies

RISC-V is an open and royalty-free Instruction Set Architecture (ISA) that gained enormous momentum in both academia and industry in recent years. The major goal of the RISC-V ISA is to provide a path to a new era of processor innovation via open standard collaboration. RISC-V became a game changer for embedded systems in several application areas including e.g. IoT and Edge devices. RISC-V features an extremely modular and extensible design that provides enormous flexibility in building application specific solutions that can leverage custom extensions and only include features that are really required. However, this enormous flexibility also leads to a significantly increased risk of introducing SW incompatibilities between different RISC-V implementations, thus causing fragmentation of the RISC-V ecosystem. This very important problem is addressed with compliance testing. More precisely, compliance testing checks whether registers are missing, modes are not there, instructions are absent, as well as the presence of only those instructions which are part of the selected ISA. If the compliance test passes for a CPU, the HW/SW contract is maintained and the SW will be portable between implementations. Note that compliance testing is not design verification. In contrast to compliance testing, the goal of verification is to find errors in the CPU implementation and ultimately prove that an implementation is correct. Thus, thorough verification has to be performed later in the development phase and is complementary to compliance testing.

In this tutorial we present a cross-level compliance testing and verification approach for RISC-V that brings together Virtual Prototypes (VPs) and Register-Transfer Level (RTL) designs. The main idea is to leverage the VP for test-case generation and comparison with the RTL design. A VP is essentially an abstract model of the entire HW platform and predominantly created in SystemC Transaction-Level Modeling (TLM). VPs are leveraged for SW execution early in the design flow and thus enable parallel development of HW and SW. Thus, SystemC-based VPs provide an industry-proven approach for analysis of complex HW/SW interactions (and other system-level use cases such as design space exploration or power/timing/performance validation). In addition, the VP serves as reference model for subsequent design flow steps. A central component of the VP is the Instruction Set Simulator (ISS), which is an abstract model of the CPU (and hence responsible to fetch, decode and execute instructions one after another).

For compliance testing we present two complementary approaches for test-case generation that target positive and negative testing. First, we present a specification-based approach for generation of high-quality compliance test-suites for positive testing. Starting point is a specification that essentially consists of two parts: a set of instruction constraints that describe valid instructions, and a set of coverage requirements that the final test-suite should satisfy. The specification is passed to a generator that leverages an SMT solver to automatically generate a test-suite that satisfies all constraints and coverage requirements. In addition, we present a fuzzing-based test-suite generation approach to complement the specification-based approach with negative testing. Therefore, we leverage state-of-the-art fuzzing techniques (based on LLVM libFuzzer) to iteratively generate test-cases which are executed on a RISC-V ISS and guide the fuzzing process through the observed code coverage of the ISS. A filter is integrated between fuzzer and ISS to conservatively remove test-cases with infinite loops and platform specific details, to avoid spurious signature mismatches and to enable automated compliance testing. To further improve the fuzzing effectiveness, we incorporate a custom coverage metric and fuzzing mutator. In combination, our approaches offer a strong compliance testing framework. We found new bugs and mismatches in several RISC-V simulators including riscvOVPsim from Imperas, which is the official reference simulator for compliance testing.

To complement compliance testing, we present a cross-level co-simulation approach for verification. At the heart of this approach is an instruction stream generator that generates new instructions on-the-fly during the simulation. This enables a very efficient and comprehensive generation of instruction streams. We provide a testbench that feeds the generated instructions to the ISS and RTL core in a co-simulation based setting. The ISS and RTL core state is compared after each executed instruction in order to detect errors in the RTL core immediately when they occur. We evaluate our cross-level verification approach on the 32 bit pipelined RISC-V core of MINRES The Good Folk (TGF) Series.

Speakers:

Vladimir Herdt, DFKI GmbH Bremen
Daniel Große, Johannes Kepler University Linz
Eyck Jentzsch, MINRES® Technologies

Tutorial 4.1: Automotive Virtual Prototypes

Time 10:30 – 11:30: | Stream 4

Organizer:

Manfred Thanner, NXP Semiconductors

In this tutorial, we share our experience with deploying virtual prototypes in the automotive supply chain. We focus on the collaboration between semiconductors, Tier1, and OEMs as well as the enabling tool ecosystem.

We briefly outline the impact of virtual prototyping on the automotive development process and the required abstraction levels for the different virtual prototyping use cases. We outline the challenges of distributing virtual prototypes upwards through the automotive supply chain, with models and SW content becoming more complex in every step. Each of the presenters shares his experiences, covering aspects like modeling, Software development use-cases, as well as technological and organizational benefits and challenges.

We close with our perspective on the required close partnership and alignment along the development path to achieve a successful deployment of virtual prototypes in the automotive supply chain, enabling a "shift-left" and more productive collaboration across different teams and companies.

Speakers:

Manfred Thanner, NXP
Ingo Feldner, Bosch
Sacha Loitz, Continental
Ralph Schleifer, Car Software Organisation
Kevin Brand, Synopsys

12:30 – 13:30
Virtual Lunch Break
Meet us in the Virtual Experience Rooms

13:30 – 14:30
Panel: Assessing the Needs and Solutions for a Secure IC Supply Chain
Moderator: **Paul Dempsey,** Tech Design Forum

Panelists:

John Hallman - OneSpin Solutions
Adnan Hamid - Breker Verification Systems
Rick O'Connor - OpenHW Group
Perry Wobil - Intel
Vivek Vedula - Arm

There is ample evidence of counterfeit and fake electronic parts infiltrating the IC supply chain and being used in safety- and security-critical applications. The mil/aero industry has been concerned with the risk of hardware Trojans being inserted in third-party IP blocks and, therefore, IC designs for many years. In 2007, DARPA launched the TRUST in Integrated Circuits program, with the goal of developing technologies for use in military applications designed and fabricated under untrusted conditions.

The availability of trustworthy electronics is a prerequisite for innovation, from low-cost IoT devices to autonomous vehicles and critical infrastructure. Many countries have identified the IC supply chain as a national security concern beyond defense applications. As such, the semiconductor industry should develop processes and technology that provide objective and measurable evidence of trustworthiness. It is reasonable and desirable to expect that IP and SoC development organizations deploy state-of-the-art technology and processes dedicated to IC trust and assurance, and a critical component of this is the tools and methodologies employed in these processes.

Verification has evolved from functional test to include infrastructure, safety and now security assurance. Security assurance is particularly complex, given the broad range of vulnerability types, the numerous stakeholders within the supply chain, and the life cycle of hardware and software components.

Moderator Paul Dempsey and a panel of experts will discuss next-generation methods used to test IP blocks and encompassing systems to identify security weaknesses, vulnerabilities, and malicious logic. They will offer examples of verification flows that address trust and security challenges within the context of an implementable security strategy.

14:30 – 15:30
Keynote: The Benefits of Hardware DevOps

Speaker: Victoria Mitchell
Vice President, Systems Engineering, Arm

Abstract: At the macro level, innovation in product development methodologies track across product types—be that software, hardware, or systems—even if the catalyst for the innovation is different. Agile methods, which originated in software to improve estimation and schedules, are becoming more common in hardware IP as design teams realize the benefits of being able to quickly prototype a feature and get quality feedback sooner. Software Development Operations, or DevOps, originated from the need to update web systems at short notice, and sometimes even on "live" web servers – hence DevOps' emphasis on Continuous Integration and Continuous Deployment (CI/CD). CI and CD can be applied to hardware IP development, bringing benefits including a shift-left on quality as well as "making space" in engineering resource loading through automation that allows time to address technical debt and research new technologies. Examples of both Agile planning and DevOps will be shared, where these techniques are being used within Arm IP Product Group (IPG)'s Central Engineering in the development of Systems IP and Media Processors.

Biography: Victoria (Vicki) Mitchell leads at ARM the Central Engineering Systems Engineering group within IPG. Systems Engineering works with global Arm engineering teams and the Arm ecosystem in the development, analysis and verification of Arm systems, production of key Systems IP (such as bus interconnect, DMA, GIC, SMMU, Display Controllers, ISP), and the development of Arm testchips. Vicki joined Arm Ltd in Cambridge in 2018 as the VP of Technology Services Group, where her remit was to define, promote, and lead the transformational change program that will deliver a >2X improvement in operating cost and design efficiency through the use of cloud compute, machine learning, operational research / design analytics, and big data. She has continued to deliver that strategy after her transfer to Central Engineering Systems and relocation to Austin, TX in 2019.

Vicki has over 30 years' experience in low-level, systems software, the majority of which has been for semiconductor companies including Altera, Intel, Cirrus Logic, SigmaTel, and IDT. Vicki holds a BS in Software Engineering from Colorado Technical University and an MS in Data Science from Northwestern University.

15:30 – 16:00
Virtual Coffee Break
Meet us in the Virtual Experience Rooms

Tutorial 1.3: Application Optimized HW/SW Design & Verification of a Machine Learning SoC

Time: 16:00 – 17:00 | Stream 1

Organizers:

Russell Klein, Mentor Graphics

Today, many embedded systems embody algorithms that were originally developed as software on general purpose computers. For example, an audio wake-word recognition algorithm or a video object recognition program. However, due to application (product) constraints, these algorithms usually cannot be run as software on embedded processors – they simply will not meet the performance or power requirements of the system, the algorithm needs to be accelerated with greater power efficiency.

Transforming an algorithm from software to a fast and efficient hardware implementation is a challenging task. Ensuring that the functionality is not compromised as development progresses is critical. Often, not all of the algorithms are appropriate to be implemented in hardware, resulting in a need to design both the hardware and the software in concert.

This tutorial walks through the process of migrating an algorithm from generic software to a hardware implementation customized to the specific requirements of your system; making intelligent trade-offs between hardware and software along the way. It will explain the tools and techniques needed to go from "Software to Systems" and cover a broad range of solutions including simulation, emulation, prototyping and High-Level Synthesis to design and verify SoCs and the software that runs on them.

The tutorial will use an example algorithm of an AI/ML object classification accelerator that takes a live camera feed and overlays bounding boxes and labels of objects classified in the feed. It can classify 20 objects and will be implemented as a combination of hardware and a software application running on a complete embedded Linux stack. This tutorial will cover everything from traditional UVM RTL verification to complex HW/SW verification to running real AI workloads and integration with AI/Deep Learning Frameworks such as TensorFlow.

Speaker:

Russell Klein, Mentor, A Siemens Business

Thank you to our Sponsor

Tutorial 2.3: Meeting ISO 26262 Functional Safety Targets Through Static and Dynamic Fault Analysis

Time: 16:00 – 17:00 | Stream 2

Organizers:

Jamil Mazzawi, Optima

Meeting today's Functional Safety Targets is posing new challenges for design teams working on automotive and other safety-critical chips at all, ASIL-A to -D, risk levels.

Even the parts of the design with the lowest ASIL A and B safety goals need some level of analysis, such as sizing different failure modes and making sure the implemented safety mechanisms at least has reasonable coverage potential. For the most safety conscious ASIL-D designs, permanent fault requirements are very stringent, and transient fault analysis must also be considered.

Eliminating transient faults can require additional hardware, in the form of hardened flip flops, which increase power consumption and silicon area especially when applied across the device. With accelerated fault analysis and the judicious use of statistical and dynamic methods, it is now possible to carefully select the appropriate flips flops for hardening to achieve ASIL D metrics while minimizing the impact on silicon real estate and power consumption. This can make a dramatic difference to the overall specific for the final device.

This tutorial will first guide attendees through the use of high-performance static fault analysis and characterization methods for all ASIL levels. It will then turn its attention to transient fault inspection and demonstrate exactly the analysis required to produce this minimal set of hardened flips flops. Attendees will be provided a full overview of the use of these techniques that can potentially save weeks in their next ISO 26262 or other safety critical design.

Speakers:

Jamil Mazzawi, Optima
Nael Qudsi, Optima
Sesha Sai Kumar C.V, Optima

Thank you to our Sponsor

Tutorial 3.3: Beyond Bug Hunting: Verification Coverage from Safety to Certification

Time: 16:00 – 17:00 | Stream 3

Organizers:

Rob van Blommestein, (Organizer), OneSpin Solutions

Understanding verification coverage is critical for meeting IC integrity standards and goes well beyond detecting bugs in the design. Without proper verification coverage metrics, meeting strict safety standards and certification may not be achievable. Precise metrics indicate where there are gaps in verification and provide a clear view of the progress being made in the verification effort. Common simulation metrics are imprecise and only measure control coverage resulting in significant lack in verification quality. These remedial practices are time-consuming and leave undetected bugs that could significantly impact design safety. Mutation analysis takes the risk out achieving safety signoff. Results and accurate and reproduceable and creates reliable identification of verification gaps by highlighting over-constraining, dead and redundant code.

This tutorial will explore how mutation analysis can have a positive impact on the safety of your design and provide signoff confidence needed to achieve proper safety certification.

In addition, the tutorial will show how to achieve a meaningful integration of formal and simulation coverage metrics. A long-standing wish of many verification engineers and managers, coverage integration reduces effort overlap between simulation and formal, and enables faster, more rigorous signoff.

Speakers:

Nicolae Tusinschi, OneSpin Solutions

Thank you to our Sponsor

Tutorial 1.4: Boost your productivity in FPGA/ASIC design and verification

Time: 17:00 – 18:00 | Stream 1

Organizers:

Bart Brosens, Sigasi

Most EDA tools take your HDL code as a starting point and process it as efficiently as possible, focusing on the silicon. But those tools do not care about how you come up with this code in the first place.

If you want to be more productive as a hardware design or verification engineer working on VHDL, Verilog and SystemVerilog code, you deserve a software tool that helps you to create and explore code in a more efficient way. Lessons learned from designing complex software systems also apply to designing complex hardware systems.

In this tutorial, Bart Brosens (Application Engineer at Sigasi) will demonstrate how to increase your productivity using an IDE for your HDL design. You'll learn our best practices from proven methodologies such as:

- » Type-time feedback,
- » Intelligent content assist,
- » Various ways to explore and navigate through large projects,
- » How to effortlessly document your design
- » And much more.

Speakers:

Bart Brosens, Sigasi

Thank you to our Sponsor

Tutorial 2.4: Using Simulation Acceleration to Speed Block and Platform Level IP Verification

Time: 17:00 – 18:00 | Stream 2

Organizers:

Fabian Delguste, Synopsys

Design complexity growth has inspired new techniques to accelerate digital simulation of circuits by taking full advantage of high-performance verification platforms available. Latest techniques include fine-grained parallelism, which can significantly reduce simulation turn-around time by automatically partitioning the design to execute on multiple processor cores, and simulation acceleration, which accelerates the verification of block and platform level IP by integrating fast simulation with the specialized, high-performance hardware provided by fast emulation systems.

This tutorial reviews novel simulation acceleration technology for Synopsys VCS and how it will enable verification engineers to speed up the digital simulation of standard UVM testbenches, including all existing verification requirements, through the seamless integration of VCS and the Synopsys ZeBu Server emulation system. The tutorial will present the use models and basic tool options required to enable simulation acceleration within a regular VCS environment, the SystemVerilog constructs used, and the available debug and profiling capabilities. For different verification needs, we will analyze how the different constructs and use-models provide trade-offs between ease of use, simulation performance and hardware utilization.

Speakers:

Behzad Safari Astaraie, Synopsys

Thank you to our Sponsor

Tutorial 3.4: Using Models to Shift-Left Verification and Enable Verification IP Re-use Throughout the Design Flow

Time: 17:00 – 18:00 | Stream 3

Organizers:

Baruch Mitsengendler, MathWorks

Using models to shift-left verification and enable Verification IP re-use throughout the design flow

The shrinking of the design cycle time and the need for zero bugs, is forcing the semiconductor industry to rethink its design flows. Particularly important are the abilities to catch bugs as early as they are introduced, to avoid long iteration cycles. Of similar importance is the Reuse of design models and verification IPs throughout the different steps of the development flow.

In this presentation we will show how MATLAB and Simulink are used by many leading semiconductor companies to quickly model their systems and IPs and to start verification at behavioral model level by defining test cases, linking them to requirements and measuring coverage to assess completeness.

After that, we will present how system models and verification IPs can be reused within EDA tools like logic simulators as well as SPICE simulators. We will explore several options, like the generation of UVM test benches, the generation of SystemVerilog behavioral models as well as the co-simulation with SPICE and logic simulators.

This approach allows engineers to find bugs earlier in their development. It also enables efficient reuse, tool interoperability, and quick iterations between design steps, significantly reducing the overall development time.

Who should attend?

Systems Engineers and Verification Engineers (both Digital and Mixed-Signal).

Speakers:

Baruch Mitsengendler, MathWorks

Cristian Macario, MathWorks

Thank you to our Sponsor

Tutorial 4.4 Analysis and Verification of Safety Critical E/E Systems and Circuits

Time: 17:00 – 18:00 | Stream 4

Organizer:

Alessandra Nardi - Cadence Design Systems

E/E systems and circuits deployed in safety critical application introduce additional metrics that quantify the likelihood of failure and the ability of the device under consideration to detect (and potentially correct) faulty behaviors. These metrics needs to be calculated and verified by Functional Safety (FS) analysis and verification techniques. In addition to specific analysis and verification challenges, the process development lifecycle for safety-critical applications is also rigorous in terms of traceability requirements throughout the distributed supply chain.

The tutorial covers an introduction to FS analysis and lifecycle development and evolves into an introduction of FS verification with a focus on fault injection and its associated challenges and potential solutions.

Speakers:

John Hayden, Analog Devices

Jason Campbell, NVIDIA

18:00 – 18:30

Closure Day 1 & Outlook Day

Technical Program: Wednesday, October 28
Time Zone is CET

9:00 – 9:15
Opening & Welcome

9:00 – 18:30
Virtual Experience Rooms & Virtual Exhibitors

9:15 – 10:15
Keynote: Challenges of a sustainable innovative automotive computing architecture

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Speaker: Dr. Matthias Traub

Head of Architecture & Technologies Car Software Organization
Volkswagen Group

Abstract: The beginning of the digital age into the 21st century, enabled by the invention of the microprocessor, enables us today to have more and more everyday tasks and responsibilities taken over by various software and systems. The technology is developing exponentially so that the underlying (computing) systems have to meet ever more complex and greater demands. Innovative and sustainable products are based on a framework that can grow and adapt to constantly changing requirements. The separation of software from hardware is an essential part of innovative and sustainable software-driven products. With a view to the automotive industry, questions arise about the design of an innovative electric/electronic architecture and the associated challenges of driving a software-centered approach with a simultaneously layered architecture, in order to be able to map any desired (driving) function quickly and efficiently in the future.

Biography: Dr. Matthias Traub, since December 2019, Head of Architecture & Technologies Car Software Organization @Volkswagen Group

Professional career

2017 – 2019 Head of E/E-Architecture, Security, Connectivity and
Computing Platforms BMW AG

2012 – 2017 Chief architect and head of e/e architecture platform
BMW AG

2010 – 2012 Architect for electric/electronic (powertrain and
chassis) BMW AG

2007 – 2010 Engineer for gateway ECU Daimler AG
Education/ Academic studies

2007 – 2010 Ph.D. Thesis "Network Architectures In-Vehicles"
Daimler AG /KIT

2001 – 2007 Studies of "Electrical and Systems Engineering" KIT

10:15 – 10:30
Virtual Coffee Break
Meet us in the Virtual Experience Rooms

Stream 1
10:30 – 12:00

10:30 – 11:00
P1.1 Does it pay off to add portable stimulus layer on top of UVM IP block test bench?
Xia Wu, Jacob Sander Andersen - Syosil Aps
Ole Kristoffersen - Ericsson

11:00 – 11:30
P1.2 Make your Testbenches Run Like Clockwork!
Markus Brosch, Salman Tanvir, Martin Ruhwandl - Infineon Technologies AG

11:30 – 12:00
P1.3 A Comprehensive Verification Platform for RISC-V based Processors
Emre Karabulut, Berk Kisinbay, Abdullah Yildiz, Rifat Demircioglu - Yonga Technology Microelectronics R&D

Stream 2
10:30 – 12:00

10:30 - 11:00
P2.1 A Methodology to Verify Functionality, Security, and Trust for RISC-V Cores
Nicolae Tusinschi, Wei Wei Chen - OneSpin Solutions

11:00 - 11:30
P2.2 Build Reliable and Efficient Reset Networks with a Comprehensive Reset Domain Crossing Verification Solution
Wanggen Shi - Big Fish Semiconductor Ltd
Yuxin You, Kurt Takara - Mentor, A Siemens Business

11:30 - 12:00
P2.3 Model-based Automation of Verification Development for automotive SOCs
Aljoscha Kirchner, Jan-Hendrik Oetjens - Robert Bosch GmbH
Oliver Bringmann - Eberhard Karls Universität Tübingen

Stream 3
10:30 – 12:00

10:30 - 11:00
P3.1 Boosting Mixed-signal Design Productivity with FPGA-based Methods Throughout the Chip Design Process
Gabriel Rutsch, Simone Fontanesi, Steven Tan Hee Yeng, Andrea Possemato, Gaetano Formato, Wolfgang Ecker - Infineon Technologies AG
Steven Herbst, Mark Horowitz - Stanford University

11:00 - 11:30
P3.2 SOBEL FILTER: Software Implementation to RTL using High Level Synthesis
Bhavna Aggarwal, Umesh Sisodia, Snigdha Tyagi - CircuitSutra Technologies Pvt. Ltd

11:30 - 12:00
P3.3 Single Source System to Register-Transfer Level Design Methodology Using High-Level Synthesis
Petri Solanti - Mentor, A Siemens Business
Thomas Arndt - COSEDA Technologies GmbH

Stream 4
10:30 – 12:00

10:30 – 11:00
P4.1 Enhancing Quality and Coverage of CDC Closure in Intel's SoC Design
Rohit Sinha - Intel

11:00 – 11:30
P4.2 Static Analysis of SystemC/SystemC-AMS System and Architectural Level Models
Karsten Einwich, Thilo Voertler - COSEDA Technologies GmbH

11:30 – 12:00
P4.3 Bit density-based pre-characterization of RAM cells for area critical SOC design
Dilip Ajay- QT Technologies Ireland

12:00 – 13:00
Virtual Lunch Break
Meet us in the Virtual Experience Rooms

12:00 – 13:00
Qualcomm Webinar
Paul Kelleher, Qualcomm Ireland Intro
Keith O'Donoghue, Analog Mixed-Signal IP
Sumit Jha, AMS Design Verification
Manu Prakash, Digital Design Verification
Andriy Temko, DV Acceleration Using ML

13:00 – 14:00
Poster Session
Virtual Experience Poster Rooms
Each poster will be located in a themed room.

P5.1 An Automated Pre-silicon IP Trustworthiness Assessment for Hardware Assurance
IP Security Room

Sergio Marchese, John Hallman, Sven Beyer, David Landoll - OneSpin Solutions
Garrett Chan, Salam Zantout, Vikram Rao - The Aerospace Corporation

P5.2 Deploying HLS in a DO-254/ED-80 Workflow
Functional Safety Room

Jacob Wiltgen, Byron Brinson, David Aerne - Mentor, A Siemens Business
Tammy Reeve, - Patmos Engineering Services & Airworthiness Certification Services

P5.3 Experience of using Formal Verification for a Complex Memory Subsystem Design
IP-XACT Room

Sujeet Kumar, Vandana Goel, Hrushikesh Vaidya, Ronak Sarikhada - Intel

P5.4 Analog Modelling to Suit Emulation for Hardware-Software Co-Verification
AMS Room

Saranya Das - Analog Devices Inc

P5.5 A step towards Zero Silicon Bugs using Assertion based Assumption Validation
SystemVerilog Room

Rohit Sinha, Christie Babu - Intel

P5.6 IP-Coding Style Variants in a Multi-layer Generator Framework
System C Room

Zhao Han, Keerthikumara Devarajegowda, Andreas Neumeier, Wolfgang Ecker - Infineon Technologies AG

P5.7 Probing UPF Dynamic Objects: Methodologies to Build Your Custom Low-Power Verification Platform
SystemVerilog Room

Progyna Khondkar - Mentor, A Siemens Business

P5.8 Automatic Diagram Creation for Design and Testbenches
UVM Room

Paul O'Keeffe, Jamie Beattie, Gian Lorenzo - CreVinn Teoranta

P5.9 Formal Verification Experiences: Silicon Bug Hunt with "Deep Sea Fishing"
Functional Safety Room

Ping Yeung, Mark Handover, Abdel Ayari - Mentor, A Siemens Business

P5.10 Achieving Faster Reset Verification Closure with Intelligent Reset Domain Crossings Detection
UVM Room

Milan Kaur Anand, Sulabh Kumar Khare - Mentor, A Siemens Business

P5.11 Verification of a Multi-languages Components - A Case Study: Specman E Environment with SystemVerilog UVM UVC
Portable Stimulus Room

Eran Lahav - Veriest Solutions

14:00 – 15:00
Panel: Verification Challenges of an Exascale Supercomputer

Moderator:
Jean-Marie Brunet - Mentor, A Siemens Business

Panelists:
Christian Beckmann - ASIC Verification Manager, Global Big Data and Security Division, Atos

Mark Glasser - Member of the Technical Staff, Cerebras

Gajinder Panesar - Fellow, Mentor, A Siemens Business

Nasr Ullah - Senior Director of SiFive Performance Architecture for RISC-V Technology and Applications (SPARTA), SiFive

Ying-Chih Yang - CTO SiPearl

Roger Espasa - CEO SemiDynamics

Europe and the European Processor Initiative (EPI) consortium are taking a huge leap forward with the goal to design a low-power, high-performance exascale supercomputer. Many notable European companies are committed to a revolutionary new microprocessor architecture and roadmap for a well-implemented design.

The stakes are high. A secure and reliable microprocessor to support high-performance computing will need to meet the demands of a range of emerging complex applications. Those include artificial intelligence, connected mobility, storage, research, health, weather forecasting, energy, defense, chemicals, engineering, cybersecurity and smart cities as a start.

Achieving success will not be possible without robust verification. A new exascale supercomputer design creates far-reaching implications and potential consequences for today's design verification flow that could require reimagining and overhauling each product segment. It may mean reeducation of verification engineers as well.

Chip design and verification experts from Europe and the U.S. will join moderator Jean-Marie Brunet from Mentor, a Siemens Business, for a discussion about the verification requirements of a new type of exascale supercomputer. At the end of the panel, they will attempt to define a specialized new verification flow to support the initiative.

15:00 – 15:30
Virtual Coffee Break
Meet us in the Virtual Experience Rooms

Stream 1
15:30 – 17:00

15:30 – 16:00
P1.4 Mutable Verification environments through Visitor and Dynamic Register map Configuration
Matteo Barbati, Alberto Allara - STMicroelectronics

16:00 – 16:30
P1.5 Facilitating Transactions in VHDL and SystemVerilog
Rich Edelman, Mentor, A Siemens Business

16:30 – 17:00
P1.6 Lean Verification Techniques: Executable SystemVerilog UVM Defect Table For Simulations
Kamel Belhous, Paul Ulrich - Teradyne, Inc
Steve Burchfiel, Kevin Schott - CorrectDesigns

Stream 2
15:30 – 17:00

15:30 – 16:00
P2.4 Discovering Deadlocks in a Memory Controller IP
Jef Verdonck, Emrah Armagan, Khaled Nsaibia, Slava Bulach - u-blox AG
Pranay Gupta, Anshul Jain, Chirag Agarwal, Roger Sabbagh - Oski Technology, Inc

16:00 – 16:30
P2.5 How To Verify Encoder And Decoder Designs Using Formal Verification
Jin Hou - Mentor, A Siemens Business

16:30 – 17:00
P2.6 Using Formal to Prevent Deadlocks
Abdelouahab Ayari, Mark Eslinger, Joe Hupcey - Mentor, A Siemens Business

Stream 3
15:30 – 17:00

15:30 – 16:00
P3.4 Mixed Electronic System Level Power/Performance Estimation using SystemC/TLM2.0 Modeling and PwClkARCH library
Antonio Genov, Loic Leconte - NXP Semiconductors
François Verdier - University of Cote d'Azur, CNRS, LEAT

16:00 – 16:30
P3.5 Timing-Aware high level power estimation of industrial interconnect module
Amal Ben Ameur, François Verdier - University of Cote d'Azur, CNRS, LEAT
Antonio Genov, Loic Leconte - NXP Semiconductors

16:30 – 17:00
P3.6 Clock Controller Unit Design Metrics: Area, Power, Software flexibility and Congestion Impacts at System Level
Michele Chilla, Leonardo Gobbi – Qualcomm Ireland

Stream 4
15:30 – 17:00

15:30 – 16:00
P4.4 Temporal assertions in SystemC
Mikhail Moiseev, Leonid Azarenkov, Ilya Klotchkov - Intel Corporation

16:00 – 16:30
P4.5 Accelerating and Improving FPGA Design Reviews Using Analysis Tools
Anna Tseng, Kurt Takara, Abdelouahab Ayari - Mentor, A Siemens Business

16:30 – 17:00
P4.6 Accelerating Automotive Ethernet validation by leveraging Synopsys Virtualizer with TraceCompass
Ashish Gandhi, Praveen Kumar Kondugari, Sam Tennent - Synopsys

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17:00 – 18:00
Keynote: The Future of Compute: Verification in the era of Heterogeneous Design

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Speaker: Dr. Mike Mayberry

Chief Technology officer at Intel Corporation

The digital transformation continues to gain momentum and is changing the shape of business, industry and consumers around the world. This transformation is characterized by continued strong demand for compute at all points in the network – at the core, the edge, and at the endpoints. Data continues to grow at an exponential rate and not only drives the compute requirements, but also requires efficient solutions for movement and storage of data that is critical for overall performance. From device to cloud, new applications and use cases are continuously emerging. In addition to continued dimensional, materials and device scaling, Moore's Law will evolve to meet the challenges and complexity of heterogeneous 3D integration, and novel architecture integration schemes that will continue to grow. This transformation demands that we adapt our design thinking and move from monolithic self-contained systems to a data/information approach where the system solutions encompasses all the elements needed to convert data to information. These integrated but heterogeneous application-specific design solutions will require different verification and testing approaches to be successful.

Biography: Dr. Michael (Mike) C. Mayberry is the chief technology officer at Intel Corporation. He is a senior vice president and general manager of Technology Development, where he is responsible for the research, development and deployment of next-generation silicon logic, packaging and test technologies that will produce future Intel products.

Since joining Intel in 1984 as a process integration engineer, Mayberry has held a variety of positions. As part of the California Technology Development team, he developed EPROM, flash and logic wafer fabrication processes. In 1994, he moved to Sort Test Technology Development, responsible for roadmaps and development of test processes for Intel microprocessors. In 2005, he moved to Components Research and was responsible for research to enable future process options for Intel's technology development organizations. In 2015, he moved to Intel Labs and became responsible for Intel's product-driven research. In 2018, he moved to the Technology Development group at Intel.

Mayberry received his bachelor's degree in chemistry and mathematics from Midland College and his Ph.D. in physical chemistry from the University of California, Berkeley.

18:00 – 18:30
Closing Session & Best Paper Awards
Thank you to our sponsor

System C Evolution Day

The fifth SystemC Evolution Day is a full-day, technical workshop on the evolution of SystemC standards to advance the SystemC ecosystem. In several in-depth sessions, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for inclusion in Accellera/IEEE standards.

SystemC Evolution Day is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance SystemC standards.

Date / Time: October 29, 2020 (day after DVCon Europe 2020) | 08:30 - 19:30

Location: Virtual Workshop

Submissions / Questions: Email systemc-evolution-day@lists.accellera.org

Organization Team:

- » Ola Dahl, Ericsson (Chair)
- » Martin Barnasconi, NXP
- » Jerome Cornet, STMicroelectronics
- » Christian Sauer, Cadence
- » Mark Burton, GreenSocs
- » Daniele Ludovici, Intel

Schedule:

8:30-9:00	Welcome and Introduction
9:00-10:00	A SystemC TLM 2.0 Extension for the Model Exchange of Off-Chip Communication Protocols
10:00-11:00	Multi-core Debugger Integration in OSCI SystemC
11:00-11:30	Update from Accellera Working Groups
11:30-12:00	Open Discussion
13:00-15:00	Virtual Networking
16:00-17:00	Towards a Standardized Multi Language Verification Framework - First Prototype and Demonstration
17:00-18:00	Temporal Assertions in SystemC
18:00-19:00	Matchlib: A New Open-source Library to Enable Efficient Use of High Level Synthesis
19:00-19:30	Summary and Concluding Discussion

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