2018
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
EUROPE

Sponsored by:
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SYSTEMS INITIATIVE™

HOLIDAY INN MUNICH CITY CENTRE
OCTOBER 24 – 25, 2018
DVCON-EUROPE.ORG

Conference Program

WELCOME TO DVCON EUROPE 2018

DVCon Europe 2018

Welcome Message from DVCon Europe General Chair, Martin Barnasconi

General Chair - *NXP Semiconductors*

Welcome to DVCon Europe 2018, the Design and Verification Conference and Exhibition in Europe!

Technical experts from around the world will come together to share the latest developments and experiences in the application of EDA languages, methodologies, and tools for the design and verification of electronic systems and integrated circuits. I am proud to see that DVCon Europe has become a well-established technical conference which is recognized and embraced by the design and verification community in Europe and beyond.

This fifth edition of DVCon Europe again offers a fully packed 2-day technical program including tutorials, panels, keynotes, presentations, and an exciting exhibition. Both days start with an inspiring keynote. On Wednesday, Dr. Stefan Jockusch from Siemens PLM Software Inc. will present "Driving Digitization with a Boundary Free Innovation Platform."

The first day of DVCon Europe traditionally covers 16 tutorials. The tutorial program offers a unique opportunity to enrich your skills or broaden your scope on a variety of topics, ranging from portable stimulus, virtual prototyping, functional safety, mixed-signal, requirements-driven verification, machine learning, and much more. The rich program contains both methodology and standardization-oriented tutorials as well as practical hands-on tutorials where users share practical experiences.

The DVCon Europe Reception takes place on the Wednesday afternoon. It is a unique networking event to interact with your colleagues, peers, partners, suppliers, or customers in the design and verification community. And perhaps you will make new friends at DVCon Europe!

On Thursday, Mr. Philippe Magarshack from ST Microelectronics will start the second day of the conference with the keynote "Simultaneous disruptions in IoT drive the perfect storm: Connectivity, Artificial Intelligence, Security, Sensor Fusion and more." It is followed by an industry panel entitled "Using Next Generation Methods of Systems Modeling and Virtual Prototyping to Revolutionise the Design, Verification and Manufacture of High Value, Complex Electromechanical Products across the Automotive Supply Chain". Jim Hogan will moderate this panel with experts from Bosch, Intel, Audi, Infineon and Siemens, to discuss and debate how the Automotive industry could strengthen its collaboration to enhance design and verification methodologies.

With the growing number of paper submissions this year, the technical program on the second day has been expanded. In four parallel tracks, 12 sessions are hosted covering topics such as UVM, virtual prototyping, functional safety, SystemC, TLM, Low power, AMS verification, advanced verification, stimulus generation, virtual platforms and visualization and more. You are invited to vote on the best paper, which will be announced at the close of the conference.

On both days, DVCon Europe hosts an exciting exhibition with more than 20 exhibitors. Feel free to interact with the EDA companies, training institutes and service providers the whole day. And most likely you will find new technologies and tooling that you use in your daily work.

Finally, a special and well deserved thank you to the DVCon Europe steering and technical program committee members, reviewers, sponsors, exhibitors, panelists, authors, presenters, attendees and other volunteers to make DVCon Europe a great event!

The DVCon Europe steering committee and Accellera wish you a warm welcome and enjoyable DVCon Europe 2018!

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accellera SYSTEMS INITIATIVE™

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

Membership

Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at www.accellera.org.

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CONFERENCE DETAILS

REGISTRATION HOURS

Location: Großer Saal Foyer

Wednesday, October 24 ------ 07:30 - 19:30
Thursday, October 25 --------- 07:30 - 18:00

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DVCON EUROPE 2018 EXPO

Location: Großer Saal

Wednesday, October 24 ------ 10:00 - 19:00
Thursday, October 25 --------- 10:00 - 18:30

TUTORIALS & PROCEEDINGS DISTRIBUTION

DVCon Conference Papers and Tutorial presenter slides will be delivered electronically online via a username and password.

To access: http://proceedings.dvcon-europe.org
Username and password will be provided to registered conference attendees

ATTENDEE BREAKS

Location: Großer Saal

Wednesday, October 24

08:00 - 08:30
09:30 - 10:00
11:30 – 11:45
15:45 - 16:00

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Thursday, October 25

07:30 - 08:00
10:30 - 10:45
14:45 - 15:15

NETWORKING RECEPTIONS

Location: Großer Saal

One of the main reasons you came to DVCon: NETWORKING! Introduce yourself and leave DVCon with a deeper professional network!

Wednesday, October 24 ------ 17:30

Thursday, October 25 --------- 17:30

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Don't miss DVCon on Facebook at https://www.facebook.com/DVCon-Europe-898352006944641/.

WIRELESS INFORMATION

Enjoy free Wi-Fi at DVCon Europe! Connect to the Conference Wi-Fi via:

SSID: DVCON18

PW: DVCON18

BEST PAPER VOTING

Vote for your favorite paper using this link:

https://dvcon-europe.org/vote

All votes need to be completed by 17:30 on Thursday, October 25, to be tallied. Award will be announced in the closing ceremony from 17:30 to 18:15 on Thursday, October 25, in Exhibit Hall.

AWARDS PRESENTATION

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Join us on **Thursday, October 25 at 17:30** in the Exhibit Hall for the Closing Ceremony and announcement of the Best Paper Awards.

CONFERENCE FLOORPLAN

WEDNESDAY'S AGENDA

2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

08:00 - 08:30	Welcome Coffee Service *Room: Großer Saal Foyer* *Thank You to Our Sponsor:* onespin			
08:30 - 08:45	Opening Session *Room: Ballsaal*			
08:45 - 09:30	Keynote: Driving Digitalization With A Boundary Free Innovation Platform *Room: Ballsaal* **Stefan Jockusch** *Siemens PLM Software Inc.*			
09:30 -10:00	Attendee Break *Room: Großer Saal Foyer* *Thank You to Our Sponsor:* onespin			
10:00 - 11:30	Tutorial 1 - Case Study of Verification Planning to Coverage Closure @ Block, Subsystem and System-on-Chip Level *Room: Forum 4*	Tutorial 2 - UVM Audit: Assessing UVM Testbenches to Expose Coding Errors and Improve Quality *Room: Forum 5*	Tutorial 3 - Efficient use of Virtual Prototypes in Hardware/Software Development and Verification *Room: Forum 6*	Tutorial 4 - Machine Learning Introduction and Exemplary Application in Embedded Wireless Platforms *Room: Forum 7*
10:00 - 19:00	DVCon Europe Expo *Room: Großer Saal*			
11:30 - 11:45	Attendee Break *Room: Großer Saal* *Thank You to Our Sponsor:* onespin			
11:45 - 13:15	Tutorial 5 - Accellera Portable Test and Stimulus: The Next Level of Verification Productivity is Here *Room: Forum 4*	Tutorial 6 - UVM Mixed Signal Extensions – Sharing Best Practice and Standardization Ideas *Room: Forum 5*	Tutorial 7 - Tutorial on RISC-V Design and Verification *Room: Forum 6*	Tutorial 8 -Firmware Firmly under Control: New Optimization and Verification Techniques for Application Specific Electronic Systems *Room: Forum 7*
13:15 - 14:15	Luncheon *Room: Großer Saal*			
14:15 - 15:45	Tutorial 9 - Developing and Testing Automotive Software on Multi-SoC ECU Architectures using Virtual Prototyping *Room: Forum 4* *Thank You to Our Sponsor:* SYNOPSYS	Tutorial 10 - Accelerating the Path from Idea to Silicon for Computer Vision and Deep Learning in Automotive ICs *Room: Forum 5* *Thank You to Our Sponsor:* Mentor A Siemens Business	Tutorial 11 - Making ISO26262 Functional Safety Verification a Natural Extension of Functional Verification *Room: Forum 6* *Thank You to Our Sponsor:* cadence	Tutorial 12 - Requirements Driven Design Verification Flow *Room: Forum 7* *Thank You to Our Sponsor:* ELECTRA IC Design & Verification
15:45 - 16:00	Attendee Break *Room: Großer Saal* *Thank You to Our Sponsor:* onespin			
16:00 - 17:30	Tutorial 13 - Functional Safety Verification for ISO 26262-Compliant Automotive Designs - What's New and What's Needed *Room: Forum 4* *Thank You to Our Sponsor:* SYNOPSYS	Tutorial 14 - Hardware and Software Co-verification in Hybrid HDL Simulation and Emulation Environment with QEMU *Room: Forum 5* *Thank You to Our Sponsor:* ALDEC THE DESIGN VERIFICATION COMPANY	Tutorial 15 - Unifying Mixed-Signal and Low-Power Verification *Room: Forum 6* *Thank You to Our Sponsor:* cadence	Tutorial 16 - Using Mutation Coverage for Advanced Bug Hunting and Verification Signoff *Room: Forum 7* *Thank You to Our Sponsor:* onespin
17:30	DVCon Reception & Expo *Room: Großer Saal* *Thank You to Our Sponsor:* intel			

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Welcome Coffee Service

Time: 08:00 - 08:30 | Room: Großer Saal Foyer

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Opening Session

Time: 08:30 - 08:45 | Room: Großer Saal Foyer

Keynote: Driving Digitalization With A Boundary Free Innovation Platform

Time: 08:45 - 09:30 | Room: Ballsaal

Speaker:
Stefan Jockusch - *Siemens PLM Software Inc.*

We are witnessing a radical change of the way products are created, produced, and utilized. As a consequence of continuing digitalization, leading technology companies are pursuing the idea of a complete, high fidelity "digital twin" that makes the boundaries between the design process of mechanical parts, electronics, embedded software, sensors and specialized IC and sensor technology are disappearing.

This digital twin is becoming a necessity. Autonomous driving, as an example, puts an end to the feasibility of verifying the functionality of today's and tomorrow's vehicles through road testing. A complete virtualization of mechanical properties, physics, electronics, real-time software, down to the sensor data processing at the IC level is the only avenue to verify the safety and functionality of advanced driver assistance systems and autonomous functions. In the same way, technologies like additive manufacturing, advanced materials and exploding variation require an extensive virtualization of the production process to accelerate verification.

IoT technology provides an unprecedented amount of information and feedback for systems in operation. It is already giving a competitive advantage to manufacturers who are going beyond "analytics" and tap into the models created during development and production to utilize the vast amounts of available data in the optimization of the system.

Biography: Dr. Stefan Jockusch is vice president of Strategy for Siemens PLM Software, a business unit of the Siemens Digital Factory Division. Dr. Jockusch drives strategic business planning and market intelligence as well as coordinates business activities across all Siemens PM Software business segments and with Digital Factory Division leadership. Dr. Jockusch has served in a number of business leadership and R&D management roles, driving the development and market introduction of radically innovative mechatronic systems. Prior to his current assignment, Dr. Jockusch was vice president of Automotive Industry Strategy, leading the company's business development and portfolio planning efforts for the automotive industry. He began his career at Siemens as a management consultant with Siemens Corporate Technology. He later moved to Siemens AG as executive board assistant for the industry, transportation and technology sectors, where he led several strategic initiatives. A U.S. and German citizen with broad international experience, he relocated to the United States in 2001 and later decided to make the U.S. his family's permanent home. Stefan holds a PhD summa cum laude in natural sciences from University of Bielefeld and a master's degree in physics from the University of Göttingen.

Attendee Break

Time: 09:30 - 10:00 | Room: Großer Saal Foyer

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Tutorial 1 - Case Study of Verification Planning to Coverage Closure @Block, Subsystem and System-on-Chip Level

Time: 10:00 - 11:30 | Room: Forum 4

Organizer:

Paul Kaunds - *Sondrel Ltd*

Verification Planning and achieving coverage closure goals on time and under budget is one of the most challenging assignments in functional verification. Complicating this task is the increasing popularity of platform-based design, where IPs are extensively parameterized to enable end-user customization and differentiated derivatives.

Metrics is the key to success and we provide concrete examples that illustrate the value of Metrics at each stage.

Coverage metrics are critical to measuring and guiding design verification. As designs have grown, increasingly advanced verification technologies, methods and additional metrics have been designed to form a fuller coverage model.

In this tutorial, we will provide an in-depth analysis of various planning, implementation, debug and coverage closure challenges faced in functional verification at block level, subsystem and system-on-chip level. By taking relevant examples we will demonstrate how these issues can be either avoided or solved. We will also highlight some of the best practices for better robustness, predictability, configurability and reuse of UVM and C code.

Speakers:

Paul Kaunds - *Sondrel Ltd*
Revati Bothe - *Sondrel Ltd*
Jesvin Johnson - *Sondrel Ltd*

Tutorial 2 - UVM Audit: Assessing UVM Testbenches to Expose Coding Errors and Improve Quality

Time: 10:00 - 11:30 | Room: Forum 5

Organizers:

Jason Sprott - *Verilab Ltd.*
Mark Litterick - *Verilab Ltd.*
Jonathan Bromley - *Verilab Ltd.*

Does your UVM codebase contain hidden traps that may undermine current or future projects?

Working on client projects we have seen many verification environments that superficially claim to follow UVM best practice, but don't stand up to expert scrutiny – for example:

- inflexible components that don't provide appropriate hooks for future extension
- code that can't easily be reused in a different setting
- stimulus that fails to make good use of the power of UVM sequences
- weak coverage that gives false confidence in verification completeness
- existing (legacy) code that doesn't do all it claims to do
- poor architecture that will be difficult for reviewers or future maintainers to understand

In this tutorial we present a strategy and guidelines for auditing existing and new UVM code, giving you a technically robust approach to planning and review of your UVM project. Going far beyond trivial "tabs or spaces" coding checklists, UVM Audit addresses the truly important issues of reuse, flexibility and verification effectiveness. It identifies a range of frequently-encountered problems, and provides easily-understood guidance that you can apply to legacy, current, and future projects.

The audit approach we offer in this tutorial has field-proven value both for project managers and for the engineering team. Its benefits include:

- quality control and assessment of your code, especially important when the team has diverse levels of skill and experience
- evaluation of existing code that you plan to reuse, improving accuracy of effort estimation for the new project
- identifying areas for improvement for you and your team's skill-sets
- reasoned prioritization of areas of improvement based on severity of defects found

The tutorial content is of interest to verification management and leadership as well as the testbench implementation team. Attendees will take away a renewed awareness of their priorities for building high-quality environments, and practical ideas for reviewing existing and newly written code to ensure it is fit for purpose.

Speaker:

Mark Litterick - *Verilab Ltd.*

Tutorial 3 - Efficient use of Virtual Prototypes in Hardware/Software Development and Verification

Time: 10:00 - 11:30 | Room: Forum 6

Organizer:

Eyck Jentzsch - *MINRES® Technologies GmbH*

Software development for embedded systems is becoming an increasingly challenging task, which calls for advanced design methods and tools to overcome productivity pains. Software developers have to cope with continuously growing complexity, instruction execution on multiple cores, a large number of hardware interactions (i.e. sensors & actors) and limited visibility into the device. Virtual Prototypes (VPs) can help to solve many of these issues as they allow insight into software execution and its interaction with the hardware, as described in multiple publications and tutorials before. An additional valuable aspect of using VPs is the possibility to model whole systems.

In this context the term system refers to a system-on-chip (SoC) with software components running on a hardware platform, but also the surrounding environment, which interacts with the SoC through peripherals that connect to sensors and actors. Existing environment models can be reused by connecting them into a VP. VPs enable a convenient analysis of what-if scenarios, which are often much more difficult to conduct using the real hardware. Such models are more widely accessible and available compared to a complex prototype hardware setup e.g. in a lab. Adding analysis and debug APIs (Application Programmable Interfaces) is easily possible in a software model. Some of those topics will be shown and demonstrated during the tutorial.

But how does this impact the hardware development process?

Hardware designers still only rarely use VPs for RTL verification even though VPs come “naturally” with the implementation of many reference algorithms. Therefore, this tutorial also showcases the benefits of VPs for hardware designers. It will be demonstrated how the debug capabilities of VPs can be used to better analyze hardware issues and how simulations can be accelerated. Hardware developers incorporating VPs into their workflows become valuable contributors in agile teams, which, in turn, result in productivity and quality improvements of the development process. Hardware and software teams can work more closely together and develop shared sources e.g. hardware access functions for both hardware test cases and software driver purposes.

Sharing the same development environment helps hardware designers to better understand how a peripheral is being stressed by software. Hardware designers can easily get an understanding of real bus traffic and interrupt loads while trace files can be used to convert software traces into hardware stimuli and result-expectation. Stimulus from VP tests can be logged and played back in other test environments as augmentation of existing tests. Such tests can be especially useful when it comes to verifying the synchronization between different processing units through interrupts, mailboxes and shared memory. However, these tests can only be developed and employed when a prototype is available. In the context of hardware testing, this implies that realistic stimulus from the software side is often not available until very late in the development process. Here the VP approach is one of the very few means to generate some realistic input early on.

The example in the tutorial will demonstrate some of the aforementioned issues and approaches as well as many not mentioned here.

Speakers:

Rocco Jonack - *MINRES® Technologies GmbH*
Eyck Jentzsch - *MINRES® Technologies GmbH*

Tutorial 4 - Machine Learning Introduction and Exemplary Application in Embedded Wireless Platforms

Time: 10:00 - 11:30 | Room: Forum 7

Organizer:

Jonathan Ah Sue - *Intel Germany GmbH*

In the late 1960s, Samuel Arthur, research scientist at IBM, first employed the term machine learning to define the ability of computers to learn from data without having been explicitly programmed. Starting from this statement, we briefly introduce in this tutorial the historical background of machine learning (ML) and some significant milestones achieved until now. Then, we outline the current enabling factors of effective ML, i.e., data availability, computational power, and algorithmic improvements, while describing for each of these factors their key value with respect to machine learning. Based on Pedro Domingos statement ("The Master Algorithm"), we cluster current machine learning algorithm structures in 5 classes, describing their main theoretical concepts and achievements.

We then describe how these approaches can solve different types of tasks, i.e., supervised, unsupervised learning… Given the several types of algorithms and tasks, we propose a concrete and simple running example to illustrate the previous and following statements of the tutorial. The current major concerns of ML are outlined (bias/variance dilemma and overfitting, exploration/exploitation…) and serve as basis to introduce the different fields of study of ML, e.g., computational learning theory and statistical learning theory. Although a clear boundary cannot always be drawn between research fields, we attempt to give an overview of the ML landscape research and to describe their proposed solutions (training/testing split, regularization, PAC framework…) with respect to the main concerns mentioned above. Given the previous running example, we describe a common ML workflow and outline the main differences compared to standard engineering or scientific approaches (i.e. iterative work, formalizing the learning vs. the problem, data-driven approach…). We further give insights on deep learning, a popular machine learning approach that achieved significant results these last years. We propose a bottom-up description of the different abstraction levels of ML, i.e., neuron, layer and network architecture. Therefore, a deep description of the maximum likelihood interpretation of logistic regression is used as key component of the explanation, and an overview of optimization methods is given.

As final section of the tutorial, we present an advanced application of ML to reduce power consumption of LTE-Advanced modems in mobile devices (LTE is the Long Term Evolution Advanced cellular radio standard by 3GPP standardization body). After describing the task we want to fulfill using ML and introducing the generic terms of LTE wireless communications from the mobile device perspective, we concretely describe a proposed methodology to evaluate ML performance on the modem at design time (power trajectories). Point by point, we outline our approach to consider the constraints of state of the art embedded system implementations for mobile devices as well as the constraints of cellular radio systems in general during the evaluation of ML algorithms. Finally, as an illustration of the ML workflow depicted in the previous section, we describe the simulation environment we used and highlight specific framework features that enable efficient analysis and scientific workflow (big data, caching, hashing, transactional data synchronization, model selection…).

This Tutorial is appropriate for engineers who want to gain insights into the fundamentals of machine learning and system level performance analysis methodologies for ML algorithms in embedded wireless systems like LTE-Advanced modems for mobile devices.

Speaker:

Jonathan Ah Sue - *Intel Germany GmbH*

Exhibit Floor Open

Time: 10:00 - 19:00 | Room: Großer Saal

Attendee Break

Time: 11:30 - 11:45 | Room: Großer Saal

Located in the Exhibit Hall.

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Tutorial 5 - Accellera Portable Test and Stimulus: The Next Level of Verification Productivity is Here

Time: 11:45 - 13:15 | Room: Forum 4

Organizer:

Tom Fitzpatrick - *Mentor, A Siemens Business*

Up until now verification teams had been unable to reuse tests as their efforts progressed from virtual platforms to RTL, block-level to system-level or from simulation to emulation, prototyping or silicon. The advent of UVM, constrained-random verification and functional coverage improved the reusability of portions of the verification environment, but these advances have not been able to enable reuse of verification intent throughout the product development process. Accellera's Portable Stimulus Working Group has created the new Portable Test and Stimulus Standard that would allow just this sort of verification intent reuse. This in-depth technical tutorial will focus on a set of typical design use-cases from a variety of applications and show how to use the Portable Test and Stimulus Standard to create an abstract model of your verification intent.

The tutorial will then demonstrate how these models can be used to generate scenarios to be executed on the different platforms and environments used in your development process, and how the models can be reused and leveraged from project to project.

For each application, we will show:

- How to model the critical verification intent,
- How that model may be used to generate multiple compatible coverage-centered scenarios,
- How to map that intent into multiple target-specific implementations,
- How the declarative semantics of the model drive the generation of executable tests on different platforms to implement the desired scenarios.

Speakers:

Tom Fitzpatrick - *Mentor, A Siemens Business*
Sharon Rosenberg - *Cadence Design Systems, Inc.*

Tutorial 6 - UVM Mixed Signal Extensions - Sharing Best Practice and Standardization Ideas

Time: 11:45 - 13:15 | Room: Forum 5

Organizer:

Joachim Geishauser - *NXP Semiconductors*

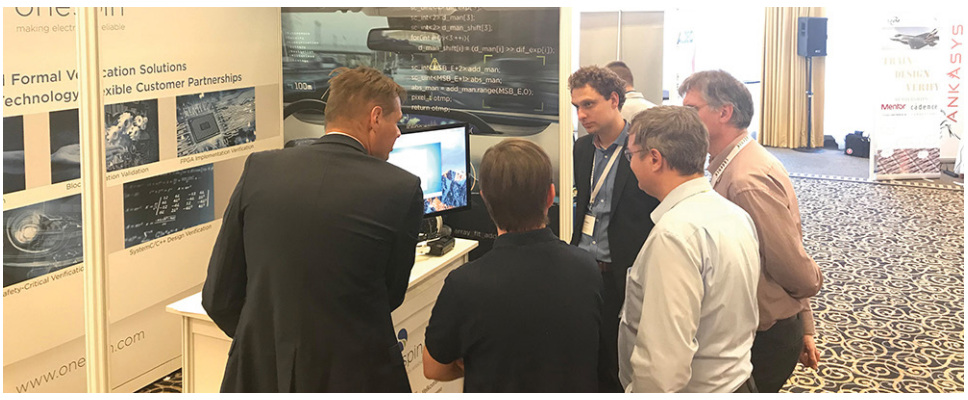
During the last couple of years, various proposals have been presented at DVCon events showing AMS extensions for UVM as attempt to enrich and improve the verification of mixed-signal products and applications. Although all proposal have a similar goal, to make UVM more mixed-signal aware, they all differ in the concept definition and implementation choices made.

This tutorial brings all contributors of these UVM mixed-signal proposals together, to share their best practices and discuss if a path to standardization is feasible.

Tutorial attendees will gain technical insight in existing UVM mixed-signal extensions, and they are invited to join the discussion on the need for further standardization in this domain. One possibility is to propose the establishment of a "Proposed Working Group" in Accellera with the objective to standardize the UVM mixed-signal extensions.

Speakers:

Sebastian Simon - *Infineon Technologies*
Patrick Lynch - *Xilinx Inc.*
Joen Westendorp - *NXP Semiconductors*



Tutorial 7 - Tutorial on RISC-V Design and Verification

Time: 11:45 - 13:15 | Room: Forum 6

Organizer:

Kevin McDermott - *Imperas Software Ltd.*

RISC-V (pronounced "risk-five") is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Founded in 2015, the RISC-V Foundation comprises more than 100 members building the first open, collaborative community of software and hardware innovators powering innovation at the edge forward. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

Verification requirements not only need to cover the wide range of features and extensions available within the RISC-V standard architecture but also allow for designs with custom instructions. The tutorial will explore the issues and challenges of SoC designers adopting RISC-V from the perspectives of IP Cores, software tools, virtual platforms and on-chip debug analytics for complex multi-core and heterogeneous many-core designs.

Speakers:

Peter Shields - *UltraSoC Technologies Ltd.*
Zdenek Prikryl - *Codasip Ltd.*
Kevin McDermott - *Imperas Software Ltd.*

Tutorial 8 - Firmware Firmly under Control: New Optimization and Verification Techniques for Application Specific Electronic Systems

Time: 11:45 - 13:15 | Room: Forum 7

Organizer:

Daniel Große - *Univ. of Bremen*

Application-specific adaptability of electronic systems demand for new design solutions. On the rise are automated firmware-based methodologies. From the application perspective this allows for flexible adaption to meet today's multiple conflicting requirements, such as performance and power. This tutorial discusses techniques targeting the optimization of memory subsystems as well as the HW/SW interface under timing and power budgets. Then, it focuses on efficient VP-based simulation techniques complemented by formal verification approaches taking the firmware into account.

T.1 Overview and Challenges for Firmware Design under Timing and Power Budgets

Daniel Große (University of Bremen)

T.2 Design-Time Optimization Techniques for Low-Power Embedded Memory Subsystems

Manuel Strobel (University of Stuttgart)

T.3 Automatic HW-SW-Interface Generation and Optimization

Martin Dittrich (TU Munich)

T.4 RISC-V based Virtual Prototype for Efficient Simulation of Firmware-based Designs

Vladimir Herdt (University of Bremen)

T.5 Properties-First Design: A New Design Methodology for SoC Hardware and Low-Level Software

Tobias Ludwig (TU Kaiserslautern)

Speakers:

Daniel Große - *Univ. of Bremen*
Manuel Strobel - *Univ. of Stuttgart*
Martin Dittrich - *Technische Univ. München*
Vladimir Herdt - *Univ. of Bremen*
Tobias Ludwig - *Univ. of Kaiserslautern*

Lunch

Time: 13:15 - 14:15 | Room: Großer Saal

Tutorial 9 - Developing and Testing Automotive Software on Multi-SoC ECU Architectures using Virtual Prototyping

Time: 14:15 - 15:45 | Room: Forum 4

Organizer:

Sam Tennent - *Synopsys, Inc.*

New demanding applications like ADAS, infotainment, and sensor fusion are driving growth in automotive semiconductors. These innovative features require both high compute power as well as predictability, which can only be delivered by heterogeneous architectures. We observe a trend towards multi-SoC Electronic Control Units (ECUs), where a high performance compute cluster, often running multiple embedded OSes, is integrated along with a traditional MCU cluster, running a real-time OS to deliver on predictability and timing constraints. In addition, the demand for complex, high bandwidth, and predictable I/O drives the need to include a "gateway" SoC, forming the communications hub with the rest of the system. For this kind of heterogeneous multi-SoC ECUs, the partitioning of software and the system integration of these components is essential to deliver on the system feature requirements.

Developing and testing software with high performance, safety, and reliability requirements of a "System-ECU" platform poses an enormous challenge. In this 90-minute tutorial, it will be shown how Virtual Prototyping enables critical use cases in today's demanding automotive software development landscape. We will discuss specific software development needs including predictable multi-SoC debugging, coverage driven fault injection, continuous integration, and "in-the-loop" testing with the environment.

The first half of this tutorial focuses on how a virtual prototype can enable a familiar and highly visible software development environment early in the lifecycle. The virtual prototype can also be used as an integral part of a software development flow later in the design cycle to enable use cases such as coverage based fault injection, where "difficult" or "impossible on hardware" scenarios can be discovered and tested in a systematic way. Focusing on integration aspects such as communications channels, I/O management and OS co-existence it will be shown how a Virtual Prototype can act as a centralized debug and test hub with an integrated view of the entire System-ECU.

The second half of this tutorial will focus on demonstrating a virtual prototype that represents a typical System-ECU. The demonstrated platform contains multiple SoC models (each themselves with multiple cores), comprising a compute-cluster SoC, a gateway, and an MCU, running multiple embedded Linux and a real-time OS accordingly. Connectivity between the SoC models is fully realized in order to facilitate end to end testing and verification of the system features. It will be shown that high visibility of the critical aspects of the system behavior can be achieved and verification and development can be realized.

Speaker:

Sam Tennent - *Synopsys, Inc.*

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Tutorial 10 - Accelerating the Path from Idea to Silicon for Computer Vision and Deep Learning in Automotive ICs

Time: 14:15 - 15:45 | Room: Forum 5

Organizer:

Carole Dunn - *Mentor, A Siemens Business*

The algorithms needed to teach a computer to "see, understand and make decisions" for ADAS and Autonomous Drive systems require a significant amount of parallel compute performance executing at the lowest possible power. Often the technology used to implement these functions employs Deep Neural Networks that demand even more high-performance parallel compute resources and inference solutions that are also low power. FPGAs and ASICs can meet these requirements for acceleration and power, but RTL development takes too long and does not adapt to rapid algorithm and late specification changes that frequently occur. To fully test these algorithms and systems thousands of driving scenarios and design parameters are required to simulate both the hardware and software to ensure safety.

This tutorial presents how High-Level Synthesis (HLS) helps designers take their algorithms and/or trained neural networks and rapidly generate low-power, high performance custom hardware accelerators. Using hardware emulation in the loop, the hardware accelerators can be verified for functional correctness, performance and power, and plugged into a larger heterogeneous system of hardware and software running on multiple ECUs. This enables the co-development of AUTOSAR software, ECU hardware and high-performance vision/networking accelerators together with mechanical system actuators, sensors and traffic scenarios.

Speakers:

John Stickley - *Mentor, A Siemens Business*
Petri Solanti - *Mentor, A Siemens Business*

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Tutorial 11 - Making ISO26262 Functional Safety Verification a Natural Extension of Functional Verification

Time: 14:15 - 15:45 | Room: Forum 6

Organizer:

Ann Keffer - *Cadence Design Systems, Inc.*

With intelligence being added to vehicles at an unprecedented rate, the opportunities for automotive silicon have never been greater. These autonomous systems require both functional verification and functional safety verification. While many semiconductor teams have established methodologies for functional verification, functional safety verification methodology is new or in development. As such, these teams need to learn about the importance of fault injection for semiconductors based on the ISO 26262 functional safety standard for road vehicles. But this knowledge is more than just a brute-force approach to measuring fault propagation. The teams need to understand when fault injection and expert judgement are important and how fault injection is significant for achieving the targeted Automotive Safety Integrity Level (ASIL) for SoCs.

This tutorial is targeted to verification methodology experts, safety experts, verification engineers, and project leads that need to implement functional safety verification or make their existing process more efficient. During the tutorial we will examine the requirements identified in the standard, the connection of those requirements to the functional verification flow for a unified methodology, and the implementation of those requirements in tools including fault simulation, automated fault characterization, safety verification campaign management, formal analysis of fault lists and results, plus more. Attendees will leave with new knowledge they can apply to fault optimization, fault analysis, traceability and congruence with the functional verification flow to provide efficiency for functional safety verification.

Speakers:

Andrew Betts - *Arm, Ltd.*
Ann Keffer - *Cadence Design Systems, Inc.*

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Tutorial 12 - Requirements Driven Design Verification Flow

Time: 14:15 - 15:45 | Room: Forum 7

Organizer:

Ateş Berna - *ElectraIC*

The purpose of this tutorial is to describe verification process flow especially to be used in safety critical ASIC/FPGA designs. Verification of a design consist of two main goals. First one is to verify if the design behaves as described in the requirements. In this process of verification, each requirement is tested and full legal input space is explored. The second goal is to ensure that design does not do anything it is not supposed to do. In general, this process of verification makes sure that every component is tested and illegal conditions are handled. Test scenarios needs to be defined in a Verification Procedure Document. It is important and crucial that Verification Procedure Document verifies all defined requirements, since in a safety critical design (i.e. DO-254, ISO 26262) everything is about tracing all verification activity back to requirements. Therefore, by using a requirements tracing tool like ReqTracer of Mentor Graphics, Requirements and Verification Procedure documents are linked together and is made sure that current test scenarios are verifying all RTL design requirements. Once test scenarios are determined, the next step is to create the verification environment. In this tutorial, design will be verified through Universal Verification Methodology (UVM) and as verification language SystemVerilog is used. After verification environment is created, the next step is to implement test cases. Each test scenario verifies certain requirements. Therefore, it is important to make sure that test case irreproachably verifies corresponding requirements.

In this tutorial verification of requirements with assertions and self-checking mechanism is explained. Self-checking is a mechanism developed by ElectraIC to be used especially in safety critical design verifications. Assertions are used in verification of the occurrence of specific conditions or sequence of events and it is important to be ensured that each assertion correctly is triggered under required conditions and verifies functionality as explained in the corresponding requirement. Due to this reason, each assertion is verified with SVA Unit and is made certain that all assertions operate properly. Test Case simulation results must be supported by functional coverage and code coverage analysis results. Functional coverage is used for design functionality verification and is explicitly defined in the form of a functional coverage model that is composed of assertions and 'cover points', which have certain conditions such as ranges, defined transitions or crosses defined in form of 'bins'. On the other hand code coverage analysis is used to measure test scenario effectiveness and is composed of statement, branch, expression, FSM and toggle coverage analysis. Advanced RTL analysis (linting and structural RTL analysis) is another way to find possible problems in the design. HDL linting, including structural static analysis, improves the quality of RTL and reduces risk earlier in the design cycle, allowing the design to be signed-off with confidence. Therefore, using RTL analysis early in the RTL development phase improves QoR of RTL, accelerates IP verification, decreases development time, and increases productivity to help meet time-to-market deadlines.

In conclusion, this tutorial aims to provide many processes/methods/methodologies of advanced verification in a requirements driven design verification flow.

Speakers:

Ateş Berna - *ElectraIC*
Ahmet Jorganxhi - *ElectraIC*

Thank You to Our Sponsor: ELECTRA IC Design & Verification

Attendee Break

Time: 15:45 - 16:00 | Room: Großer Saal

Located in exhibit hall.

Thank You to Our Sponsor: onespin making electronics reliable

Tutorial 13 - Functional Safety Verification for ISO 26262-Compliant Automotive Designs - What's New and What's Needed

Time: 16:00 - 17:30 | Room: Forum 4

Organizer:

Werner Kerscher - *Synopsys, Inc.*

Automotive has evolved into one the fastest growing parts of the worldwide semiconductor industry, and automotive semiconductor content is exploding, driven by the LED headlights to the many advanced SoCs powering autonomous drive, infotainment, and vehicle communication systems. The "traditional" automotive electronics are not standing still either, with advanced drivetrains and sophisticated safety and ADAS systems creating demand for even-larger and more integrated SoCs

As automotive electronic systems become ever more complex, the potential impact on the safety of vehicle's occupants and bystanders becomes a critical consideration for these systems. ISO 26262, the functional safety standard for road vehicles was created to guide the development of electrical and electronic systems for automobiles, and meeting ISO 26262 compliance needs are rapidly becoming a part of many companies' design and verification requirements. For IP and SoC companies, ISO 26262 product development at the hardware level guidelines are particularly important—from a verification perspective, it lays out a set of requirements for functional safety that need to be understood and followed, and which are in addition to best-practice functional verification methodologies.

State-of-the-art functional safety verification is necessary, but not sufficient for ISO 26262. Functional verification seeks to find and eliminate design-related bugs, which would manifest as systematic faults during product operational lifecycles. In addition, complete functional safety verification must also be performed, with the objective of determining the product's ability to safely manage random faults that may arise during its lifecycle. This is a different verification objective compared to functional verification, and is based on fault injection flows in addition to logic simulation flows.

This tutorial will provide a practical, hands-on overview of the following:

- ISO 26262 considerations for SoC and IP design verification, customer insights and today's challenges
- Unique challenges for automotive SoC and IP verification engineering teams
- New functional verification challenges, solutions and flows
- Functional safety verification
- Failure mode analysis
- Fault injection testing; best practice methodologies for verification engineers
- Annotation of diagnostic data
- Conclusions and QA

Speakers:

Jean-Marc Forey - *Synopsys, Inc.*
Werner Kerscher - *Synopsys, Inc.*

Thank You to Our Sponsor: SYNOPSYS®

Tutorial 14 - Hardware and Software Co-verification in Hybrid HDL Simulation and Emulation Environment with QEMU

Time: 16:00 - 17:30 | Room: Forum 5

Organizer:

Krzysztof Szczur - *Aldec, Inc.*

The FPGA or ASIC SoC require a robust pre-silicon hardware/software co-verification platform. Developing device drivers in pure HDL/RTL simulation environment would be counterproductive and developing or testing embedded operating system and application stack impossible. Virtual platforms and virtual machines have been used by software developers as a high-speed simulation vehicle but they are only appropriate with standard components like CPU, memory, timers and the like. The challenge emerges when custom IP-core is added to the design. Lack of virtual models for custom IP blocks or off-chip devices is a common drawback and the obstacle to complete firmware validation in pure virtual platform and before silicon tape-out. Hybrid co-simulation and then co-emulation of custom HDL blocks with CPU subsystem simulated as virtual machine bridges this gap in verification environment.

QEMU is a generic and open source machine emulator that supports various computer hardware architectures including Intel x86 and ARM® Cortex® families. It can be connected with Aldec's Riviera-PRO™ high performance HDL simulator and HES-DVM™ the FPGA based emulation platform to provide a hybrid co-simulation and co-emulation environment for early hardware/software co-verification and embedded software development.

In this tutorial we will demonstrate the latest QEMU Bridge designed to provide connection between virtual machine of CPU subsystem in QEMU and custom hardware designed in VHDL or Verilog which is simulated in Riviera-PRO or emulated in the HES FPGA board. We will also show how software debugger (GDB) can be used in step-lock mode with the Aldec Hardware Debugger to provide holistic view into the entire SoC and so facilitate debugging typical problems that are resulting from design specification being misunderstood by either software or hardware developers or last minute changes introduced in this specification. The QEMU Bridge was designed to integrate with the latest QEMU version that can be obtained from the official github and is extended with the co-simulation and co-emulation hooks by applying Aldec's patch that modifies PCI device tree in QEMU virtual machine. During the tutorial we will explain and discuss the integration layer as well as the functionality of the environment with the benefits it brings to hardware and software verification teams.

Speakers:

Krzysztof Szczur - *Aldec, Inc.*
Radoslaw Nawrot - *Aldec, Inc.*

Thank You to Our Sponsor: ALDEC THE DESIGN VERIFICATION COMPANY

Tutorial 15 - Unifying Mixed-Signal and Low-Power Verification

Time: 16:00 - 17:30 | Room: Forum 6

Organizer:

Adam Sherer - *Cadence Design Systems, Inc.*

Electronics design has long included digital, analog, and power. It's enabled us to create the phenomenal array of devices that permeate our lives. More than ever, these design elements are unified on a single chip and the system depends on their integrated functionality. Achieving the performance, quality, and safety metrics needed for commercial and safety-dependent applications will require new technologies and methodologies.

Often, a tutorial with a title such as this one professes a single, grand-unification methodology but doing so for mixed-signal and low-power at this time isn't credible. The electronics industry is driving innovation in both the standards and in IC development space because of the complexity of the problem. While that is happening, we need to get ICs built, verified, and in production so we have a series of immediate challenges we need to address.

As we work on these topics, a general methodology may emerge and along the way we will make each project more efficient with solutions to these challenges. As sample of such challenges includes the following:

- Connectivity verification
- Early/system verification for mixed-signal
- Fast build-time for mixed-signal simulation
- Fast SoC/full-chip simulation
- Mixed-signal and low-power verification
- Mixed-signal coverage reporting and analysis
- Simulation of analog trims
- Testbench-driven (UVM) mixed-signal simulation

The challenges in the list above cover a wide range of topics. From tool level topics to methodology topics, from system level to transistor level. The tutorial will address each of these in general, and then select 3 – 4 topics for an in-depth discussion. For the detailed discussions, we will present an open-source reference design to support a cookbook approach to addressing each challenge.

And standards like Accellera SystemVerilog-AMS, IEEE-1800, Accellera UPF, and IEEE-1801 play an important role in realizing those devices. However, the next generation of devices will require higher performance, more sophisticated power management, higher abstraction, and more. We need to examine the content and application of the Accellera and IEEE standards that enable these mixed signal, low power SoCs to ensure that we are enabling interoperability and defining the requirements for the next generation of electronics.

Attendees to this tutorial will gain practical knowledge they can apply to the development of designs with mixed-signal and low power requirements. These topics, and others that attendees will certainly suggest in this interactive tutorial, will provide the stepping stones the semiconductor industry needs to develop a unifying methodology for mixed-signal and low-power.

Speakers:

Kawe Fotouhi - *Cadence Design Systems, Inc.*
Andre Baguenier - *Cadence Design Systems, Inc.*

Thank You to Our Sponsor: cadence

Tutorial 16 - Using Mutation Coverage for Advanced Bug Hunting and Verification Signoff

Time: 16:00 - 17:30 | Room: Forum 7

Organizer:

Sergio Marchese - *OneSpin Solutions GmbH*

Modern verification methodologies incorporate multiple coverage solutions. These range from functional to structural coverage, leverage various coverage models, and operate using varied technologies in both the simulation and formal process. The main purpose of these coverage solutions is to establish a signoff metric that indicates when enough verification has been performed. However, as coverage approaches have evolved, new use models have emerged for these tools that increase their value in the verification process.

Mutation coverage is a relatively new technique pioneered by formal and simulation providers. The approach is to pose the question: if my design is fully covered by a specific testbench or assertion set, then if I change something in the design, the tests should detect this change. If they don't then the area of change is not covered. The approach is widely regarded as a highly effective method for establishing both structural and functional coverage, and is used in design flows where high verification confidence is mandatory.

The exhaustive nature of formal further improves the value of mutation coverage and allows for useful information on the source of uncovered scenarios to be obtained. This opens up a new use model in the area of bug hunting, where coverage tools may be used to analyze complex operational scenarios and detect well-hidden error conditions.

In addition, model-based mutation coverage allows for a meaningful integration of formal and simulation coverage metrics. A long-standing wish of many verification engineers and managers, coverage integration reduces effort overlap between simulation and formal, and enables faster, more rigorous signoff.

Leveraging classic case studies notorious for complex bugs, the attendees will be guided through a range of techniques applicable to many design applications.

The tutorial agenda is as follow:

- Introduction to mutation and formal coverage
- Model-based mutation coverage with formal – it's not so tough!
- Bug hunting using mutation coverage
- Bug hunting on a practical design example
- Signoff with model-based mutation coverage
- Merging formal and simulation coverage metrics

Speaker:

Nicolae Tusinschi - *OneSpin Solutions GmbH*

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DVCon Reception & Expo

Time: 17:30 - 19:00 | Room: Großer Saal

Thank You to Our Sponsor: intel

THURSDAY'S AGENDA

2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

07:30 - 08:00	Welcome Coffee Service *Room: Großer Saal Foyer*			
08:00 - 08:15	Opening Session *Room: Ballsaal*			
08:15 - 09:00	Keynote: Accelerating IoT Device Development - from Silicon to Developer Tools *Room: Ballsaal* **Philippe Magarshack** *STMicroelectronics*			
09:15 - 10:30	Panel: Using Next Generation Methods of Systems MODELLING and VIRTUAL PROTOTYPING to Revolutionise the Design, Verification and Manufacture of High Value, Complex Electromechanical Products across the Automotive Supply Chain *Room: Ballsaal*			
10:00 - 18:30	Exhibit Floor Open *Room: Großer Saal*			
10:30 - 10:45	Attendee Break *Room: Großer Saal*			
10:45 - 12:15	Session 1 - TLM *Room: Forum 4*	Session 2 - SystemC *Room: Forum 5*	Session 3 - UVM 1 *Room: Forum 6*	Session 4 -New Horizons in Functional Verification *Room: Forum 7*
12:15 - 13:15	Luncheon *Room: Großer Saal Foyer*			
13:15 - 14:45	Session 5 - Virtual Prototyping *Room: Forum 4*	Session 6 - Generating Stimulus *Room: Forum 5*	Session 7 - UVM II *Room: Forum 6*	Session 8 - Low Power Design and Verification *Room: Forum 7*
14:45 - 15:15	Attendee Break *Room: Großer Saal*			
15:15 - 16:45	Session 9 - Virtual Platforms and Visualization *Room: Forum 4*	Session 10 - Functional Safety *Room: Forum 5*	Session 11 - Advanced Verification Techniques *Room: Forum 6*	Session 12 - AMS Verification *Room: Forum 7*
16:45 - 17:30	Panel: Accellera Town Hall Meeting and Q&A *Room: Ballsaal*			
17:30 - 18:30	Closing Session & Best Paper Awards *Room: Großer Saal*			

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Welcome Coffee Service

Time: 07:30 - 08:00 | Room: Großer Saal Foyer

Opening Session

Time: 08:00 - 08:15 | Room: Großer Saal Foyer

Keynote: Accelerating IoT Device Development - from Silicon to Developer Tools

Time: 08:15 - 09:00 | Room: Ballsaal

Speaker:
Philippe Magarshack - *STMicroelectronics*

The Internet of Things is accelerating, thanks to the broad availability of affordable building blocks for IoT devices, combined with ubiquitous wireless connectivity, cloud computing and artificial intelligence. ST has a broad offering for developers of IoT devices and applications as well as software and hardware tools to make prototyping and industrialization faster and easier. The development of IoT SoCs pose a number of challenges for chipmakers in order to enable successful first-time silicon and fast bring-up. This talk addresses these topics as well as some of the perspectives for IoT applications.

Biography: Philippe Magarshack is MDG Group Vice President at ST Microelectronics, responsible for Microcontrollers and Digital ICs Group (MDG) Special Projects. From 1985 to 1989, Magarshack worked as a microprocessor designer at AT&T Bell Labs in the USA, after which he joined Thomson-CSF in Grenoble, France, and took responsibility for libraries and ASIC design kits for the military market. In 1994, Magarshack joined the Central R&D Group of SGS-THOMSON Microelectronics (now STMicroelectronics), where he held several roles in CAD and Libraries management for advanced integrated-circuit manufacturing processes. In 2005, Magarshack was appointed Group Vice President and General Manager of Central CAD and Design Solutions at STMicroelectronics' Technology R&D and Manufacturing organization. In 2012, he was promoted to ST's Executive Vice President in charge of Design Enablement & Services. Magarshack has been President of the Minalogic Collaborative R&D Cluster in Grenoble since June 2014. Philippe graduated with an engineering degree in Physics from Ecole Polytechnique, Palaiseau, France, and with an Electronics Engineering degree from Ecole Nationale Supérieure des Télécommunications in Paris, France.

Panel: Using Next Generation Methods of Systems MODELLING and VIRTUAL PROTOTYPING to Revolutionise the Design, Verification and Manufacture of High Value, Complex Electromechanical Products across the Automotive Supply Chain

Time: 09:15 - 10:30 | Room: Ballsaal

Organizer:
Paul Nottingham - *Synopsys, Inc.*

Moderator:
Jim Hogan - *Vista Ventures*

Panel Background: Vehicle design is an area that is currently undergoing significant transformation – new requirements include autonomous driving, active safety, infotainment, power train and energy source, vehicular connectivity etc. The result of this is that brand new vehicle platforms are being developed, yielding an enormous amount of new system design and integration, all of which could potentially benefit from the application of higher level virtual prototypes of the full platform and integrated systems.

Panel Objectives: The panel consists of industry experts in their respective domain from the automotive supply chain (e.g. OEMS, IDMs, EDA, CAD, IP suppliers) to discuss and debate how the Automotive industry could strengthen their collaboration to enhance and agree on new design and verification methodologies, including model-based design, virtual prototypes, IP / design reuse, as well as the application of new standards and infrastructure, etc., to support an efficient development cycle from virtual prototypes to real products

Panelists:
Matthieu Worm - *Siemens PLM Software Inc.*
Ralf Schleifer - *Audi AG*
Josef Eckmueller - *Intel Corp.*
Ingo Feldner - *Bosch Research*
Thomas Rühlicke - *Infineon Technologies AG*

Exhibit Floor Open

Time: 10:00 - 18:30 | Room: Großer Saal

Attendee Break

Time: 10:30 - 10:45 | Room: Großer Saal

Session 1 - TLM

Time: 10:45 - 12:15 | Room: Forum 4

Chair:
Cyril Spasevski - *Onomia*

User experiences from simulations based on Transaction Level Modeling.

1.1 Using UVM-ML Library to Enable Reuse of TLM2.0 Models in UVM Test Benches
Sarmad J. Dahir, Hans-Martin Bluethgen, Rafael Zuralski, Nils Luetke-Steinhorst, Christian Sauer - *Cadence Design Systems,GmbH*

1.2 Acceleration of Product and Test Environment Development using SystemC-TLM.
Florian Barrau, Alexandre Piccini - *Schneider Electric*
Mark Burton, Luc Michel - *GreenSocs Ltd*
Alexandre Nabais Moreno - *Schneider Electric*
Clement Deschamps - *GreenSocs Ltd*

1.3 Performance Modeling and Timing Verification for DRAM Memory Subsystems
Thomas Schuster, Peter Prueller, Christian Sauer - *Cadence Design Systems,GmbH*

Session 2 - SystemC

Time: 10:45 - 12:15 | Room: Forum 5

Chair:
Mark Burton - *GreenSocs Ltd*

New twists on SystemC.

2.1 Hardware Construction with SystemC
Roman Popov, Mikhail Moiseev - *Intel Corp.*

2.2 Increasing Efficiency and Reuse in Modeling SystemC/TLM IPs Targeting Virtual Prototypes for Software Development
David Spieker, Thomas Schuster, Rafael Zuralski, Christian Sauer - *Cadence Design Systems,GmbH*

2.3 A Hybrid Channel for Co-Simulation of Behavioral SystemC IP with its Full System Prototype on FPGA
Antonis Papagrigoriou, **Miltos D. Grammatikakis**, Voula Piperaki - *Technological Educational Institute of Crete*

Session 3 - UVM I

Time: 10:45 - 12:15 | Room: Forum 6

Chair:
Alexander Rath - *Infineon Technologies*

New Ideas on UVM.

3.1 Extending Functionality of UVM Components by using Visitor Design Pattern
Darko M. Tomusilovic - *VTool Ltd.*

3.2 UVM Register Map Dynamic Configuration
Matteo Barbati, Alberto Allara - *STMicroelectronics*

3.3 Clustering and Classification of UVM Test Failures using Machine Learning Techniques
Andy Truong, Daniel Hellström, Harry Duque, **Lars Viklund** - *Axis Communications AB*

Session 4 - New Horizons in Functional Verification

Time: 10:45 - 12:15 | Room: Forum 7

Chair:
Harry Foster - *Mentor, A Siemens Business*

How Engineers are tackling the Verification Problems of tomorrow's SOCs.

4.1 Advanced Techniques to Accomplish Power Aware CDC Verification
Ashish Hari - *Mentor, A Siemens Business*
Rohit K. Sinha - *Intel Technology India Pvt. Ltd*
Sulabh K. Khare - *Mentor, A Siemens Business*

4.2 Guiding Functional Verification Regression Analysis using Machine Learning and Big Data Methods
Eman El Mandouh - *Mentor, A Siemens Business*
Laila Maher, Moutaz Ahmed, **Yasmin ElSharnoby**, Amr G. Wassal - *Cairo Univ.*

4.3 Hybrid Flow: A Smart Methodology to Migrate from Traditional Low Power Methodology
Rohit K. Sinha - *Intel Technology India Pvt. Ltd*
Prashanth N - *Intel Corp.*

Lunch

Time: 12:15 - 13:15 | Room: Großer Saal

Session 5 - Virtual Prototyping

Time: 13:15 - 14:45 | Room: Forum 4

Chair:
Tim Kogel - *Synopsys, Inc.*

The latest techniques for Virtual Prototyping.

5.1 Fast and Furious: Quick Innovation from Idea to Real Prototype
Simone Fontanesi, Gaetano Formato - *Infineon Technologies*
Thomas Arndt - *COSEDA Technologies*
Andrea Monterastelli - *Infineon Technologies*

5.2 Temporal Decoupling – Are "Fast" and "Correct" Mutually Exclusive?
Jakob Engblom - *Intel Corp.*

5.3 Generating Bus Traffic Patterns
Jacob Sander S. Andersen - *SyoSil ApS*
Lars Viklund - *Axis Communications AB*
Kenneth Branth - *SyoSil ApS*

Session 6 - Generating Stimulus

Time: 13:15 - 14:45 | Room: Forum 5

Chair:
Matthias Bauer - *Infineon Technologies*

Interesting Approaches for Generating Meaningful Stimulus.

6.1 Portable Stimulus Driven SystemVerilog/UVM Verification Environment for the Verification of a High-capacity Ethernet Communication Endpoint
Andrei Vintila, Ionut Tolea - *AMIQ srl*

6.2 Use Stimulus Domain for Systematic Exploration of Time Dimension and Automatic Testcase Construction
Ning Chen, Martin Ruhwandl - *Infineon Technologies AG*

6.3 MicroTESK: Automated Architecture Validation Suite Generator for Microprocessors
Mikhail Chupilko, **Alexander Kamkin**, Alexander Protsenko, Sergey Smolov, Andrei Tatarnikov - *Ivannikov Institute for System Programming of the RAS*

Session 7 - UVM II

Time: 13:15 - 14:45 | Room: Forum 6

Chair:
Uwe Simm - *Cadence Design Systems, Inc.*

New Ideas on UVM (again).

7.1 Automated Configuration of Verification Environments using Specman Macros
Dejan Janjic, **Milos Mirosavljevic** - *Veriest*
Ron Sela - *Valens Semiconductor Ltd.*
Efrat Shneydor - *Cadence Design Systems, Inc.*

7.2 Characterizing RF Wireless Receivers Performance in UVM Environment
Salwa Elqassas, Mohammed T. Abdel-Hafez, **Ahmed Nasr** - *Silicon Vision*

7.3 Multi-Variant Coverage: Effective Planning and Modelling
Vikas Sharma, Manoj Manu, **Dirk Hansen** - *Mentor, A Siemens Business*

Session 8 - Low Power Design and Verification

Time: 13:15 - 14:45 | Room: Forum 7

Chair:
Mohammad A. Fahim - *Intel Corp.*

How people ensure that their SOCs consume less power (and verify it).

8.1 IEEE 1801 Assisted Custom IP Development and Low Power Checks using Cadence Virtuoso Power Manager
Matthias Steffen - *Infineon Technologies AG*
Amit Chopra - *Cadence Design Systems, Inc.*
Sonal Singh - *Cadence Design Systems, India Pvt. Ltd.*

8.2 A New Approach to Low-power Verification: Low Power Apps
Madhur Bhargava - *Mentor Graphics (India) Pvt. Ltd.*
Awashesh Kumar - *Mentor, A Siemens Business*

8.3 UPF Power Models: Empowering the Power Intent Specification
Amit Srivastava, Harsh Chilwal - *Synopsys, Inc.*

Attendee Break

Time: 14:45 - 15:15 | Room: Großer Saal

Session 9 - Virtual Platforms and Visualization

Time: 15:15 - 16:45 | Room: Forum 4

Chair:
Philipp A. Hartmann - *Intel Corp.*

Advanced Approaches based on Virtualization and Visualization.

9.1 Same Bits, Different Meaning – When Direct Execution based Simulation Becomes Complicated
Evgeny Yulyugin - *Intel Corp.*

9.2 Intelligent Virtual Platforms
Ola Dahl, Mikael Eriksson, Udayan Prabir Sinha, Daniel Haverås - *Ericsson*

9.3 Enabling Visual Design Verification Analytics - From Prototype Visualizations to an Analytics Tool using the Unity Game Engine
Markus Borg - *Swedish Institute of Computer Science*
Andreas Brytting - *KTH Royal Institute of Technology*
Daniel Hansson - *Verifyter AB*

Session 10 - Functional Safety

Time: 15:15 - 16:45 | Room: Forum 5

Chair:
Clemens Roettgermann - *NXP Semiconductors*

Coping with formalities. This session deals with how Verification Engineers ensure that their approaches keep up with the most challenging safety standards.

10.1 Efficient Fault Injection Methods for Safety Software Testing based on Virtual Prototypes: Application to Powertrain ECU
Ons Mbarek - *Robert Bosch GmbH*
Dineshkumar Selvaraj - *Infineon Technologies AG*
Romero Chica Jose Miguel, Rajagopal Shenoy, Holger Riethmueller - *Robert Bosch GmbH*

10.2 Improving the Confidence Level in Functional Safety Simulation Tools for ISO 26262
Ahmet Cagri Bagbaba, Felipe A. da Silva, Christian Sauer - *Cadence Design Systems,GmbH*

10.3 Qualification of a Verification IP under Requirement based Verification standards: An Approach to the Verification of the Verification
Francois Cerisier, Adrien Carmagnat - *Aedvices Consulting*
Alessandro Basili, Gilles Curchod - *Melexis*

Session 11 - Advanced Verification Techniques

Time: 15:15 - 16:45 | Room: Forum 6

Chair:
Raik Brinkmann - *OneSpin Solutions GmbH*

Advanced Approaches to solve unusual Verification Problems.

11.1 Use of Formal Methods for Verification and Optimization of Fault Lists in the Scope of ISO26262
Felipe A. da Silva, Ahmet Cagri Bagbaba, - *Cadence Design Systems,GmbH,*
Said Hamdioui, *Delft Univ. of Technology*
Christian Sauer, *Cadence Design Systems,GmbH*

11.2 Formal Verification of a Highly Configurable DDR Controller IP
Sumit Neb - *Synopsys, Inc.*
Chirag Agarwal, Deepak K. Gupta, **Roger Sabbagh** - *Oski Technology, Inc.*

11.3 Fault Effect Propagation using Verilog-A for Analog Test Coverage
Aishwarya Prabhakaran, **Ahmed Sokar**, Jaafar Mejri - *Infineon Technologies AG*

Session 12 - AMS Verification

Time: 15:15 - 16:45 | Room: Forum 7

Chair:
Karsten Einwich - *COSEDA Technologies*

User Experiences on AMS Verification.

12.1 Using Constraints for SystemC AMS Design and Verification
Thilo Vörtler, Karsten Einwich - *COSEDA Technologies*
Muhammad Hassan - *DFKI*
Daniel Grosse - *University of Bremen & DFKI GmbH*

12.2 Methodology for Automated Generation and Validation of Analog Behavioral Models for Mixed-Signal Verification
Nan Ni, Chunya Xu - *Infineon Technologies AG*
Sebastian Simon - *Infineon Technologies*

12.3 Protocol Verification of an IEEE 802.3bw PHY
Joen C. Westendorp, Marcel Oosterhuis - *NXP Semiconductors*

Panel: Accellera Town Hall Meeting and Q&A

Time: 16:45 - 17:30 | Room: Ballsaal

The Accellera town hall meeting is the concluding event at DVCon Europe where all conference participants are invited to interact with the Accellera Systems Initiative leadership team and working group members to discuss standardization opportunities and challenges. During this session, Accellera will give a short summary of the ongoing standardization developments happening in the various working groups. Members of the Accellera Board of Directors and working groups are available to answer questions from the audience and discuss important standardization initiatives.

This Q&A session offers a unique opportunity to articulate your needs, requirements and expectations related to design and verification methodologies, languages and standards. It will give you additional insights on what is happening in the Accellera working groups which are defining the standards of tomorrow! We invite you to participate in this Q&A session and if you are interested to contribute to the standardization yourself, this event can bring you in contact with the standardization experts to join one of the working groups.

Closing Reception & Best Paper Awards

Time: 17:30 - 18:30 | Room: Großer Saal

All Full Conference registrants are entitled to vote for the "DVCon Europe Best Paper" awards. The attendees are the judges! Place your votes on Thursday. Best Paper announced at 17:30 in the Expo Hall. https://dvcon-europe.org/vote

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Exhibit Hours:

Wednesday, October 24.....10:00 - 19:00
Thursday, October 25.....10:00 - 18:30

DVCON EUROPE 2018 EXHIBITORS*

** As of 9/28/2018*

ATTENDEE BREAKS

Location: Großer Saal

Wednesday, October 24

11:30 – 11:45

15:45 - 16:00

Thursday, October 25

10:30 - 10:45

14:45 - 15:15

16:30 – 16:45

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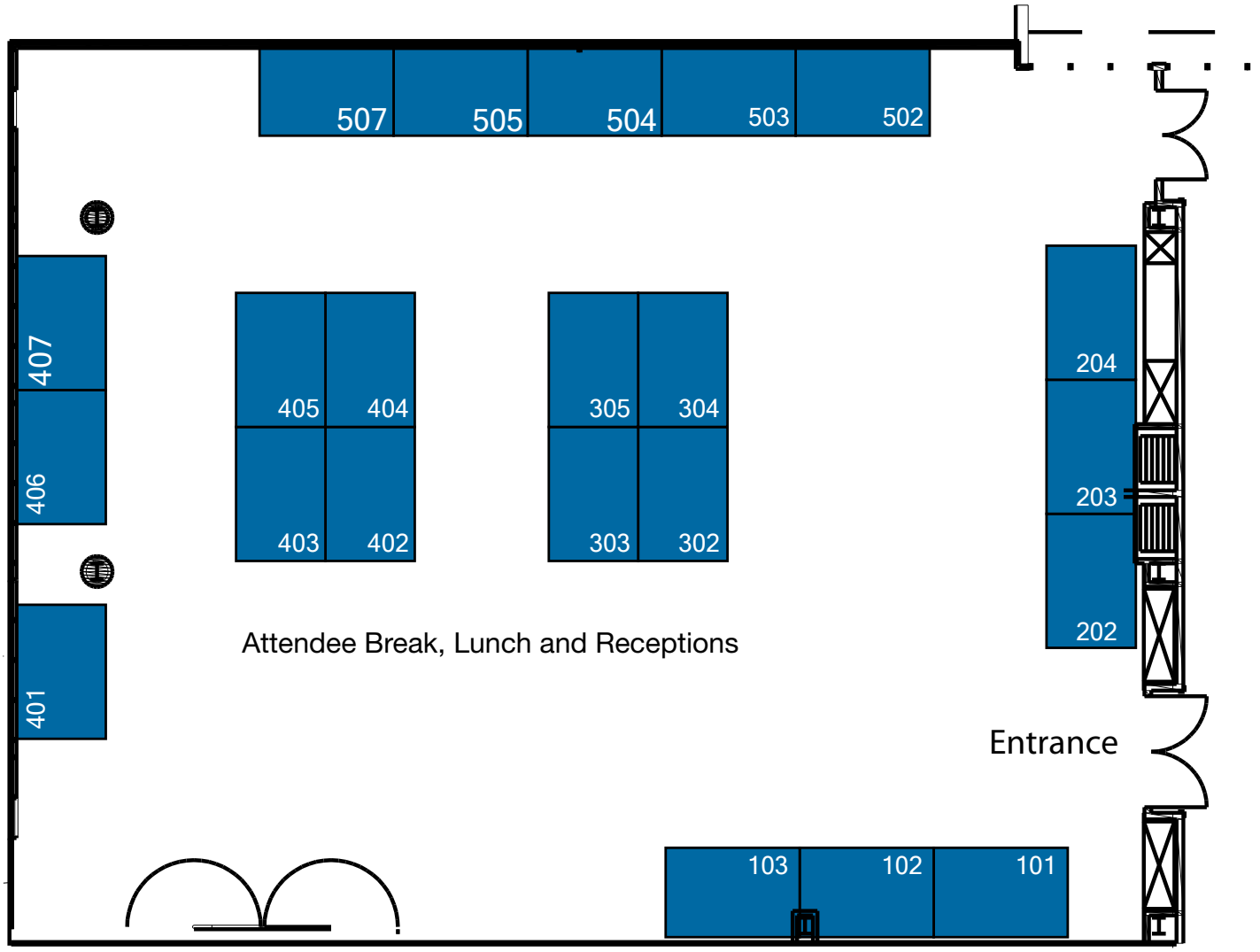
EXHIBIT FLOORPLAN



EXHIBITORS

Agnisys, Inc.

Booth: 305 | www.agnisys.com

Agnisys Inc. is a leading supplier of Electronic Design Automation software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for system-on-chip and intellectual property enabling faster design, verification, firmware, and validation. Agnisys is based in Boston, Massachusetts, with R&D centers in the United States and India.

Aldec, Inc.

Booth: 403 | www.aldec.com

Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design and Mixed-Language Simulation (VHDL, Verilog, SystemVerilog/UVM), FPGA-based Hardware-Assisted Verification, SoC and ASIC Prototyping, Emulation, Design Rule Checking, Clock Domain Crossing, VIP Transactors, Requirements Lifecycle Management, Embedded Development Kits, High-Performance Computing/Acceleration, DO-254 Functional Verification and Military/Aerospace solutions.

AMIQ EDA

Booth: 302 | www.amiq.com

AMIQ EDA provides software tools that enable design and verification engineers, increase the speed and quality of new code development, simplify legacy code maintenance, accelerate language and methodology learning, and improve source code reliability. The company is recognized for its high quality solutions - DVT Eclipse IDE, DVT Debugger Add-On, Verissimo Linter and Specador Documentation Generator - and customer service responsiveness. Websites: www.amiq.com; www.dvteclipse.com

ANKASYS

Booth: 304 | www.ankasys.com

ANKASYS is a microelectronic design and verification company providing advanced design and verification services to its customers from specification to final ASIC GDS or FPGA based embedded systems. The two co-founders bring more than two decades of ASIC/FPGA design and verification experience. The company provides design and verification trainings targeting mainly FPGA-based design, Verilog/SystemVerilog language and the application of the OVM/UVM methodology.

Avery Design Systems, Inc.

Booth: 505 | www.avery-design.com

A leader in Verification IP providing robust models, compliance testsuites, and services for PCI Express, USB/xHCI, UFS/UFSHCI, NVMe/f, SATA Express, SATA, UniPro, Soundwire, Sensewire, CSI/DSI, HDMI, DP, eMMC, SDIO, DDR4/LPDDR4, HBM, HMC, ONFI/Toggle, CAN FD, LIN, FlexRay, and ACE/AXI3/AXI4/AHB. A leader in verification tools. SimXACT automatically eliminates X bugs in RTL and gate-level simulation. ResetOPT minimizes reset/retention design overhead.

Breker Verification Systems, Inc.

Booth: 405 | www.brekersystems.com

Breker uses a single, comprehensible, executable intent specification based on enhanced Portable Stimulus, for easy and fast scenario modeling. An AI-driven test synthesizer converts abstract scenario models into rigorous portable test sets that rapidly detect complex bugs. Breker's unique deployment models allow the tests to be loaded into existing UVM & SoC environments with zero modification.

Cadence Design Systems, Inc.

Booth: 103 | www.cadence.com

Cadence® software, hardware and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work and play. The company's System Design Enablement strategy helps customers develop differentiated products—from chips to boards to systems. Learn more at cadence.com.

CircuitSutra Technologies Pvt Ltd.

Booth: 407 | www.circuitsutra.com

Circuitsutra is an Electronics System Level (ESL) design IP & Services company, headquartered in India, having development centres in Noida & Bangalore, and serves the customers worldwide. It enables customers to adopt advanced methodologies based on C, C++, SystemC, TLM, IP-XACT, UVM-SystemC, SystemC-AMS. Its core competencies include virtual prototype (development, verification, and deployment), Architecture & Performance modelling, co-simulation, co-emulation, HLS, SoC & System verification.

COSEDA Technologies GmbH

Booth: 101 | www.coseda-tech.com

COSEDA Technologies provides software solutions in the field of system level design for complex electronic hard- & software products based on SystemC and SystemC AMS. We make latest modelling and simulation technologies available for our customers to enable them to master new concepts cost-effectively for innovative, complex and safety-critical products.

Doulos

Booth: 202 | www.doulos.com

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HDL Design House

Booth: 504 | www.hdl-dh.com

HDL Design House delivers leading-edge front end digital design/verification services, analog and back end services in numerous areas of SoC/FPGA. The company also develops IP cores and turn-key solutions using state of the art Cadence EDA tools. HDL DH joined the ARM® Approved Design Partner program, through which leading SoC design houses are recognized by ARM as accredited partners in specific technologies.

EXHIBITORS

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MathWorks is the leading developer of mathematical computing software. MATLAB is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink is a graphical environment for simulation and Model-Based Design. Engineers and scientists worldwide rely on these product families to accelerate the development of electronics and semiconductors in automotive, aerospace, communications and other industries..

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OneSpin Solutions
Booth: 402 | www.onespin.com

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Real Intent, Inc.
Booth: 203 | www.realintent.com

Real Intent is the leading provider of EDA software to accelerate Early Functional Verification and Advanced Sign-off of digital designs. It provides comprehensive clock-domain crossing verification, advanced RTL analysis and sign-off solutions to eliminate complex failure modes of SoCs. Our Verix, Meridian, and Ascent product families lead the market in performance, capacity, accuracy and completeness

SmartDV Technologies India Private Ltd.
Booth: 303 / www.smart-dv.com

SmartDV offers high quality standard and custom protocol Verification IPs, Memory Models, Simulation Acceleration IPs and Design IPs covering MIPI, Networking, Video, Storage, Automotive, SOC areas. The VIPs and IPs are licensed to 120+ customers all around the world. SmartDV also offers design and verification services in the area of ASIC and FPGA design, with emphasis on quality deliverable. SmartDV VIPs are 2-4x faster to compile and simulate compared to our competition.

Synopsys, Inc.
Booth: 401 | www.synopsys.com

Synopsys is the Silicon to Software partner for innovative companies developing electronic products and software applications. Synopsys' Verification Continuum combines best-in-class technology, including simulation, verification IP, emulation, advanced debug, static and formal verification, prototyping and virtual prototyping, with advanced methodologies enabling users to address rapidly escalating SoC complexity, accelerate time-to-market and bring products to market sooner.

Test and Verification Solutions Ltd
Booth: 406 | *www.testandverification.com*

T&VS helps companies create products that are reliable, safe and secure. TVS has many years of experience delivering verification services from hardware and firmware, through embedded software and middleware to software applications. T&VS has global offices offering services onsite, offshore or a mix, allowing T&VS meet cost objectives to support DfT, analog, verification, Si validation, telecoms testing, safety, security, etc.

Veriest Solutions Ltd.
Booth: 404 | www.veriests.com

Veriest is a design house providing ASIC/FPGA engineering services. Our clients are industry leaders and startups developing high-end chip technology. With headquarters in Israel and R&D centers in Serbia, our 100+ engineers have made their mission to provide customers with superior solutions that include architecture design, design implementation for digital/mixed-signal designs, system modelling, functional and formal verification and embedded software.

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Booth: 102 | www.verifyter.com

Verifyter develops and sells PinDown, an automatic debugger of regression failures. Using machine learning, PinDown quickly identifies the bad code and validates the debug analysis by making the failing test pass again.

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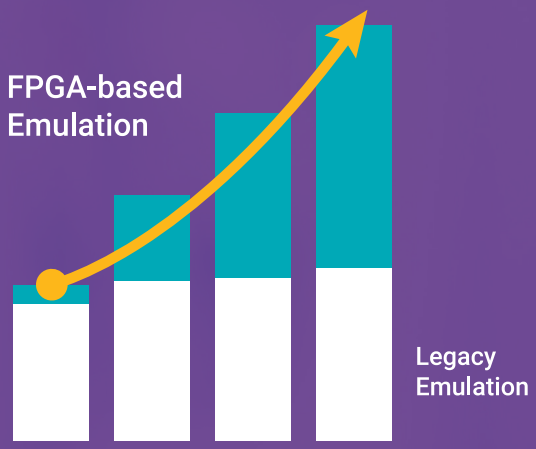

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