



Sponsored by:



HOLIDAY INN MUNICH CITY CENTRE | OCTOBER 16-17, 2017  
DVCON-EUROPE.ORG

# CONFERENCE PROGRAM



# WELCOME TO DVCON EUROPE 2017



## DVCon Europe 2017

### Welcome Message from DVCon Europe General Chair, Oliver Bell

**General Chair - Intel**

I'm pleased to welcome you to the 2017 edition of the Design and Verification Conference & Exhibition Europe, October 16-17, 2017.

This year's DVCon Europe continues its tradition with an exciting lineup, with both days packed with tutorials, panels, keynotes, technical presentations, and an attractive exhibition. Each day will begin with a keynote held by a prominent Industry speaker.

Mr. Horst Symanzik from Bosch Sensortec will kick off DVCon on Monday with his keynote, "Consumer MEMS Products: Quality rather than Commodity" an overview about some of the challenges in the ASIC development for current and future MEMS products and how to tackle these challenges while originating from a mixed-signal heritage.

The focus on Monday will be on a rich tutorial program with 16 tutorials, given by user-companies, standardization experts, consultancy companies, universities or EDA tool providers. We'll also introduce an evening reception at the extended DVCon Europe Exhibition.

On Tuesday, Mr. Berthold Hellenthal from Audi will present, "Driving Virtual Prototyping of Automotive Electronics." Berthold will highlight ongoing developments and challenges for the increased usage of Virtual Prototypes at the automotive domain, to keep up with the development speed of consumer electronics, despite different system levels, value chains and development processes.

Further highlights on Tuesday include the panel "The Best Tools for Driving Safety and Security in Automotive Applications", right after the keynote and one panel in the afternoon to provide answers to "Intelligent Automation: How to Decide What to and What not to Automate?".

For the first time, DVCon Europe will feature a 5G special interest session, with industry experts from Intel, Nokia and Rohde & Schwarz, who will provide insights on the path to 5G, highlight Spectrum opportunities and challenges, and offer also a Test

& Measurement perspective for the emerging next generation of cellular communication.

The DVCon keynotes, papers, presentations and panels unite the practical application of state-of-the-art design and verification techniques, applied to a broad mixture of different domains. Primary areas of this year's program include System Level, Virtual Prototyping, Advanced Verification with UVM and Formal, Design for Functional Safety, IP Reuse, Mixed-Signal and Low Power Techniques. Please vote for your favorite DVCon 2017 paper for the closing session.

The exhibition at DVCon Europe is an integral part of the conference and we welcome all exhibitors presenting their EDA tools, services and solutions. Feel free to interact with the exhibitors on both days - maybe the solution for your current design or verification problem will be shown!

Adjacent to DVCon Europe, we will also have the 2nd edition of Accellera's SystemC Evolution Day, following its successful launch last year. This "spinoff" from DVCon Europe will take place October 18th at the Technical University of Munich.

DVCon Europe is a great opportunity to meet and connect with the DVCon community, which includes experts from different companies, fields and countries, design automation tool users and vendors, senior fellows and freshmen, as well as researchers and many more.

Finally, I would like to thank all the sponsors, exhibitors and the many volunteers, authors, presenters, panelists, reviewers and steering team members, who work hard year-round to shape an interesting and high-quality program. It's amazing for me to see this fantastic collaboration throughout the industry to make DVCon Europe happen.

The DVCon Europe Steering Committee and the Accellera Systems Initiative welcome you from the heart at downtown Munich. Enjoy DVCon Europe!

# TABLE OF CONTENTS

## GENERAL CHAIR'S WELCOME.....2

Conference Sponsor.....4

DVCon Europe 2017 Committees .....5

Conference Details .....6

## MONDAY'S AGENDA..... 8

Monday's Session Details .....10

## TUESDAY'S AGENDA .....19

Tuesday's Session Details.....20

## DVCON EUROPE 2017 EXPO .....25

Thank You to Our Sponsors.....25

Exhibitor Listing & Floorplan .....26

Exhibitor Details.....28



# CONFERENCE SPONSOR



Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other “smart” electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

## Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

## Membership

Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at [www.accelera.org](http://www.accelera.org).

## Accellera Global Sponsors

cādence®

Mentor®  
A Siemens Business

SYNOPSYS®

# 2017 COMMITTEES

## STEERING COMMITTEE



### GENERAL CHAIR

**Oliver Bell**  
Intel  
oliver.bell@intel.com



### GENERAL VICE CHAIR

**Thomas Klotz**  
Bosch Sensortec GmbH  
Thomas.Klotz@bosch-sensortec.com



### PANEL CHAIR

**Joachim Geishauser**  
NXP Semiconductor  
joachim.geishauser@nxp.com



### PROGRAM CHAIR

**Matthias Bauer**  
Infineon  
matthias.dvcon@mbtj.de



### TUTORIAL CHAIR

**Martin Barnasconi**  
NXP Semiconductor  
martin.barnasconi@nxp.com



### POSTER CHAIR

**Paul Nottingham**  
ARM Ltd.  
Paul.Nottingham@arm.com



### PROMOTIONS CHAIR

**Dave Kelf**  
OneSpin Solutions  
dave.kelf@onespin-solutions.com



### ACCELLERA REPRESENTATIVE / FINANCE CHAIR

**Lynn Garibaldi**  
Accellera  
lynn@accellera.org



### CONFERENCE MANAGEMENT

**Susie Horn**  
MP Associates  
Susie@MPAssociates.com



### CONFERENCE MANAGEMENT

**Terri MacKenzie**  
MP Associates  
Terri@mpassociates.com

## TECHNICAL PROGRAM COMMITTEE



### PROGRAM CHAIR

**Matthias Bauer**  
Infineon  
matthias.dvcon@mbtj.de

**Ali Haydar Akbaba**  
Texas Instruments, Inc.

**Jerome Cornet**  
STMicroelectronics

**Thorsten Klose**  
Infineon Technologies AG

**Giuseppe Scata**  
Apple, Inc.

**Rafal Baranowski**  
Robert Bosch GmbH

**Philippe Cuenot**  
Continental AG

**Daniele Ludovici**  
Intel Corporation

**Uwe Simm**  
Cadence Design Systems, Inc.

**Mike Bartley**  
Test and Verification Solutions

**Guy Dupenloup**  
STMicroelectronics

**Laurent Maillet-Contoz**  
STMicroelectronics

**Manfred Thanner**  
NXP Semiconductors

**Rafael Pena Bello**  
Apple, Inc.

**Wolfgang Ecker**  
Infineon Technologies AG

**Akshaya Narayanan**  
Infineon Technologies AG

**Walter Tibboel**  
NXP Semiconductors

**Staffan Berg**  
Mentor, A Siemens Business

**Karsten Einwich**  
COSEDA Technologies

**Jasminka Pasagic**  
Texas Instruments, Inc.

**Darko Tomusilovic**  
Veriest Vtool

**Stefan Birman**  
AMIQ srl

**Mohammad Fahim**  
Intel Corporation

**Alexander Rath**  
Infineon Technologies AG

**Joen Westendorp**  
NXP Semiconductors

**Raik Brinkmann**  
OneSpin Solutions GmbH

**Bill Flanders**  
ARM, Inc.

**Horst Rieger**  
Renesas Electronics Europe GmbH

**Thomas Wilde**  
Intel Corporation

**Mark Burton**  
GreenSocs Ltd

**Harry Foster**  
Mentor, A Siemens Business

**Clemens Roettgermann**  
NXP Semiconductors

**Yang Xu**  
Intel Corporation

**Moomen Chaari**  
Infineon Technologies AG

**Alan Hunter**  
ARM, Inc.

**Christian Sauer**  
Cadence Design Systems, Inc.

# CONFERENCE DETAILS

## REGISTRATION HOURS

**Location: Foyer Großer Saal**

Monday, October 16 ----- 07:30 - 19:30

Tuesday, October 17----- 07:30 - 18:00

Thank You to Our Sponsor:



## DVCON EUROPE 2017 EXPO

**Location: Großer Saal**

Monday, October 16 ----- 10:00 - 19:00

Tuesday, October 17----- 10:00 - 18:30

## TUTORIALS & PROCEEDINGS DISTRIBUTION

DVCon Conference Papers and Tutorial presenter slides will be delivered electronically online via a username and password.

To access: <http://proceedings.dvcon-europe.org>

Username and password will be provided to registered conference attendees

## ATTENDEE COFFEE BREAKS

**Location: Großer Saal**

**Monday, October 16**

08:00 - 08:30

11:00 - 11:30

15:30 - 16:00



Thank You to Our Sponsor:

**Tuesday, October 17**

07:30 - 08:00

10:00 - 10:30

14:30 - 15:00

## NETWORKING RECEPTIONS

**Location: Großer Saal**

One of the main reasons you came to DVCon: NETWORKING! Introduce yourself and leave DVCon with a deeper professional network!

Monday, October 16 ----- 17:30

Tuesday, October 17----- 17:30

Thank You to Our Sponsor:



## SOCIAL MEDIA AT DVCON EUROPE



Follow [@DVConEurope](https://twitter.com/DVConEurope) on Twitter and tweet [#DVConEurope](https://twitter.com/DVConEurope) about your experience and highlights at the conference!

Don't miss DVCon on Facebook at

<https://www.facebook.com/DVCon-Europe-898352006944641/>.

## WIRELESS INFORMATION

Enjoy free Wi-Fi at DVCon Europe! Connect to the Conference Wi-Fi via:

**Wi-Fi SSID: DVCon2017**

**Password: DVCE2017**

## BEST PAPER VOTING

Vote for your favorite paper using the SurveyMonkey link:

<https://www.surveymonkey.com/r/BPEurope17>

All votes need to be completed by 17:30 on Tuesday, to be tallied. Award will be announced in the closing ceremony from 17:30 to 18:15 on Tuesday, October 17, in Exhibit Hall.

## AWARDS PRESENTATION

Join us on Tuesday, October 17 at 17:30 in the Exhibit Hall for the Closing Ceremony and announcement of the Best Paper Awards.

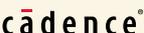
Thank You to  
Our Sponsor:



## CONFERENCE FLOORPLAN



# MONDAY'S AGENDA

08:00 - 08:30	 <b>Attendee Coffee Break</b> <i>Room: Großer Saal Foyer</i>				Thank You to Our Sponsor: 
08:30 - 09:30	<b>Consumer MEMS Products: Quality Rather than Commodity</b> <i>Room: Ballsaal</i>				
09:30 - 11:00	<b>Tutorial 1 - Formal Verification in the Real World</b> <i>Room: Forum 4</i>	<b>Tutorial 2 - Advancing the SystemC Ecosystem</b> <i>Room: Forum 5</i>	<b>Tutorial 3 - An Introduction to the Accellera Portable Stimulus Standard</b> <i>Room: Forum 6</i>	<b>Tutorial 4 - Generation of (at least) UVM Register Models from IP-Xact Using Model Driven SW Techniques</b> <i>Room: Forum 7</i>	
10:00 - 19:00	<b>DVCon Europe Expo</b> <i>Room: Großer Saal</i>				
11:00 - 11:30	 <b>Attendee Coffee Break</b> <i>Room: Großer Saal Foyer</i>				Thank You to Our Sponsor: 
11:30 - 13:00	<b>Tutorial 5 - Virtual Prototypes and Platforms - A Primer</b> <i>Room: Forum 4</i>	<b>Tutorial 6 - UVM-SystemC: Migrating Complex Verification Environments</b> <i>Room: Forum 5</i>	<b>Tutorial 7 - ESL Design and Modeling with SystemC AMS (IEEE 1666.1) for Mixed-Signal IoT and Automotive Applications</b> <i>Room: Forum 6</i>	<b>Tutorial 8 - Automatic Firmware Design for Application-Specific Electronic Systems: Opportunities, Challenges and Solutions</b> <i>Room: Forum 7</i>	
13:00 - 14:00	<b>Luncheon</b> <i>Room: Großer Saal Foyer</i>				
14:00 - 15:30	<b>Tutorial 9 - Next Generation ISO 26262-based Design Reliability Flows</b> <i>Room: Forum 4</i>  Thank You to Our Sponsor: 	<b>Tutorial 10 - TLM Modeling and Simulation for NAND Flash and Solid State Drive Systems</b> <i>Room: Forum 5</i>  Thank You to Our Sponsor: 	<b>Tutorial 11 - Using Cadence and MathWorks Tools Together for Mixed-Signal Design and Verification</b> <i>Room: Forum 6</i>  Thank You to Our Sponsor: 	<b>Tutorial 12 - Software Driven Test of FPGA Prototype</b> <i>Room: Forum 7</i>  Thank You to Our Sponsor: 	
15:30 - 16:00	 <b>Attendee Coffee Break</b> <i>Room: Großer Saal Foyer</i>				Thank You to Our Sponsor: 
16:00 - 17:30	<b>Tutorial 13 - Making Cars Safer - One Chip at a Time</b> <i>Room: Forum 4</i>  Thank You to Our Sponsor: 	<b>Tutorial 14 - Leveraging Virtual Prototypes from Concept to Silicon: An Exploration of Best Practices</b> <i>Room: Forum 5</i>  Thank You to Our Sponsor: 	<b>Tutorial 15 - Testbench Automation : How to Create a Complex Testbench in a Couple of Hours</b> <i>Room: Forum 6</i>  Thank You to Our Sponsor: 	<b>Tutorial 16 - Boosting Debug Productivity – Practical Applications of Debug Innovations in a UVM World</b> <i>Room: Forum 7</i>  Thank You to Our Sponsor: 	
17:30	<b>DVCon Europe Reception</b> <i>Room: Großer Saal</i>				Thank You to Our Sponsor: 

THANK YOU TO OUR SPONSORS

## DVCON EUROPE 2017 TUTORIAL SPONSORS





## Keynote: Consumer MEMS Products: Quality Rather than Commodity

**Horst Symanzik**, *Bosch Sensortec*

**Time: 08:30 - 09:30 | Room: Ballsaal**

When it comes to MEMS (Micro Electro Mechanical System) sensors, Bosch is both a pioneer and the world's leading manufacturer. The company developed the underlying semiconductor manufacturing process in house, and has been producing these sensors on an industrial scale for over 20 years now. To date, Bosch sensors can not only be found in most cars but as well in three out of four smartphones worldwide, and 75 percent of Bosch MEMS sensors are now used in consumer electronics applications.

While first early consumer sensor products had only moderate complex signal read out chains for the MEMS sensors, more recent products are more and more driven by advanced ASIC features containing, depending on their field of application, integrated micro controllers, digital signal processors, image pipelines, external components and more. At the same time, also the complexity of the considered MEMS application grew significantly, from terrestrial magnetic, acceleration and yaw sensors to new systems such as the micro mirror.

This keynote will discuss some of the challenges Bosch Sensortec is facing in the ASIC development for current and future MEMS products. Special attention is paid to the changes in the design and verification methodology which became necessary in order to tackle these challenges while originating from a mixed-signal heritage.

**Biography:** Dr. Horst Symanzik has received his Diploma degree in Electrical Engineering (EE) from RWTH Aachen and holds a PhD degree in EE from TU Chemnitz where he was a research associate for MEMS electronic circuit design. He worked in semiconductor industry in several positions as a mixed-signal design engineer, ASIC project manager and wireless IC development manager. In 2007 he joined Bosch Sensortec, the new established MEMS Consumer Sensor branch of Bosch, to build up a non-automotive IC development organization. As the Director of Engineering Integrated Circuits, he has grown his organization in five international locations of the Bosch Consumer ASIC supplier, with more than 5 billion devices in the field.

---

## Tutorial 1 - Formal Verification in the Real World

**Time: 09:30 - 11:00 | Room: Forum 4**

### Organizers:

Jason Sprott - *Verilab Ltd.*

Jonathan Bromley - *Verilab Ltd.*

Building on our well-received foundation-level tutorial Formal Verification - Too Good to Miss presented at DVCon Europe 2016, this year's session will cover some of the more advanced techniques and workflow patterns that have proven valuable in our own formal verification work.

Carefully avoiding mathematical jargon, it aims to demystify some approaches that help to make a formal verification project productive. Black-boxing, using abstractions for counters and other common structures, and exploiting design symmetry are often mentioned, but rarely described in an accessible way. They will all be covered in a practical style, emphasising broad applicability.

In addition to purely technical content, the session will illustrate how to approach the planning and tracking of your formal verification project - concerns that are easily overlooked in the initial enthusiasm of adopting formal.

This tutorial is appropriate for engineers who are embarking on, or part-way through, a project that uses formal verification. It tackles troublesome questions that commonly become challenges for anyone as their experience deepens: how to establish metrics and criteria for project progress, knowing when you're done, overcoming performance and capacity issues, achieving confidence in the robustness and trustworthiness of your formal verification environment, and integrating results from formal into your simulation-based verification flow.

## Tutorial 2 - Advancing the SystemC Ecosystem

Time: 09:30 - 11:00 | Room: Forum 5

### Organizer:

Philipp Hartmann - Intel Corp.

For more than a decade, SystemC has been used by system architects and design engineers. Not only since the inclusion of Transaction Level Modeling (TLM) into the IEEE 1666-2011 SystemC standard, SystemC is the language of choice for virtual prototyping across the industry. In order to meet the needs of today's and tomorrow's electronic systems, advanced system-level design methodologies and the evolution of SystemC-related standards are required. This tutorial gives an overview on the latest advancements to the SystemC ecosystem in the Accellera working groups including an introduction to SystemC 2.3.2. Two additional technical presentations give more in-depth insights on custom protocol modeling at transaction level as well as state-of-the-art high-level synthesis.

### 2T.1 Accellera Update: What's New and Cooking in SystemC Standardization

Philipp A. Hartmann - Intel Corp.

### 2T.2 TLM-Serial: Easy and Intuitive Controller Area Network (CAN) Modeling

Jerome Cornet - STMicroelectronics

Martin Schnieringer - Robert Bosch GmbH

### 2T.3 SystemC for HLS: What Works well for Deployment and Challenges

Frederic Doucet - Qualcomm, Inc.

## Tutorial 3 - An Introduction to the Accellera Portable Stimulus Standard

Time: 09:30 - 11:00 | Room: Forum 6

### Organizers:

Larry Melling - Accellera

Tom Fitzpatrick - Mentor, A Siemens Business

Much of the history of electronic design automation (EDA) has involved replacement of manual effort by automated processes. Place-and-route tools replaced hand layout, logic synthesis supplanted gate-level netlists, and constrained-random testbenches reduced or eliminated hand-written test vectors. Standardized formats used as input to the automation tools include SystemVerilog, Property Specification Language (PSL), and the Universal Verification Methodology (UVM).

In 2014, the Accellera standards organization observed that the level of automation provided by the UVM was insufficient to provide portability across all phases of chip verification. The Portable Stimulus Working Group (PSWG) was formed in December of that year to standardize "portable stimulus" models that can be used to generate tests at multiple integration levels and across multiple verification platforms.

The PSWG will release the first review draft of the portable test and stimulus standard this summer. The group has defined a declarative domain-specific language (DSL) with an alternative semantically-equivalent C++ input format to specify these models. Users can choose either format or mix and match models from different sources, as well as incorporate legacy code into the models via a direct procedural interface.

The new standard will raise the abstraction level of stimulus and test intent specification by modeling resource and data dependencies of behaviors, and composing them into scenarios using flow graphs. The abstract model can be analyzed by tools to solve constraints and dependencies at the scenario level, from which, along with a hardware/software interface library, target implementations may be automatically generated for the desired platforms.

This tutorial is an introduction to the standard, starting with background on the intended scope and defining goals. The main concepts behind the standard will be reviewed, including the key semantics underlying the model formats. Portable stimulus

is not intended as a replacement for the UVM, but rather as a complement to it. The tutorial provides guidance on when and where the new methodology can be applied for maximum benefit on a chip project. Attendees will learn how to:

- Develop abstract, portable test and stimulus models for their chip designs
- Use constraints to guide randomization of both data and control flow
- Create low level driver sequences or reuse existing low-level sequences or drivers in the generation of tests
- Generate tests tuned for IP, subsystem, and full system verification
- Execute the generated tests across all verification engines: virtual platforms, simulation, acceleration, emulation, FPGA prototype, and silicon in the bring-up lab
- Specify and gather coverage metrics at every step to assess verification completeness

The tutorial takes a building-block approach, starting with simple models and showing how these can be expanded and combined for more complex designs and more sophisticated verification scenarios. The ultimate goal is to generate use cases that reflect how the chip will be used in real applications. Attendees will learn how to use the standard to specify and verify realistic system-level behavior, and will leave the tutorial educated on the value of portable stimulus and the basics of the standard.

### Speakers:

Tom Fitzpatrick - Mentor, A Siemens Business

Sharon Rosenberg - Cadence Design Systems, Inc.

David Kelf - Breker Verification Systems, Inc.

Piyush Sukhija - Synopsys, Inc.

Karthick Gururaj - Vayavya Labs Pvt., Ltd.

Thank You to Our Sponsor:



## Tutorial 4 - Generation of (at least) UVM Register Models from IP-Xact Using Model Driven SW Techniques

Time: 09:30 - 11:00 | Room: Forum 7

### Organizer:

Jacob Sander Andersen - *SyoSil ApS*

The tutorial will be a mixture of normal presentation and an ongoing demo/live example to support the presentation.

The topic is “code generation” which is a well-known discipline but done in a more sophisticated way to ease maintenance and re-usability. This is obtained by leveraging from EMF (Eclipse Modelling Framework) and utilizing this framework to build a proper model driven SW flow showing the benefits.

The tutorial will contain 5 sections:

1. Introduction to model driven SW development
2. Introduction to EMF
3. Presentation of the example/demo
4. Demo/example
5. Conclusions/Extensions

The example will use generation of UVM register models from IP-Xact specifications as a driver and each step in the development cycle will be presented and shown live on the screen.

Additionally, how to generate other register formats will also be shown in the demo.

Finally, the tutorial will be ending with information about how model driven SW techniques with EMF can be deployed in other aspects of the ASIC development cycle.

### Speaker:

Jacob Sander Andersen - *SyoSil ApS*

## Tutorial 5 - Virtual Prototypes and Platforms - A Primer

Time: 11:30 - 13:00 | Room: Forum 4

Today’s electronics devices are dominated by ‘system on chips’ (SoCs) where software outweighs more and more in terms of amount of lines-of-code (LOC) and of effort to create and validated it. To allow for short product cycles virtual prototypes and platforms (VPs) are developed to start software development before silicon is available or to validate design decisions during the initial stages of RTL design. This requires the modeling and simulation of the system’s components and environment at various levels of abstraction, representativeness, and accuracy. Certainly the availability of VPs will allow changing the development approach in other areas as well.

This tutorial aims to highlight challenges and opportunities in the development and deployment of VPs from a practical point of view. Use cases are not only in the semiconductor vendor domain but also at its customers.

The first part focuses on the clarification of the terms virtual prototype and virtual platform and sheds some light on the foundation of both. Essential for VP development are standards as well as tools and IPs adhering to them. This allows assembling and developing VPs at various levels of abstraction and accuracy. Various modeling styles like untimed (UT), loosely timed (LT) or approximately timed (AT) can be used and even mixed within a single VP to achieve the desired accuracy and simulation performance.

The second part presents use cases of virtual prototypes and platforms for both semiconductor vendor and their customer. Various engineering groups and roles in the VP development and adoption can be identified, such as IP authors, platform authors/IP integrators, and platform users/SoC integrators/system integrators. During the design phase these groups use VPs (amongst others) for architectural exploration, performance analysis and validation, functional verification and early

software (esp. firmware) development. Depending on these use cases the requirements for VPs are different and there may be trade-offs i.e. between performance and accuracy.

But the availability and use of virtual platforms allows changing the system software development approach for both system integrators and users of the SoCs. Modern software development principles in embedded software development like test-driven-design (TDD) and continuous integration (CI) are enabled by virtual platforms. Using common strategies like Hardware-in-the-loop (HIL) typically don’t scale well enough and impose some fundamental restrictions for these approaches. For the software developer VPs typically provide better debugging capabilities as well as reproducibility and by this ease the development itself. When necessary other pre-silicon environments can be augmented by implementing parts of system as VP, while executing components for instance on FPGAs

Some aspects of the aforementioned possibilities will be illustrated with demonstrations to highlight key features.

The third part of the tutorial will wrap-up and summarize the advantages of using a virtual prototypes and platforms in the discussed use cases over other approaches such as FPGA prototyping, emulation or HIL. Limitations of VPs will be identified and discussed as well as how the various approaches to hardware/software validation and verification augment each other.

### Speakers:

Rocco Jonack - *MINRES Technologies GmbH*

Eyck Jentsch - *MINRES Technologies GmbH*

## Tutorial 6 - UVM-SystemC: Migrating Complex Verification Environments

Time: 11:30 - 13:00 | Room: Forum 5

UVM-SystemC is an implementation of the UVM standard for SystemC and is based on the donation of a proof-of-concept UVM implementation in SystemC to Accellera in 2014. Standardization efforts of UVM for SystemC (named UVM-SystemC) have gained momentum to the point that a public review release was done during end of 2016 and a subsequent release is planned for end of 2017 to incorporate the feedback of the previous release. Since the public review release people have been implementing first verification environments, seeking to replace previously used proprietary verification mechanisms. Experiences gained from these first applications of UVM-SystemC will be used for constructing complex verification environments in productive development and verification stages. Re-usability and robustness will be shown as the prime advantages of using the UVM-SystemC framework for verification efforts in SystemC.

This tutorial will show how a proprietary verification environment is transformed into a UVM-SystemC verification environment using the standardized UVM-mechanisms. This process will be presented in this tutorial over three sections. In the first introductory section, the previously used verification environment will be presented. We will discuss its benefits and drawbacks and the reasons to move to UVM-SystemC. The next step, the migration to the UVM-SystemC verification environment will be presented. We will show how this can be done in a fast manner and where caveats were found. This shows how UVM-SystemC can be used in a productive manner and how re-usability can be achieved to reduce the verification effort while maintaining a high verification quality.

The second part will show how randomization using SCV and CRAVE is introduced to further improve verification confidence. Here we will explicitly refer to last year's UVM-SystemC tutorial about UVM-SystemC and its CRAVE inclusion and show how the presented concepts are applied in a production

environment. We will be showing examples where the user can have fine grained control on the quality of randomization by tweaking the seed used for each simulation run. Additionally, techniques to reproduce a failing randomized scenario will be presented to further improve the usefulness of the testbench setup. The audience will gain useful insights on how to use UVM-SystemC/CRAVE/SCV outside of well-known previously shared examples.

The final section will discuss the outcome of the migration presented in the previous two sections from a proprietary verification environment to UVM-SystemC including randomization by using CRAVE/SCV. This outcome will be measured by using different key performance indicators (KPIs) such as manual effort, simulation speed and re-usability and thus showing the superiority of the standardized approach.

As an informal closing section we will present the ongoing development of the proof-of-concept implementation and the language reference manual to show clearly where UVM-SystemC is headed and what has been already achieved in the past activities. As a closing item, future standardization topics, such as functional coverage, within the Accellera Verification Working Group and further application fields of UVM-SystemC will be discussed to give the audience an outlook.

The intended audience includes managers, system and verification engineers and architects with a basic knowledge in SystemC and/or UVM, who are interested to further improve their system-level verification practices.

### Speakers:

**Stephan Gerth** - *Fraunhofer IIS/EAS*

**Akhila Madhukumar** - *Intel Technology India Pvt. Ltd*



## Tutorial 7 - ESL Design and Modeling with SystemC AMS (IEEE 1666.1) for Mixed-Signal IoT and Automotive Applications

Time: 11:30 - 13:00 | Room: Forum 6

### Organizer:

Karsten Einwich - COSEDA Technologies

This tutorial will present the latest developments and features of the SystemC Analog/Mixed-Signal (AMS) extensions, which has been released as IEEE Standard 1666.1 in 2016. The SystemC AMS standard is defined in a language reference manual (LRM) defined as C++ class library, which can be used for electronic system-level (ESL) design and modeling for use by system architects and engineers, who need to address complex heterogeneous systems that are a hybrid between analog, digital and software components.

The tutorial will start with a brief introduction of the IEEE Standard 1666.1-2016 and present the capabilities of the SystemC AMS extensions. Especially, the different models of computation to model analog behavior at a higher level of design abstraction are explained.

Then, the tutorial will present modelling patterns for practically using the SystemC AMS extensions for system-level design and verification. The various use cases for the application of SystemC AMS and their relation to the different modeling formalisms are explained. Using some basic examples, the most elementary modeling concepts and main features are highlighted.

The tutorial will feature application examples from the automotive and Internet of Things (IoT) domain, which will

demonstrate how to apply fault injection and modeling of analog inaccuracies at the system-level.

The tutorial will conclude with pointers on how to use SystemC AMS modeling in your daily work as well as how to update or extend your open source or commercially supported design flow with the use of a SystemC AMS simulation kernel.

Intended audience:

This tutorial targets system engineers and system architects, who would like to use the SystemC AMS extensions for their system-level design and verification tasks. The main use cases for

ESL design and modeling in SystemC AMS are the creation of an executable specification and to facilitate architecture exploration as well as concept development by means of creating virtual prototypes of mixed-signal heterogeneous systems. Both, novel and advanced users, will benefit from this tutorial, since it will present basic as well as advanced modeling concepts.

### Speakers:

**Martin Barnasconi** - NXP Semiconductors

**Christoph Grimm** - TU Kaiserslautern

**Torsten Mähne** - Berner Fachhochschule

**Karsten Einwich** - COSEDA Technologies

## Tutorial 8 - Automatic Firmware Design for Application-Specific Electronic Systems: Opportunities, Challenges and Solutions

Time: 11:30 - 13:00 | Room: Forum 7

### Organizer:

Daniel Große - Univ. of Bremen

In today's and tomorrow's systems balancing conflicting non-functional properties, such as power and performance, is of fundamental importance. This task has been posing a significant pressure on the design of the systems. Conflicting design goals have to be met while at the same time great flexibility resulting from the application scenario is required. Therefore, design solutions based on firmware that allow for the application-specific adaptability of the system are on the rise. This tutorial discusses the opportunities and the challenges of firmware-based design as well as outlines a technical roadmap. Then, it focuses several recently developed approaches for automatic firmware design under consideration of timing and power budgets.

### 8T.1 Overview and Challenges for Firmware Design under Timing and Power Budgets

**Daniel Große** - Univ. of Bremen and DFKI GmbH

### 8T.2 Context-Sensitive Loop Acceleration in Source-Level Timing Simulation

**Joscha Benz** - Univ. of Tübingen

### 8T.3 Validation of Firmware-Based Power Management Using Constrained-Random Techniques

**Vladimir Herdt** - Univ. of Bremen

### 8T.4 Enabling the Generation of Low-Memory-Footprint Firmware for IoT Devices

**Martin Dittrich** - Technische Univ. München

## Tutorial 9 - Next Generation ISO 26262-based Design Reliability Flows

*Time: 14:00 - 15:30 | Room: Forum 4*

### Organizer:

Dave Kelf - *OneSpin Solutions GmbH*

Design and verification flows for safety critical designs, such as automotive ISO 26262 regulated development, continue to be enhanced using new techniques and technologies. These solutions have the potential to improve the reliability of designs for many applications and, as such, all engineers can learn from advancements in this area. Formal-based fault analysis and safety synthesis have emerged as key techniques for ultra reliable design development, and this tutorial will demonstrate a practical, proven flow leveraging these tools.

OneSpin Solutions and Austemper Design Systems have teamed up to produce this detailed tutorial, which demonstrates a complete safety development process, providing valuable information for any engineer adopting these techniques. The tutorial will consist of the following flows:

- Diagnostic coverage will be formally measured on a key IP block
- Safety mechanisms will be synthesized into the block

- The safety mechanism will be verified using various techniques, including formal fault injection.
- Formal diagnostic coverage will be rerun to show improvement
- Fault simulation will be discussed and executed on a larger IP block
- Formal Fault Propagation analysis will also be discussed to accelerate the Fault Sim process.

At all stages of the tutorial, the techniques and methodology steps will be explained, as well as their application on various design styles.

### Speakers:

**Jörg Grosse** - *OneSpin Solutions GmbH*

**Sanjay Pillay** - *Austemper Design*

Thank You to Our Sponsor:



## Tutorial 10 - TLM Modeling and Simulation for NAND Flash and Solid State Drive Systems

*Time: 14:00 - 15:30 | Room: Forum 5*

The demand for Solid State Drives (SSD) is growing both in the Enterprise and Client storage markets. SSD based on NAND Flash technology is a non-volatile storage that can be electrically erased and reprogrammed. NAND Flash technology provides higher durability than Hard Disk Drives (HDD), while providing access times similar to DRAM. However, it has also important limitations with regard to the amount of times that a memory block can be written before it starts wearing out. This effect (among others) implies that NAND Flash storage requires complex management, which is typically implemented on software and running on embedded device micro-controllers. In order to deal with the ever shortening time to market, NAND Flash manufactures are increasingly using virtual prototyping solutions that allow them and their SSD customers to develop controller's firmware as early as possible in the design cycle. Moreover, using virtual prototyping, SSD manufactures can improve the reliability of the firmware by using fault injection techniques based on fast simulation models. All in all, NAND

Flash and SSD manufactures are able to mitigate the risk of achieving their deadlines while dealing with new software architectures, algorithms and interface components. This tutorial describes our experience in modeling high density SSD systems using Transaction Level Modeling (TLM), including a TLM implementation of the standard ONFI protocol and extensive instrumentation that helps debugging and analyzing the FLASH Translation Layer (FTL) software running on those devices. Using our SSD reference Virtualizer Development Kit (VDK), we will demonstrate the main scenarios for software debugging, analysis and fault-injection, running actual FTL embedded software in a typical SSD hardware architecture.

### Speakers:

**Tim Kogel** - *Synopsys, Inc.*

**Victor Reyes** - *Synopsys, Inc.*

Thank You to Our Sponsor:



## Tutorial 11 - Using Cadence and MathWorks Tools Together for Mixed-Signal Design and Verification

Time: 14:00 - 15:30 | Room: Forum 6

### Organizer:

Kawe Fotouhi - *Cadence Design Systems GmbH*

In this technical tutorial we will see details of how Cadence and MathWorks toolsets can be used together to provide an integrated flow for mixed-signal systems, supporting both top-down design and bottom-up verification. This session includes live examples (ADCs, PLLs, and RF PAs), and will be presented by engineers from both companies. Attendees will gain a full appreciation of the technologies available and how they can be applied into their day-to-day work.

The session would benefit design and verification engineers and managers of teams developing mixed-signal semiconductor products, and design methodology teams supporting mixed-signal development.

### Speakers:

**Andrew Beckett** - *Cadence Design Systems Limited*  
**Graham Reith** - *MathWorks, Inc.*

Thank You to Our Sponsor:

**cādence**<sup>®</sup>

## Tutorial 12 - Software Driven Test of FPGA Prototype

Time: 14:00 - 15:30 | Room: Forum 7

Current SoC ASIC designs and recently also more and more FPGA ones are not purely hardware, but contain a significant amount of the software stack and so co-verification of hardware and software is put at high importance among other requirements in the verification plan. Before such a design is taped-out it can be verified and validated at speeds near real operating conditions with peripherals and external devices connected to it using FPGA prototyping boards instead of simulation models. However, preparing a robust FPGA prototype is not a trivial task. It requires strong hardware skills and spending a lot of time in the lab to configure and interconnect all required devices with an FPGA base board. Even more difficult is to create a comprehensive test scenario which contains procedures to configure various peripherals and should incorporate various test sequences capturing real life dataflow cases and dependencies. Programming hundreds of registers in proper sequence and then reacting on events, interrupts, and checking status registers is a complex process to implement. The task which is straightforward during simulation, where full control over design is assured, becomes extremely hard to implement in an FPGA prototype. Facing this challenge, verification engineers often connect a microprocessor or microcontroller daughter card to the main FPGA board. The design under test which is an IP or SoC subsystem will be connected with some kind of CPU anyhow, so this way seems to be natural. Having a CPU connected to the design implemented in an FPGA facilitates creating programmatically reconfigurable

test scenarios and enables test automation. Moreover, the work of software developers can be now reused because the software stack with device drivers can become a part of the initialization procedure in the hardware test.

Recent evolution of the FPGA follows the SoC path known from ASIC designs and now we already have hybrid devices like Xilinx Zynq that combine CPU such as ARM Cortex with reconfigurable FPGA in one die. These devices are flexible enough to be used as embedded and software driven testbench for the design prototyped in FPGA. And limited FPGA capacity of the Zynq-like devices is not an obstacle there because additional high capacity FPGA parts can be added to the board - for example Xilinx UltraScale whose largest member (XC7V440) estimates to 26 Million ASIC gates.

In this tutorial we will explain how to build robust embedded testbench that runs software driven test scenarios. The tutorial will present multiple connectivity options applicable for SoC testing including AMBA AXI Interconnect and demonstrate an example of such with Aldec's Proto-AXI interface and HES-US-440 prototyping board containing both Virtex Ultrascale XC7V440 for the design and Zynq XC7Z100 for the embedded software driven testbench.

### Speakers:

**Radosław Nawrot Nawrot** - *Aldec Inc.*  
**Krzysztof Szczur** - *Aldec Inc.*

Thank You to Our Sponsor:

**ALDEC**<sup>®</sup>  
 THE DESIGN VERIFICATION COMPANY

## Tutorial 13 - Making Cars Safer - One Chip at a Time

*Time: 16:00 - 17:30 | Room: Forum 4*

Autonomous driving is real. Coming out of the realm of research, autonomous vehicles are now on roads around you. Safety of these vehicles is an important consideration in their design. How do you make sure that the vehicle is safe enough

for you to put your loved ones in it? This presentation will explore some challenges in making autonomous vehicles safer and to overcome these challenges.

Thank You to Our Sponsor: **cādence**<sup>®</sup>

## Tutorial 14 - Leveraging Virtual Prototypes from Concept to Silicon: An Exploration of Best Practices

*Time: 16:00 - 17:30 | Room: Forum 5*

The challenges of verifying software and hardware in modern SoCs are many and varied. Verification is required at all stages, from the early conceptual phases of IP design and IP selection through system design to software bring up and optimisation. There is no one solution or set of tools that provides all the answers. The requirements at different stages of the design cycle can be radically different. One commonality in all the solutions is the availability of a consistent portfolio of models that support each stage of the process and address the varying requirements.

This tutorial will overview the approach to modelling that we have taken at Arm to meet these requirements. We will explain the types of models that Arm delivers, how these models are developed and how they are deployed at all stages of the design process.

The tutorial is intended to give a high-level overview into the many aspects of model usage and the benefits can be gained. We will include real-world examples of the application of the techniques described based on both our internal experiences. We will also show how we partner with members of the Arm ecosystem to provide a complete solution for the end users.

**Speaker:**

**Robert Kaye** - ARM, Inc.

Thank You to Our Sponsor:

**arm**



## Tutorial 15 - Testbench Automation : How to Create a Complex Testbench in a Couple of Hours

*Time: 16:00 - 17:30 | Room: Forum 6*

In 2014, the semiconductor industry passed an important milestone. For the first time, the average engineering team had more verification engineers than designers. This means that any improvement in the efficiency of verifications teams has a significant impact on overall project costs and time to market.

In the past two decades, the industry has converged on two complementary strategies to verify increasingly complex SoCs : the reuse of testbenches from subsystem level to SoC level, and the use of advanced verification techniques such constrained random, assertions, and verification management. The key technology that enables these two strategies is the UVM.

Despite its success and proliferation, experience shows us that there are two main problems with this approach. The first is that there is a significant learning curve associated with the adoption of UVM, and the second is that even for UVM experts, creating the necessary infrastructure, getting it up and running, and achieving coverage closure is a time consuming and error prone process.

This tutorial introduces three new technologies which significantly reduce the time to create a reusable testbench infrastructure. These three technologies are integrated into a single comprehensive flow that significantly improves the efficiency of the whole testbench creation process.

In this tutorial, you will learn how to create a complex testbench in a couple of hours. In particular, you will learn:

- How to use UVM-F code generation to rapidly build reusable testbench infrastructure for simulation and emulation
- How to use a VIP Configurator to shorten the bring up time for industry standard protocols
- How Portable Stimulus shortens the time to create efficient, systematic scenario-level stimulus

You will also hear from industry experts who have successfully used this testbench automation flow on their projects.

This tutorial is intended for verification engineers, architects and managers who are interested in making significant improvements to the overall efficiency of their verification process.

### Speakers:

**Graeme Jessiman** - Mentor, A Siemens Business

**Tom Fitzpatrick** - Mentor, A Siemens Business

Thank You to Our Sponsor:



## Tutorial 16 - Boosting Debug Productivity - Practical Applications of Debug Innovations in a UVM World

*Time: 16:00 - 17:30 | Room: Forum 7*

With the growing complexity of today's SoCs, teams are facing intense time pressures for SoC verification closure, with engineers on the lookout for better verification and debug methodologies. As verification teams migrate to SystemVerilog and UVM class-based testbenches for higher efficiency and increased verification reuse across projects, debug methodology needs to scale accordingly to fully realize the benefits of this migration.

In this technical tutorial, we will focus on practical applications of Verdi debug innovations:

- Root causing a complex testbench bug with UVM-aware Reverse Debug natively integrated with simulation
- Techniques to quickly identify, isolate and debug failures using OneSearch, SmartLog and advanced SystemVerilog testbench debug capabilities
- Faster debug at higher levels of abstraction - from transaction debug for protocols to synchronized hardware software debug for earlier SW bring up

Attendees will take home an arsenal of techniques they can put to immediate use to significantly boost their debug productivity.

### Speaker:

**Joerg Richter** - Synopsys, Inc.

Thank You to Our Sponsor:



# TUESDAY'S AGENDA

07:30 - 08:00	 <b>Attendee Coffee Break</b> <i>Room: Großer Saal Foyer</i>		
08:00 - 09:00	<b>Keynote: Driving Virtual Prototyping of Automotive Electronics</b> <i>Room: Ballsaal</i>		
09:00 - 10:00	<b>Panel: The Best Tools for Driving Security and Automotive Applications</b> <i>Room: Ballsaal</i>		
10:00 - 10:30	 <b>Attendee Coffee Break</b> <i>Room: Großer Saal Foyer</i>		
10:30 - 12:00	<b>Session 1 - Formal Verification and Techniques</b> <i>Room: Forum 4</i>	<b>Session 2 - Functional Coverage and IP-XACT</b> <i>Room: Forum 5</i>	<b>Session 3 - AMS Verification, Power Verification, Debugging</b> <i>Room: Forum 6</i>
10:00 - 18:30	<b>DVCon Europe Expo</b> <i>Room: Großer Saal</i>		
12:00 - 13:00	<b>Luncheon</b> <i>Room: Großer Saal Foyer</i>		
13:00 - 14:30	<b>Session 4 - Firmware Verification, Software Design Techniques in Verification, High Level Synthesis</b> <i>Room: Forum 4</i>	<b>Session 5 - System Level Design - SystemC</b> <i>Room: Forum 5</i>	<b>Session 6 - UVM</b> <i>Room: Forum 6</i>
14:30 - 15:00	 <b>Attendee Coffee Break</b> <i>Room: Großer Saal Foyer</i>		
15:00 - 16:30	<b>Session 7 - Functional Safety</b> <i>Room: Forum 4</i>	<b>Session 8 - Architecture Exploration, VP, Specification Automation</b> <i>Room: Forum 5</i>	<b>Session 9 - 5G Special Interest Session</b> <i>Room: Forum 6</i>
16:30 - 17:30	<b>Panel: Intelligent Automation: How to Decide What to and What not to Automate?</b> <i>Room: Ballsaal</i>		
17:30 - 18:30	<b>Closing Session &amp; Best Paper Awards</b> <i>Room: Großer Saal</i>		



## Keynote: Driving Virtual Prototyping of Automotive Electronics

**Berthold Hellenthal**, *Audi*

*Time: 08:00 - 09:00 | Room: Ballsaal*

The regular 36 month to 48 month development cycles of Automotive Electronics is relatively long compared to the development cycle of semiconductor devices. This is due

to different system levels, different value chains and different development processes. To keep up with the development speed of consumer electronics and meet the customer expectations the development cycle of Automotive Electronics needs to be decreased. Enabling virtual prototyping from the device level into automotive applications and systems is an important step to accelerate the time to market.

**Biography:** Berthold Hellenthal runs the Progressive Semiconductor Program (PSCP) at the Audi Competence center for Electronics and Semiconductors, and is responsible for the company's semiconductor strategy. Having joined Audi in 2008 as a member of its senior management team, Mr. Hellenthal specializes in electronic hardware reviews and application analysis as well as semiconductor programs. Mr. Hellenthal holds a Dipl.-Ing from RWTH Aachen University in Germany.



## Panel: The Best Tools for Driving Safety and Security in Automotive Applications

Time: 09:00 - 10:00 | Room: Ballsaal

### Moderator:

Paul Dempsey - *Tech Design Forum*

The reliability of safety-critical chips for automotive applications is a well-known imperative for high-end vehicles, making automotive applications the driver of reliable, repeatable and verifiable functional safety.

Safety-critical designs must be free from systematic errors. Development strategies must ensure development design flaws are handled with rigorous design verification, based on certified design methodologies with intricate requirements tracking. That's why attention is drawn more than ever to the verification flow and strategic verification planning.

Similarly, recent vehicle hacks and system patches have highlighted the need for security to be seen as a safety-critical issue.

Automotive device verification therefore represents the state-of-the-art in methodologies overall. This means that automotive engineering designers involved in safety-critical development are evaluating a trove of verification tools in search of those that can meet the stringent requirements driven by regulations such as ISO26262. Formal verification and its thorough and exhaustive analysis, fault-simulation, emulation and specialized verification planning tools are all under consideration. One example is the verification of fault handling mechanisms, using fault injection by leveraging either traditional fault simulation or more modern formal verification. There are many more.

Meanwhile, protecting against vulnerabilities that allow the operation of a chip to be maliciously subverted has become key, and is likely to become part of a future version of ISO 26262.

Special tools and techniques are required to ensure secure device operation.

A panel of knowledgeable verification experts from each discipline, along with users of such tools, will draw from their experiences to discuss and debate which tools are best for driving security and safety in automotive applications. They will be challenged by Moderator Paul Dempsey of Tech Design Forum and each other to defend their positions and will be expected to offer a clear, concise rationale for the use of a particular tool. Panelists will be asked as well to describe the ideal strategic verification plan for these types of application. Audience participation will be encouraged. The discussion will conclude with a look toward other technology sectors that will soon add reliability to their verification planning strategy.

This will be a lively, thought-provoking discussion covering the range of verification challenges for security and automotive applications related to ISO26262. Attendees can expect to hear the speakers' personal experiences working within the standard's envelope. At the conclusion, the audience will have a clear picture of the serious verification challenges facing this sector and how the rigorous verification planning it requires could soon be required elsewhere.

### Panelists:

**Jörg Koch** - *Renesas Electronics Europe GmbH*

**Jörg Grosse** - *OneSpin Solutions GmbH*

**Sanjay Pillay** - *Austemper Design*

**Holger Busch** - *Infineon Technologies*

**Gabriele Pulini** - *Mentor, A Siemens Business*



## Session 1 - Formal Verification and Techniques

Time: 10:30 - 12:00 | Room: Forum 4

- Chair:**  
Clemens Roettgermann - *NXP Semiconductors*
- 1.1 A Mutually-Exclusive Deployment of Formal and Simulation Techniques Using Proof-Core Analysis**  
**Keerthikumara Devarajgowda**, Jeroen Vliegen - *Infineon Technologies AG*  
Goran Petrovity, Kawe Fotouhi - *Cadence Design Systems, Inc.*
- 1.2 Use of CDC-Jitter-Modeling in Clock-Domain-Crossing-Circuits in RTL Design Phase**  
**Jan Hayek**, Jochen Neidhardt, Robert Richter - *Bosch Sensortec GmbH*
- 1.3 Automatic Testbench Build to Reduce Cycle Time and Foster Reuse**  
**Joachim Geishauser**, Alexander Schiling - *NXP Semiconductors*

## Session 2 - Functional Coverage and IP-XACT

Time: 10:30 - 12:00 | Room: Forum 5

- Chair:**  
Cyril Spasevski - *Onomia*
- 2.1 Accelerating Functional Verification Coverage Data Manipulation Using Map Reduce**  
**Eman M. El Mandouh** - *Mentor, A Siemens Business*  
Ahmed Gamal, Ahmed Khaled, Amr G. Wassal - *Cairo Univ.*,  
Taha Ibrahim - *Cairo Univ. & Mentor, A Siemens Business*,  
Elsayed Hemayed - *Cairo Univ. & IEEE*
- 2.2 Static Checking for Correctness of Functional Coverage Models**  
**Wael Mahmoud** - *Mentor, A Siemens Business*
- 2.3 SimpleLink™ MCU Platform: IPXACT to UVM Register Model - Standardizing IP and SoC Register Verification**  
**Jasminka Pasagic**, Frank Donner - *Texas Instruments, Inc.*

## Session 3 - AMS Verification, Power Verification, Debugging

Time: 10:30 - 12:00 | Room: Forum 6

- Chair:**  
Karsten Einwich - *COSEDA Technologies*
- 3.1 UPF: How to Avoid Traps in a Hierarchical Implementation Low Power Flow?**  
**Frederic Saint-Preux** - *STMicroelectronics*
- 3.2 Between the Dialog and the Algorithm or Innovative Technological Narratives Leveraging the Idea of Authenticity in a Human Being**  
**Hagai Arbel**, Anna M. Ravitzki, Uri Feigin - *VTool Ltd.*
- 3.3 Verification IP for Complex Analog and Mixed-Signal Behavior**  
**Thilo Vörtler**, Karsten Einwich - *COSEDA Technologies*

## Session 4 - Firmware Verification, Software Design Techniques in Verification, High Level Synthesis

Time: 13:00 - 14:30 | Room: Forum 4

- Chair:**  
Raik Brinkmann - *OneSpin Solutions GmbH*
- 4.1 Automatic Firmware Verification for Automotive Applications**  
**Torsten Andre**, Daniel Valtiner - *Infineon Technologies AG*
- 4.2 Modelling Finite-State Machines in the Verification Environment Using Software Design Patterns**  
**Darko M. Tomusilovic**, Mihajlo Z. Minovic - *Veriest Vtool*
- 4.3 UVM Made Language Agnostic - Introducing UVM for SystemC**  
**Akhila M** - *Intel Technology India Pvt. Ltd*

## Session 5 - System Level Design - SystemC

Time: 13:00 - 14:30 | Room: Forum 5

**Chair:**

Mark Burton - *GreenSocs Ltd*

**5.1 Building Code Generators for Reuse - Demonstrated by a SystemC Generator**

**Ulrich Nageldinger**, Saad Siddiqui - *Intel Corp.*

**5.2 Mechanical Mounting Variation Effects on Magnetic Speed Sensor Applications - Combining Finite Element Methods and SystemC Simulations to Study the Effects of Mechanical Tilts and Offset on Magnetic Speed Sensor Applications**

**Simone Fontanesi** - *Infineon Technologies Austria AG*

Se Hwan Kim - *Infineon Technologies Korea Co. Ltd.*

Gernot Binder, Andrea Monterastelli - *Infineon Technologies Austria AG*

**5.3 UVM-Multi-Language Hands-On**

**Thorsten Dworzak** - *Verilab, Inc.*

Angel Hidalgo - *Infineon Technologies AG*

## Session 6 - UVM

Time: 13:00 - 14:30 | Room: Forum 6

**Chair:**

Stefan Birman - *AMIQ srl*

**6.1 Extending the UVM Register Model Generation and Integration Flow to Support User-Defined Scenarios and Register Mask Values**

**Shuang Han**, Kees van Kaam, Martin Barnasconi - *NXP Semiconductors*

**6.2 Flexible Indirect Registers with UVM**

**Uwe Simm** - *Cadence Design Systems, Inc.*

**6.3 Adopting UVM for Safety Verification Requirements**

Srinivasan Venkataramanan - *VerifWorks Pvt. Ltd.*

Hemakiran Kolli - *CVC Pvt., Ltd.*

Gurubasppa Kinagi - *VerifWorks Pvt. Ltd.*

**Satinder Paul Singh** - *Cogknit Semantics Pvt Ltd.*

## Session 7 - Functional Safety

Time: 15:00 - 16:30 | Room: Forum 4

**Chair:**

Akshaya Narayanan - *Infineon Technologies*

**7.1 Formal Fault Propagation Analysis that Scales to Modern Automotive SoCs**

**Sergio Marchese**, Jörg Grosse - *OneSpin Solutions GmbH*

**7.2 An Efficient Requirements-Driven and Scenario-Driven Verification Flow**

**Heino van Orsouw**, Walter Tibboel, Shuang Han - *NXP Semiconductors*

**7.3 Using an Enhanced Verification Methodology for Back-to-Back RTL/TLM Simulation**

**Frank Poppen**, Ralph Görden - *OFFIS - Institute for Information Technology*

Kai Schulz, Andreas Mauderer, Jan-Hendrik Oetjens - *Robert Bosch GmbH*

Joachim Gerlach - *Albstadt-Sigmaringen University*

## Session 8 - Architecture Exploration, VP, Specification Automation

Time: 15:00 - 16:30 | Room: Forum 5

- Chair:**  
Philipp Hartmann - Intel Corp.
- 8.1 Specification by Example for Hardware Design and Verification**  
Jussi Mäkelä - Verranto AS
- 8.2 State-Space "Switching" Model of DC-DC Converters in SystemVerilog.**  
Elvis Shera - Dialog Semiconductor
- 8.3 Heterogenous Virtual Prototyping for IoT Applications**  
Karsten Einwich - COSEDA Technologies  
Mark Burton - GreenSocs Ltd  
Paul Ehrlich - COSEDA Technologies  
Luc Michel - GreenSocs Ltd

## Session 9 - 5G Special Interest Session

Time: 15:00 - 16:30 | Room: Forum 6

- Chair:**  
Oliver Bell - Intel Corp.
- Speakers:**  
Sabine Roessel - Intel Corp.  
Werner Mohr - Nokia  
Meik Kottkamp - Rohde & Schwarz GmbH & Co KG
- The mobile industry is eagerly working towards 5G, the next generation of cellular communication. 5G will be a game changer, facilitating new services, e.g. for autonomous driving and Industrial Internet-of-Things. To meet 5G's promise will require not just new wireless frequency bands and radio tech but also a much smarter, data-oriented network, pushing the limits towards ultra-high bandwidth and ultra-low latency solutions.
- This special interest session with industry experts from Intel, Nokia and Rohde & Schwarz will provide insights on the path to a 5G Internet-of-Things, highlight the Spectrum opportunities and challenges, and offer also a Test & Measurement perspective.

## Panel: Intelligent Automation: How to Decide What to and What not to Automate?

Time: 16:30 - 17:30 | Room: Ballsaal

- Moderator:**  
Krishnapriya Chakiat Ramamoorthy - Infineon Technologies
- We are in the era of automation explosion, and the semiconductor industry is at the forefront. While certain automation has given increased productivity and efficiency, could there be kinds of automation that has resulted in drop in productivity and team morale? Are there certain areas in the semiconductor industry, especially in the front end development where judicious care is required on what we automate and what we do not?
- The event aims to bring together experienced personnel in various phases of an IC development cycle, who have been involved in decision making roles to discuss and decide what aspects do we need to consider when we are faced with a decision to automate a process. Is every automation good? What are the trade offs and the risks involved. Are there certain flows or processes you would never automate, and why. Drawn from personal experiences with automation, the event will discuss the what to and what not to automate and equip the participants with the argumentation for every decision regarding automation they would face in future.
- Panelists:**  
Ashish Darbari - OneSpin Solutions GmbH  
Joachim Geishauser - NXP Semiconductors  
Gernot Koch - TDK-Micronas GmbH  
Yuanfen Zheng - Infineon Technologies

## Closing Session - Best Paper Awards

Time: 17:30 - 18:30 | Room: Großer Saal

# THANK YOU TO OUR SPONSORS

## Gold Sponsors



## Silver Sponsors



## ATTENDEE BREAKS



## BEST PAPER AWARD



## RECEPTION CO-SPONSOR



## CONFERENCE NOTEPAD



## CONFERENCE PEN



## NAME BADGE/ LANYARD



## REGISTRATION



## MEDIA SPONSORS



# DVCON EXPO

## DVCON EUROPE 2017 EXPO

Join us in the Exhibit Hall for the DVCon Europe 2017 Expo!

### Exhibit Hours:

Monday, October 16 ----- 10:00 - 19:00

Tuesday, October 17----- 10:00 - 18:30

---

## DVCON EUROPE 2017 EXHIBITORS\*

Aldec, Inc. ....	404	ELECTRA IC.....	302
AMIQ, EDA .....	502	HDL Design House .....	503
ANKASYS .....	505	Magillem Design Services .....	303
ARM Ltd. ....	407	MathWorks.....	203
Avery Design Systems, Inc.....	403	Mentor, A Siemens Business.....	304
Blue Pearl Software.....	405	OneSpin Solutions.....	402
Cadence Design Systems.....	103	Real Intent, Inc.....	202
ChipGlobe GmbH.....	305	Silvaco Europe Ltd. ....	504
CircuitSutra Technologies Pvt Ltd.....	102	Synopsys.....	401
COSEDA Technologies GmbH .....	101	SyoSil ApS.....	204
Doulos.....	406		

## ATTENDEE BREAKS

Monday, October 16

- 08:00 - 08:30
- 11:00 - 11:30
- 15:30 - 16:00

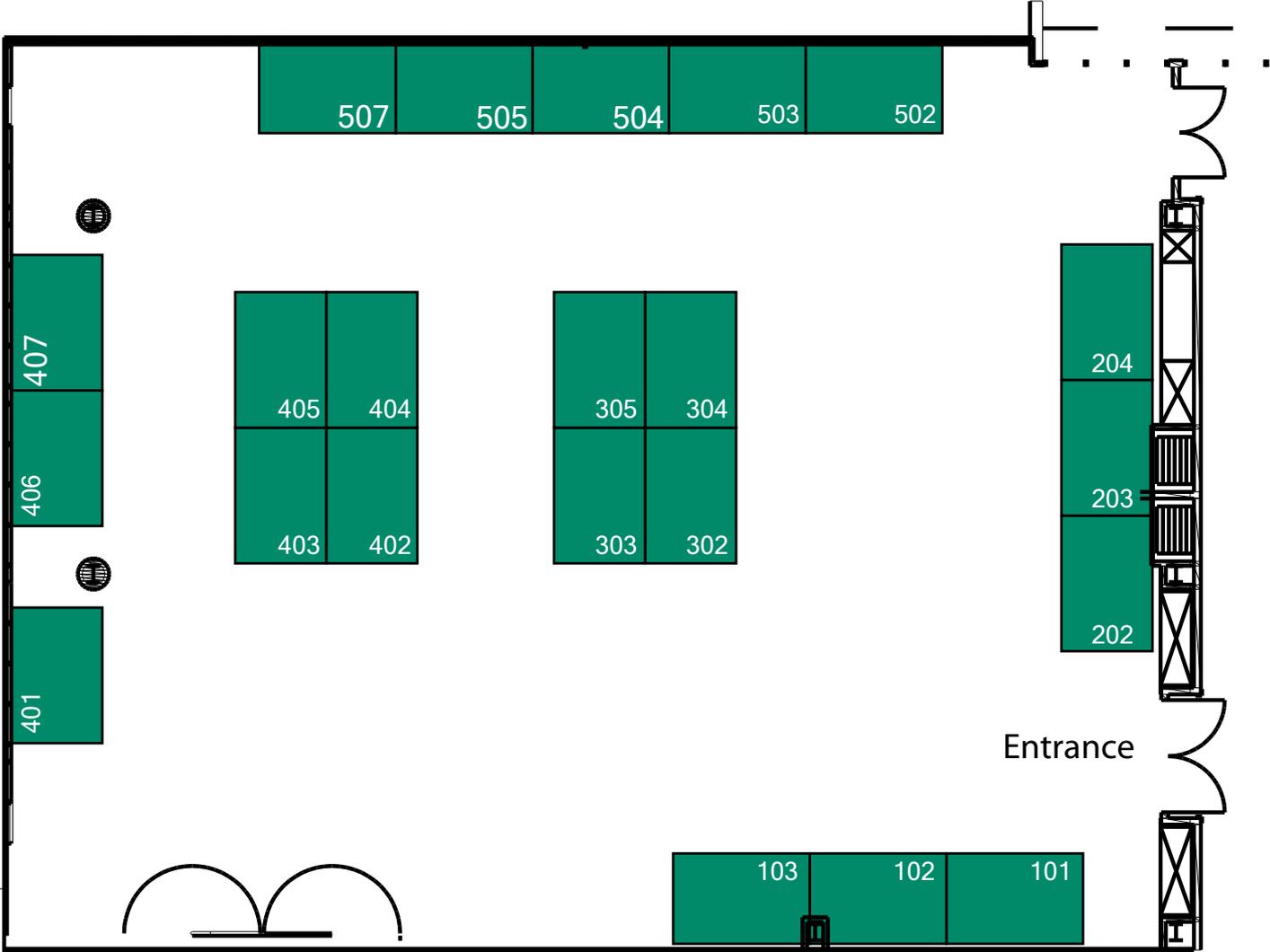


Thank You to Our Sponsor:

Tuesday, October 17

- 07:30 - 08:30
- 10:00 - 10:30
- 14:30 - 15:00

## EXHIBITOR FLOORPLAN



## EXHIBITOR DETAILS



**Aldec, Inc.**  
Booth: 404 | [www.aldec.com](http://www.aldec.com)

Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design and Mixed-Language Simulation (VHDL, Verilog, SystemVerilog/UVM), FPGA-based Hardware-Assisted Verification, SoC and ASIC Prototyping, Emulation, Design Rule Checking, Clock Domain Crossing, VIP Transactors, Requirements Lifecycle Management, Embedded Development Kits, High-Performance Computing/Acceleration, DO-254 Functional Verification and Military/Aerospace. [www.aldec.com](http://www.aldec.com)



**AMIQ EDA**  
Booth: 502 | [www.amiq.com](http://www.amiq.com)

AMIQ EDA provides software tools that enable design and verification engineers, increase the speed and quality of new code development, simplify legacy code maintenance, accelerate language and methodology learning, and improve source code reliability. The company is recognized for its high quality solutions - DVT Eclipse IDE, DVT Debugger Add-On, Verissimo Linter and Specador Documentation Generator - and customer service responsiveness. Websites: [www.amiq.com](http://www.amiq.com); [www.dvteclipse.com](http://www.dvteclipse.com)



**ANKASYS**  
Booth: 505 | [www.ankasys.com](http://www.ankasys.com)

ANKASYS is a microelectronic design and verification company providing advanced design and verification services to its customers from specification to final ASIC GDS or FPGA based embedded systems. The two co-founders bring more than two decades of ASIC/FPGA design and verification experience. The company provides design and verification trainings targeting mainly FPGA-based design, Verilog/SystemVerilog language and the application of the OVM/UVM methodology.



**ARM, Ltd.**  
Booth: 407 | [www.arm.com/](http://www.arm.com/)

Arm technology is at the heart of a computing and connectivity revolution that is transforming the way people live and businesses operate. Our advanced, energy-efficient processor designs are enabling the intelligence in 100 billion silicon chips and securely powering products from the sensor to the smartphone to the supercomputer. With more than 1,000 technology partners including the world's largest business and consumer brands, we are driving Arm innovation into all areas compute is happening inside the chip, the network and the cloud.



**Avery Design Systems, Inc.**  
Booth: 403 | [www.avery-design.com](http://www.avery-design.com)

A leader in Verification IP providing robust models, compliance testsuites, and services for PCI Express, USB/xHCI, UFS/UFSHCI, NVMe/f, SATA Express, SATA, UniPro, Soundwire, Sensewire, CSI/DSI, HDMI, DP, eMMC, SDIO, DDR4/LPDDR4, HBM, HMC, ONFI/Toggle, CAN FD, LIN, FlexRay, and ACE/AXI3/AXI4/AHB. A leader in verification tools. SimXACT automatically eliminates X bugs in RTL and gate-level simulation. ResetOPT minimizes reset/retention design overhead.



**Blue Pearl Software**  
Booth: 405 | [www.bluepearlsoftware.com](http://www.bluepearlsoftware.com)

Blue Pearl Software, Inc., an industry leading provider of design automation software for ASIC, FPGA and IP RTL verification, offers Linting, debug, and CDC solutions proven to improve quality of results, accelerate RTL error find/fix rates while ensuring uniform coding styles. Blue Pearl provides out-of-the-box consistent results, easy setup, SDC generation, management dashboard views and runs on Linux and Windows.

**cadence® Cadence Design Systems, Inc.**  
Booth: 103 | [www.cadence.com](http://www.cadence.com)

Cadence software, hardware and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work and play. The company's System Design Enablement strategy helps customers develop differentiated products-from chips to boards to systems. Learn more at [cadence.com](http://cadence.com).



**ChipGlobe GmbH**  
Booth: 305 | [www.chipglobe.com](http://www.chipglobe.com)

ChipGlobe GmbH Headquarters and Design Center is located in Munich/Germany with a subsidiary in Singapore and an ODC Design Center in Belgrade/Serbia. We are more than 60 senior experts focusing on RTL2GDS2 and functional verification services and solutions. Quality made in Germany working in a global setup! With PAECA we ensure planning security for you.



**CircuitSutra Technologies Pvt. Ltd.**  
Booth: 102 | [www.circuitsutra.com](http://www.circuitsutra.com)

Circuitsutra is an Electronics System Level (ESL) design IP & Services company, headquartered in India, having development centres in Noida & Bangalore, and serves the customers worldwide. It enables customers to adopt advanced methodologies based on C, C++, SystemC, TLM, IP-XACT, UVM-SystemC, SystemC-AMS. Its core competencies include virtual prototype (development, verification, and deployment), Architecture & Performance modelling, co-simulation, co-emulation, HLS, SoC & System verification.



**COSEDA Technologies GmbH**  
Booth: 101 | [www.coseda-tech.com](http://www.coseda-tech.com)

COSEDA Technologies provides software solutions in the field of system level design for complex electronic hard- & software products based on SystemC and SystemC AMS. We make latest modelling and simulation technologies available for our customers to enable them to master new concepts cost-effectively for innovative, complex and safety-critical products.



**Doulos**  
Booth: 406 | [www.doulos.com](http://www.doulos.com)

Doulos has set the industry standard for high quality training and KnowHow for 25 years in design and verification languages and methodologies for system, hardware, and embedded software designers. The essential choice for 3000+ companies across 60+ countries, Doulos provides scheduled classes across North America and Europe, and delivers on-site and live online training worldwide. Find out more: [www.doulos.com](http://www.doulos.com)

## EXHIBITOR DETAILS



### ELECTRA IC

Booth: 302 | [www.electraic.com](http://www.electraic.com)

ElectraIC provides D&V services especially for Advanced Verification for Safety Critical Digital Hardware Development. ElectraIC can work with you in your DO-254 projects, support you as an independent verification team for your DAL-A/B/C product verifications or help you deploying methods, tools and templates required in a DO-254 certification process like configuration management, requirements traceability, verification procedures and records, etc.



### OneSpin Solutions

Booth: 402 | [www.onespin.com](http://www.onespin.com)

OneSpin Solutions, a leader in formal verification, is creating the industry's most advanced formal platform, encompassing agile design evaluation, coverage-driven ABV, and automated DV apps. The world's leading electronics companies partner with us to pursue design perfection in areas where reliability really counts: safety-critical verification, SystemC/C++ HLS code analysis, and FPGA equivalence checking. OneSpin: Making Electronics Reliable



### HDL Design House

Booth: 503 | [www.hdl-dh.com](http://www.hdl-dh.com)

HDL Design House delivers leading-edge front end digital design/verification services, analog and back end services in numerous areas of SoC/FPGA. The company also develops IP cores and turn-key solutions using state of the art Cadence EDA tools. HDL DH joined the ARM® Approved Design Partner program, through which leading SoC design houses are recognized by ARM as accredited partners in specific technologies.



### Magillem Design Services

Booth: 303 | [www.magillem.com](http://www.magillem.com)

Magillem Design Services provides customers with tools and services that drastically reduce the global cost of complex design, help them preserve their independence from vendors and their investment by relying on a worldwide adopted formats like IP-XACT (IEEE 1685).

Clients are semiconductors manufacturers (ASICs, ASSPs), system integrators and information technology companies engaged in the research, design, development, manufacturing and integration of advanced technology systems and products (using ASICs and FPGA).

Magillem is headquartered in Paris, France with a subsidiary in the USA and sales offices in Asia. The Magillem team has been a contributor to the IP-XACT specification since 2003. Magillem has established partnerships with EDA vendors, alliances with ASICs leaders, universities, and R&D European. For more information, visit [www.magillem.com](http://www.magillem.com)



### MathWorks

Booth: 203 | [www.mathworks.com](http://www.mathworks.com)

MathWorks is the leading developer of mathematical computing software. MATLAB is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink is a graphical environment for simulation and Model-Based Design. Engineers and scientists worldwide rely on these product families to accelerate the pace of discovery, innovation, and development in automotive, aerospace, communications, electronics, and other industries.

### Mentor® Mentor, A Siemens Business

A Siemens Business Booth: 304 | [www.mentor.com](http://www.mentor.com)

Mentor Graphics delivers the most comprehensive Enterprise Verification PlatformT (EVP), which combines Questar for high performance simulation, verification management and coverage closure, low-power verification with UPF, CDC, Formal Verification, accelerated functional coverage, and processor-based hardware verification, Velocet OS3 global emulation technology, and the VisualizerT debug environment, to deliver performance and productivity improvements ranging from 400X to 10,000X.



### Real Intent, Inc.

Booth: 202 | [www.realintent.com](http://www.realintent.com)

Real Intent is the leading provider of EDA software to accelerate Early Functional Verification and Advanced Sign-off of digital designs. It provides comprehensive clock-domain crossing verification, advanced RTL analysis and sign-off solutions to eliminate complex failure modes of SoCs. Our Verix, Meridian, and Ascent product families lead the market in performance, capacity, accuracy and completeness.



### Silvaco Europe Ltd

Booth: 504 | [www.silvaco.com](http://www.silvaco.com)

Silvaco is a leading EDA provider of software tools used for process and device development and for analog/mixed-signal, power IC and memory design. The portfolio also includes tools for power integrity sign off, reduction of extracted netlist, variation analysis and also production-proven intellectual property (IP) cores. Silvaco delivers a full TCAD-to-Signoff flow for vertical markets including: displays, power electronics, optical devices, radiation & soft error reliability, analog and HSIO design, library and memory design, advanced CMOS process and IP development. The company is headquartered in Santa Clara, California, and has a global presence with offices located in North America, Europe, Japan and Asia.

### SYNOPSYS® Synopsys, Inc.

Booth: 401 | [www.synopsys.com](http://www.synopsys.com)

Synopsys is the Silicon to SoftwareT partner for innovative companies developing the electronic products and software applications we rely on every day. Whether you're designing advanced semiconductors or developing software that requires the highest quality and security, Synopsys has the EDA, semiconductor IP and software integrity solutions needed to deliver smarter, more secure products. Learn more at [www.synopsys.com](http://www.synopsys.com).



### SyoSil ApS

Booth: 204 | [www.syosil.com](http://www.syosil.com)

SyoSil is a leader in FPGA/ASIC design and verification solutions, including device firmware and tool development. We advise our clients on how to improve their design and verification methodologies, and deliver turn-key verification flows and Verification IP, based on industry standards such as SystemVerilog/UVM. Our clients include top European and U.S. semiconductor companies.

# DVCON EXPO

## DVCON EUROPE 2017 EXHIBITORS\*



# JOIN US IN THE UNITED STATES

2018  
DESIGN AND VERIFICATION™  
**DVCON**  
CONFERENCE AND EXHIBITION  
**UNITED STATES**

**FEBRUARY 26 - MARCH 1, 2018**

**DoubleTree Hotel, San Jose, CA  
San Jose, CA, U.S.A.  
DVCon.org**

2018  
DESIGN AND VERIFICATION™  
**DVCON**  
CONFERENCE AND EXHIBITION  
**CHINA**

# JOIN US IN CHINA!

**APRIL 18, 2018**

**DoubleTree by Hilton Shanghai-Pudong  
Shanghai, China  
DVCon-China.org**

# Most Comprehensive Automotive Verification Solution

- Speed up functional safety SoC verification for ISO 26262
- Accelerate software development and test from SoCs to ECUs
- Enable collaboration between automotive semiconductor, Tier 1s and OEMs

Visit Synopsys at Booth #401

