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2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

November 11-12, 2015
Holiday Inn City Centre
Munich, Germany

Conference Program

Exhibition Guide

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DVCon Europe Welcomes You Again

Martin Barnasconi
NXP Semiconductors
General Chair
DVCon Europe 2015

After its successful launch last year, I'm pleased to announce that the **Design and Verification Conference & Exhibition Europe** is back in 2015!

With more than 250 attendees in 2014, full tutorial rooms, a good variety of technical presentations, and a nicely crowded exhibition floor, we can conclude that DVCon Europe fulfils a clear need: an industry-oriented conference, focusing on design and verification of electronic systems and integrated circuits.

Also this year, DVCon Europe will bring the engineering community together to share experiences and to present the practical use of Electronic Design Automation (EDA) standards, languages and methodologies for design and verification. The main conference themes this year are: System Level Design & Verification, Advanced Verification & Validation, Design for Functional Safety, IP Reuse and Design Automation, Analog and Mixed-Signal Design & Verification, Lower Power Techniques and RTL Simulation Techniques.

The tutorial day last year was highly valued by the participants, so DVCon Europe 2015 starts again with a rich tutorial program. In total 15 tutorials are given by user-companies, standardization teams, training institutes, consultancy companies, or EDA tool providers.

With the high number of paper submissions, the program committee created a diverse technical program reflecting today's industry practices in design and verification. The technical program on Thursday hosts various paper sessions and a poster session. You are invited to vote on the best paper and poster, which will be announced at the closure of the conference.

New in DVCon Europe 2015 is the special focus on Automotive design and verification, by introducing a dedicated session on functional safety. Furthermore, a plenary panel session has been added to the program to discuss the requirements and needs for functional safety in the Automotive value chain. Also the keynote this year will focus on the Automotive domain, and will give you a glimpse into the future of Automotive.

The exhibition at DVCon Europe has been expanded and we welcome the new exhibitors this year presenting their EDA tools, services and solutions. On Wednesday and Thursday you can interact with these EDA companies, training institutes and service providers. Perhaps they can offer the solution for your design or verification problem!

With these tutorials, technical program and exhibition, DVCon Europe is our contribution to you to learn and grow. The DVCon Europe Steering Committee and the **Accellera Systems Initiative** welcome you at the conference. Enjoy DVCon Europe!

Martin Barnasconi

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

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Conference & Exhibition Highlights

DVCon Europe Opening and Overview:

Wednesday, November 11, 8:30 – 8:45, Großer Saal (Forum 1+2+3)

Thursday, November 12, 8:30 – 8:45, Großer Saal (Forum 1+2+3)

Tutorials:

Wednesday, November 11, 9:00 – 17:00, Forum 1, 2+3, 8 and 10+11.

Panel Session:

Wednesday, November 11, 17:15 – 18:00, Großer Saal (Forum 1+2+3)

DVConnect Reception:

Wednesday, November 11, 18:30 – 19:30, Foyer Großer Saal

Gala Dinner:

Wednesday, November 11, 20:00 – 22:30, Ballsaal

Keynote:

Thursday, November 12, 8:45 – 9:35, Großer Saal (Forum 1+2+3)

Technical Presentations & Poster Session:

Thursday, November 12

Technical presentations: 10:00 – 17:00, Forum 1, 2+3, and 8

Poster session: 12:45 – 13:45, Forum 10+11

Best Paper and Best Poster Award:

Wednesday, November 12, 17:15 – 17:45, Großer Saal (Forum 1+2+3)

Exhibition:

Wednesday, November 11, Foyer Großer Saal, Prime Exhibition Hours:

10:30 – 11:00, 12:30 – 13:30, 15:00 – 15:30, 18:00 – 20:00

Thursday, November 12, Foyer Großer Saal, Prime Exhibition Hours:

11:00 – 11:30, 12:30 – 14:00, 15:30 – 16:00

Registration Information

Registration Sponsored by:

Registration Hours:

Wednesday, November 11: 8:00 – 17:00, Foyer Großer Saal
Thursday, November 12: 8:00 – 12:00, Foyer Großer Saal

Registration Type	Registration Fee
Full Conference (**2 days**) Accellera Member	375€
Full Conference (**2 days**) Non-Member	425€
Tutorial Day (**1 day**, Nov. 11 only) Accellera Member	275€
Tutorial Day (**1 day**, Nov. 11 only) Non-Member	325€

All prices are in Euros, excluding tax (VAT).

Full conference (2 day) registration includes:

- DVCon Europe Conference entry fee (2 days)
- DVCon Europe Exhibition (2 days)
- Access to proceedings via website with tutorials, papers, and presentations
- Gala Dinner on November 11, 20:00 – 22:30
- Lunch on November 11 and 12
- Coffee breaks on November 11 and 12

Tutorial day (1 day) registration includes:

- DVCon Europe Conference entry fee on Wednesday, November 11 only (1 day)
- DVCon Europe Exhibition on Wednesday, November 11 only (1 day)
- Access to tutorial proceedings via website
- Gala Dinner on November 11, 20:00 – 22:30
- Lunch on November 11
- Coffee breaks on November 11

Exhibition only pass:

- DVCon Europe exhibition pass, valid for one day from 2pm to 6pm: 25€
  Note that this pass only gives access to the exhibition and not to the conference itself
- A supplemental ticket for the Reception and Gala Dinner: 75€

Gala Dinner guest registration:

One Gala Dinner ticket is included with your conference registration. You may also purchase an additional Gala Dinner ticket with your registration if you would like to bring a guest: 49€

Hotel Information

DVCon Europe takes place at **Holiday Inn City Centre**. The hotel is located close to downtown Munich, with only a 10 minute walk to visit the city center. The hotel is easy to reach by S-Bahn (Rosenheimer Platz) and 35 minutes by train from Munich Airport (Franz Josef Strauss).

Hotel address:

Holiday Inn Munich City Centre
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How to reach Holiday Inn City Center

From the airport by car: Turn on to Highway A92 then take Highway A9, signed for Munich. Follow the Highway until the exit for Munich East. Continue straight, then turn left onto Ludwigsbruecke and follow Rosenheimer Strasse for 100 meters, then turn right on Hochstrasse where you will see the hotel entrance. Distance to hotel is approximately 35 km. Driving time is approximately 30 minutes.

From the airport by train (S-Bahn): Take the S-Bahn "S8" from Munich Airport towards Munich center. The train station can be found between Terminals 1 and 2. Trains depart every 20 minutes, with a direct connection to "Rosenheimer Platz" station reachable in 35 minutes. Take exit "Rosenheimer Platz" and follow directions to "Gasteig". Take the escalator and follow the Holiday Inn Munich – City Centre signs. You'll pass "Subway", "Aldi" and "Hit" supermarkets on the left, and you'll find the hotel on your left. Please note that there is a lift behind the stairs that ensures you easy access to the lobby and reception.

For the train trip you need a one-way ticket of 4 zones, which currently costs 10.80€. Alternatively, you might consider the Airport-City Day Ticket, which is a day ticket for the entire MVV network, valid from the moment you purchase until 6am the following day.

Estimated price by **Taxi** from Munich Airport: 60€.

Conference Sponsor

Accellera Systems Initiative, the proud sponsor of DVCon Europe, is an independent organization with the mission to provide design and verification standards required by systems, semiconductor, IP and design tool companies to enhance a front-end design automation process. We collaborate with our community of members to deliver the standards that lower the cost of designing commercial EDA, IC and embedded systems solutions. As a result of its partnership with the IEEE, Accellera standards are transferred to the IEEE Standards Association for formalization and ongoing change control.

Accellera Systems Initiative: A New Synergy for Standards

System, software, and semiconductor design are converging to meet the increasing challenges to create complex integrated circuits and systems on chips. This convergence has brought to the forefront the need for a single organization to facilitate the creation of system-level, semiconductor design and verification standards. Accellera addresses the needs of the system and semiconductor designers who must find new and smarter ways to create and produce increasingly complex chips. The organization is creating more comprehensive standards that benefit the global electronic design community.

Membership

Accellera's members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera and for information on how to join us, please visit our website at **www.accellera.org**.

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Note that the username and password are case sensitive.

Please respect the '*one device per user*' policy to allow access for everyone.

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During the attendee breaks you can enjoy a cup of coffee or tea, start networking with your peers, and visit our exhibitors!

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Program-at-a-Glance – Wednesday, Nov. 11

	Track 1 (Forum 1)	Track 2 (Forum 2+3)	Track 3 (Forum 8)	Track 4 (Forum 10+11)
8:30 – 8:45	**Welcome & Overview** (Großer Saal)			
9:00 – 10:30	T1a Advanced UVM Tutorial - Taking Reuse to the Next Level (Part 1)	T2 System-Level Modeling for Today and Tomorrow with SystemC	T3 Applying Design Patterns to Accelerate Development of Reusable, Configurable and Portable UVCs	T4 Methodology of Communication Protocols Development: From Requirements to Implementation
10:30 – 11:00	**Coffee Break & Exhibition** (Foyer Großer Saal)			
11:00 – 12:30	T1b Advanced UVM Tutorial - Taking Reuse to the Next Level (Part 2)	T5 UVM Goes Universal - Introducing UVM in SystemC	T6 Accellera Standards Technical Update	T7 Verifying Functional, Safety and Security Requirements (for Standards Compliance)
12:30 – 13:30	**Lunch & Exhibition** (Foyer Großer Saal)			
13:30 – 15:00	T8 Easier UVM – Learning and Using UVM with a Code Generator **DOULOS**	T9 FPGA Debug Using Configuration Readback **DINI GROUP**	T10 Advanced, High-Throughput Debug from Design to Silicon **MENTOR GRAPHICS**	T11 Golden UPF Tutorial: Preserving Power Intent from RTL to Implementation **SYNOPSYS**
15:00 – 15:30	**Coffee Break & Exhibition** (Foyer Großer Saal)			
15:30 – 17:00	T12 The Functional Verification Roadmap: Where Will We Be in Five Years? **ONESPIN SOLUTIONS**	T13 The How To's of Advanced Mixed-Signal Verification **CADENCE**	T14 UVM Hardware Assisted Acceleration with FPGA Co-emulation **ALDEC**	T15 SystemVerilog Assertions Verification **AMIQ CONSULTING**
17:15 – 18:00	**Panel: Functional Safety in the Automotive Value Chain** (Großer Saal)			
18:00 – 20:00	**Exhibition** (18:00 – 20:00) **DVConnect Reception** (18:30 – 19:30) (Foyer Großer Saal) Birds-of-a-Feather sessions (18:30 – 19:30, Forum 2+8)			**AGNISYS**
20:00 – 22:30	**Gala Dinner** (Ballsaal)			**ACCELLERA + SYNOPSYS**

Tutorial Overview and Panel Session

Special Thanks to our Tutorial Sponsors

Wednesday, November 11

Tutorial T1: Advanced UVM Tutorial - Taking Reuse to the Next Level

Forum 1 **Part A: 9:00 – 10:30, Part B: 11:00 – 12:30**

This tutorial provides intermediate and advanced users of the Universal Verification Methodology (UVM) with comprehensive in-depth material on all aspects of achieving vertical and horizontal verification reuse using UVM. The content is derived from Verilab's extensive experience in solving reuse issues for many different clients, projects and applications using a variety of verification languages and includes pragmatic guidelines as well as real-world examples. It is aimed at engineers with a good understanding of SystemVerilog and practical experience in either OVM or UVM. UVM beginners may also find the content interesting although the details could be somewhat overwhelming, at any rate it should raise awareness and provide some good reference material for the future.

After a very brief introduction to UVM in order set the scene and put the other topics into context, the tutorial takes a detailed look at reuse concerns such as structural architecture, user-focused encapsulation and stimulus layering, automatic adaptation and tuning of stimulus, checks and coverage based on static and non-static configuration fields as well as required roles of the corresponding agents in the enclosing verification environments. The material is grouped into the following topics:

- Vertical & Horizontal Reuse of UVM Environments
- Configuration Object Encapsulation & Appropriate config_db Usage
- Stimulus Structure & Sequence Layering for Reuse
- Adaptive Protocol Checks - Configuration Aware Assertions
- Self-Tuning Functional Coverage - Strategy & Implementation
- Parameterized Classes, Interfaces & Registers

A deeper understanding of how these key reuse requirements are implemented in UVM provides the verification engineer with the expertise necessary to go beyond the beginner level and excel at applying UVM reuse concepts to a wide variety of applications. The focus is very much on pragmatic real-life working solutions, but we go behind the scenes of UVM where required in order to highlight the mechanics and demonstrate how it all fits together.

Presenters:

Jonathan Bromley, *Verilab*, United Kingdom

Jason Sprott, *Verilab*, United Kingdom

Wednesday, November 11

Tutorial T2: System-Level Modeling for Today and Tomorrow with SystemC

Forum 2+3 **9:00 – 10:30**

The ever-increasing complexity of electronic systems is adding pressure to move to an abstraction above RTL. SystemC IEEE 1666-2011 provides the language elements for system-level and transaction level modeling (TLM) and has been widely adopted by the industry to develop Virtual Prototypes (VP) of (embedded) systems for pre- and post-silicon software development, hardware software co-design, architectural analysis etc.

In this tutorial, hands-on users and tool developers share their recent experience and describe advanced methodologies that have helped them achieve significant benefits already today:

A. **Accellera Update on SystemC Standardization**

Philipp A Hartmann, *Intel*; **Martin Barnasconi**, *NXP*; **Stephan Schulz**, *Fraunhofer*

The tutorial will start with an update and overview about recent standardization activities from the different SystemC-related Accellera and IEEE Working Groups, giving a condensed overview about status and plans around SystemC.

B. **Virtual Platform(s) Simulation: an Open-Source, Reusable, Affordable and Structured Approach based on TLM/CCI**

Guillaume Delbergue, *GreenSocs / IMS Bordeaux*; **Mark Burton**, *GreenSocs*

GreenSocs developed a new way to build fast and efficient virtual platform using the power of SystemC/TLM and components from the open source community. This tutorial will introduce QBox (QEMU in a box), a package of shared libraries containing QEMU-based CPU models. It will explain how QBox works, how its interfaces comply with the TLM-2.0 standard and how a QBox object can be used with your existing SystemC simulation components and environment.

C. **What is Needed Beyond SystemC and TLM-2.0 to Address the Bigger System-Levels?**

Jérôme Cornet, *STMicrolectronics*; **Martin Schnieringer**, *Robert Bosch GmbH*

TLM-2.0 is a well-defined abstraction level to model on-chip buses and components that are connected to these buses and interconnects. To enable proliferation of VPs that support as many as possible use cases these off-chip interfaces have to be standardized to enable fast & cheap platform assembly. This tutorial will address the (automotive) use cases and requirements of systems using these off-chip interfaces. Specific scenarios will be presented that are used to assess implementation alternatives of such a standard. Finally, some possible solutions for modeling off-chip buses will be presented.

Wednesday, November 11

Tutorial T3: Applying Design Patterns to Accelerate Development of Reusable, Configurable and Portable UVCs

Forum 8 **9:00 – 10:30**

Verification methodologies such as UVM heavily rely on object orientation to achieve code reuse. But there are other reuse possibilities that cannot be accomplished by only using object-oriented programming. One of the methods to increase reuse significantly which in turn accelerates the process of developing new UVCs is by applying "Design Patterns".

In this tutorial we will define what "design patterns" are and demonstrate how they can be applied in the context of building UVCs. We will use transaction implementation as an example because it's widely used and well understood. With this approach we have seen about 2x-5x gains in productivity and quality.

In this tutorial we will take detailed example of Template and Abstract Factory Design Patterns and apply it to building reusable configurable portable UVCs:

- "Template Design Pattern" applied to a UVM Transaction:
  Transaction is an abstraction used in verification environments for data modelling. Verification methodologies provide a set of pre-defined methods for standard transaction implementation.
- "Abstract Factory Design Pattern" applied to a UVM Transaction:
  A transaction in constrained random verification environment typically used with a set of other related classes. For instance, a BFM processing transaction will need to provide a set of events related to the transaction for synchronization, error configurations to inject errors in transaction and call-backs for transaction. A test bench would be needed to provide the functional coverage for the transaction.

We will also cover other key Design Patterns like Factory Methods, Observer, Singleton, Strategy and Adapter.

Intended audience: Verification Engineers at block, subsystem and SOC level, Verification Environment Architects and Verification Managers.

Presenter:

Paul Kaunds, *EnSilica Ltd*, United Kingdom

Wednesday, November 11

Tutorial T4: Methodology of Communication Protocols Development: From Requirements to Implementation

Forum 10+11 **9:00 – 10:30**

The communication protocol design is a rather complicated process. It consists of multiple steps of development which should result in a physical implementation. Some of these steps are closely related to modeling, which simplifies development, reduces its cost and helps to avoid serious bugs and errors and fix them before the hardware implementation.

The communication protocol design encounters a number of difficulties caused by increasing complexity of projects, increasing requirements to products reliability, power consumption and demand to speed-up the project design phase which is very important especially for avionics and onboard systems.

The tutorial is intended to share with the audience our experience in the communication protocols development. In our tutorial we will cover the following aspects:

1. Introduction to general design flow for protocol development.
2. Main principles and problems of collecting requirements.
3. Directions of communication protocols simulation and investigation including C++, SystemC, SDL, SDL/SystemC and VHDL.

This tutorial will be useful for specialists who work in the field of communication protocol and network equipment development.

We have applied this protocol development methodology in a number of European and Russian projects such as MIPI UniPro, SpaceWire, SpaceWire-RT and STP-ISS projects.

Presenter:

Irina Lavrovskaya

Saint-Petersburg State University of Aerospace Instrumentation, Russia

Wednesday, November 11

Tutorial T5: UVM Goes Universal - Introducing UVM in SystemC

Forum 2+3 **11:00 – 12:30**

UVM is a verification methodology which has gained widespread acceptance in the semiconductor industry. Despite being a universal verification methodology, it is currently limited to the SystemVerilog world, where an open source reference implementation is available for several years now and is supported by many EDA vendors.

Since the donation of a proof-of-concept UVM implementation in SystemC to Accellera in 2014, standardization efforts of UVM for SystemC (named UVM-SystemC) have gained momentum to the point that the release of a public SystemC-based proof-of-concept implementation is expected later this year.

This tutorial will introduce the basic concepts and will give a range of examples on how to apply UVM-SystemC to address the challenges in ESL design and verification. Furthermore, it will discuss the advantages compared to the current SystemVerilog-based UVM implementation.

This tutorial will be presented in three sections:

- In the first introductory section, several key mechanisms of UVM are explained to bring the audience to a common basic knowledge level.
- Verification examples demonstrating the applications of the UVM-SystemC implementation will be presented in the second part of the tutorial. Furthermore, an outlook will be given how verification components can be used for different abstraction levels of the same design-under-test, including an outlook how hardware-in-the-loop systems can be supported.
- The final section will discuss the ongoing development of the proof-of-concept implementation and the language reference manual to show clearly where UVM-SystemC is headed and what has been already achieved in the past activities.

The intended audience includes managers, system and verification engineers and architects with a basic knowledge in SystemC and/or UVM, which are interested to further improve their system-level verification practices.

Presenters:

Stephan Schulz, *Fraunhofer IIS/EAS*, Germany

Thilo Vörtler, *Fraunhofer IIS/EAS*, Germany

Wednesday, November 11

Tutorial T6: Accellera Standards Technical Update

Forum 8 **11:00 – 12:30**

In this tutorial, experts in the Accellera standardization will given a technical update on the recent standardization activities in the various working groups:

Universal Verification Methodology: The UVM library specification standard is now being managed by the P1800.2 IEEE working group. The initial goal of the working group is to achieve a standard that has a well specified API. The Accellera UVM WG will continue to develop a base class version that is aligned to the upcoming UVM IEEE specification. In this tutorial we will provide some insight with respect to the changes above and the development processes. Attendees will be able to provide feedback to the committees, use the information to plan future migrations and interact with industry UVM gurus.

Portable Stimulus: The Accellera Portable Stimulus Working Group (PSWG) is working to define a specification to permit the creation of a single representation of stimulus, verification intent and coverage from which multiple target implementations may be derived that run on a variety of execution platforms including simulation, emulation, FPGA prototyping and post-silicon. This session is intended to provide attendees an opportunity to learn about Portable Stimulus and where the PSWG currently stands in the standard-creation process.

IP-XACT: IP-XACT, defined in IEEE 1685, defines an XML Schema for meta-data documenting of Intellectual Property (IP) and a tool interface (TGI) to provide access to the meta-data. It is used in the integration and verification of electronic systems. In this talk, the most important updates of the standard provided in the IEEE 1685-2014 version are presented and their relevance to enhance IP integration and flow automation. The updates include view-dependent port maps in bus interfaces, conditionality of meta-data and extensions of TGI to support full meta-data creation, inspection, manipulation, and deletion.

SystemC: SystemC, ratified as IEEE Std. 1666™-2011, is the language of choice for system-level design and verification spanning hardware and software. This talk presents the ongoing work on the evolution of SystemC-related standards, to address the needs for today's and tomorrow's systems both in terms of increased modeling productivity and for better model-model and model-tool interoperability.

Presenters:

UVM – **Uwe Simm**, *Cadence Design Systems*

Portable Stimulus – **Sharon Rosenberg**, *Cadence Design Systems*

IP-XACT – **Erwin de Kock**, *NXP Semiconductors*

SystemC – **Philipp A. Hartmann**, *Intel*

Wednesday, November 11

Tutorial T7: Verifying Functional, Safety and Security Requirements (for Standards Compliance)

Forum 10+11 **11:00 – 12:30**

Markets such as automotive, avionics, nuclear, medical, rail, industrial, etc. require compliance to stringent development standards to ensure the devices are safe. As the devices become increasingly connected then security also becomes increasingly important. The standards require developers to minimize errors in such devices and to also ensure that the device can recover safely from any errors.

Errors in such devices can come from two main sources: systematic design errors introduced during the development process; random physical errors occurring in the field. Both types of error need to be addressed – the former is addressed through mandating stringent development practices and the latter through error detection and correction mechanisms.

The types of development practices mandated vary according to the safety integrity level assessed for the device but all safety levels mandate that requirements are properly captured and traced through development to verification. In this tutorial we consider how functional, safety and security requirements can be traced to verification tasks and then subsequently signed off. The tutorial will cover the following topics in detail

- Defining safety requirements related to ECC (Error Code Correction) mechanisms through identifying assertions and proving them using formal property checking.
- Identifying security requirements (such as privileged accesses to memory), translating them into assertions that can be checked in simulation.
- Demonstrating how all requirements can be traced through feature analysis to a verification plan and how that can be traced through to verification execution and thus resulting in a proof of implementation for conformance to development standards.

Presenters:

Mike Bartley, *Test and Verification Solutions*, United Kingdom

Dave Kelf, *OneSpin Solutions*, USA

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Tutorial T8: Easier UVM – Learning and Using UVM with a Code Generator

Forum 1 **13:30 – 15:00**

This tutorial gives a short introduction to UVM, the Universal Verification Methodology for SystemVerilog, by taking full advantage of the Easier UVM code generator. By using a code generator to generate the boilerplate code, we are able to focus attention where it matters - on the verification methodology and the concepts – without getting distracted by the coding detail.

Easier UVM consists of a set of coding guidelines and a code generator that creates UVM code compliant to those guidelines. Easier UVM is used in this tutorial because it is an effective way of learning and adopting UVM, and furthermore the Easier UVM guidelines and code generator are freely available for use after the tutorial (under an Apache 2.0 license). Easier UVM was created to help individuals and project teams learn and then become productive with UVM as quickly as possible.

This tutorial focuses on UVM itself, using the perspective brought by a code generator to allow us to distinguish between code that can be automatically generated and code specific to the verification task, where the verification engineer is able to add value to the boilerplate code. Topics presented:

- Introduction, background, and motivation for UVM
- An overview of the main technical highlights of UVM
- A tutorial introduction to the basic features of UVM: SystemVerilog interfaces, UVM agents, sequencers, drivers, monitors, subscribers, TLM connections, reporting, configuration objects, the factory, sequences, virtual sequences, envs, and tests
- Understanding which parts of a UVM environment can be automatically generated and which parts need to be user-defined
- How to run the Easier UVM code generator to create your own examples

This tutorial is suitable for total beginners and for people with some experience of UVM. To get the most from this tutorial, attendees should have at least some familiarity with SystemVerilog.

Presenter:

John Aynsley, *Doulos*, United Kingdom

Wednesday, November 11

Tutorial Sponsored By:

Tutorial T9:
FPGA Debug Using Configuration Readback

Forum 2+3 **13:30 – 15:00**

FPGAs are now one of the most common devices used to implement complex electronics systems. With the largest devices now approaching 30M equivalent ASIC gates, FPGAs have been very successful at replacing ASICs and ASSPs that previously made up the bulk of complex system designs.

Increased size and complexity does not come free. Once an FPGA has been designed it needs to be debugged. Painstaking simulation can eliminate many errors, but even the most careful development process will miss subtle definitional errors, unexpected sub-system interaction issues, or even board level timing/noise problems that require significant detective work to find and fix. It might not be even be worthwhile to exhaustively simulate an FPGA-based design since the downside of initial bugs is not nearly as catastrophic as with an ASIC.

Several hardware oriented techniques have been implemented by FPGA manufacturers and third parties to simplify hardware-based debugging. A careful understanding of each of these key techniques, including the various advantages and disadvantages, is useful when considering which technique or combination of techniques is suitable for a particular design.

This tutorial will describe the most common FPGA hardware debugging approaches, describe their strengths and weaknesses, and will illustrate how readback can be used to augment, but not replace, existing debug approaches.

Presenter:

Mike Dini, *Dini Group*, USA

Wednesday, November 11

Tutorial T10: Advanced, High-Throughput Debug from Design to Silicon

Tutorial Sponsored By:

Mentor Graphics®

Forum 8 **13:30 – 15:00**

Ongoing improvements in verification compute engine performance have created a new verification challenge: dealing with an avalanche of data for D&V engineers to process. While methodologies like coverage-driven test ranking and sophisticated checkers can help focus the verification results on the most high-value data points, a real live person must still sift through the all output and navigate the failure analysis – bug identification – fix – validate cycle. In a nutshell, the debug challenge is big and is only growing. Indeed, based on semi-annual customer surveys debug is now exceeding 36% of an engineer's time, which is more than any other single verification task. Clearly, improving debug productivity from block to system pre-silicon verification, emulation, as well as post-silicon validation is critical to stay on schedule and simultaneously meet quality goals.

In this tutorial we show how you can significantly improve debug productivity in the context of the following recommendations:

- Leverage new debug technologies to expedite causality discovery
- Apply low-power debug techniques in every D&V phase
- Employ advanced tools for multi-core embedded SW/HW debug and performance tuning
- Extend these Debug techniques to Post-Silicon validation

The tutorial will include live demonstration to illustrate the effectiveness of these recommendations in real world projects.

Presenters:

Gordon Allan, *Mentor Graphics*, USA

Mike Horn, *Mentor Graphics*, USA

Wednesday, November 11

Tutorial T11: Golden UPF Tutorial: Preserving Power Intent from RTL to Implementation

Tutorial Sponsored By:

SYNOPSYS®

Forum 10+11 **13:30 – 15:00**

Power-aware design differs from conventional design in both well-understood and subtle ways. While higher level specifications hold a promising future, RTL is the commonly used representation of design intent today. It guides the implementation process and relies on functional verification to assure the intent carries through to silicon. In power-aware design, the power format file, like IEEE 1801 (UPF), is the specification (and not the RTL by itself). While all the tools in the end-to-end flow can read the power intent, the power intent itself goes through alterations wherein the synthesis and implementation tools write out their own UPF making it difficult for you to ascertain whether the original power intent is preserved or not.

The answer for preserving the power intent is Golden UPF. The original RTL UPF is structured and more concise and easier to read. It has user comments and conditional sections not evaluated by the implementation tools. It also has wildcards and find/query operations. This information is lost when the RTL UPF goes through synthesis and implementation wherein it is called UPF' (post-synthesis) and UPF'' (post-implementation).

Users are upset with the updated UPF file since it looks very different than Golden UPF file. They are not sure if the original power intent of the Golden UPF file is intact in the updated UPF file. Moreover, it is difficult to guarantee whether the functionality of the updated UPF is the same as that of the RTL UPF. In today's context, the pace of design and the cost of silicon failure do not permit the electronics industry a similar "baking" time for power-aware design.

This tutorial presents how the Golden UPF flow can be applied across the different verification and implementation tools to minimize the risk of subtle bugs escaping into silicon.

Presenters:

Himanshu Bhatt, *Synopsys*, USA

James Gillespie, *Synopsys*, USA

Wednesday, November 11

Tutorial/Panel T12: The Functional Verification Roadmap: Where Will We Be in Five Years?

Tutorial Sponsored By:

Forum 1 **15:30 – 17:00**

Engineers are confronted with a confusing array of functional verification options and emerging standards. This tutorial panel will consider and predict various areas of advancements required in functional verification for the next five years. Issues to be discussed include the creation of an effective flow with tools from many sources, the collection and leverage of metrics to measure progress, the impact of safety-critical device verification, and increased software content. Experts in these different areas will consider questions, such as the effectiveness of existing standards, including UVM, SystemC and UCIS, and the likely evolutionary paths of verification flows.

Join Paul Dempsey and distinguished verification leaders with European connections who will represent an accurate picture of what progress has been made and what is still missing in functional verification. They will attempt to sort out which standards are gaining momentum and recommend a sensible way to develop a functional verification strategy to manage today's challenges. Audience participation in the debate is welcome.

Each panelist will deliver a 5-7 minute technical talk, including practical examples and user experiences. After the presentations, panelists will interact with the audience to discuss and debate the presented material, challenges and address next-generation solutions. Recommendations for future developments are expected. The panelists are:

- **Mike Bartley**, President and CEO, *TVS*: "General overview of verification with an emphasis on Planning and Metrics"
- **Lauro Rizzatti**, Verification and hardware emulation expert: "A practical look at the latest developments in hardware emulation, including its use in hardware/software verification"
- **Raik Brinkmann**, President and CEO, *OneSpin Solutions*: "Evolving formal techniques for mainstream verification, including high-end, safety-critical applications"
- **Colin McKellar**, Senior Director of Hardware Engineering, *Imagination Technologies* and Chairman Accellera UCIS Committee: "Report from the trenches: Optimizing a multi-facetted verification environment"
- **Holger Busch**, Senior Staff Engineer, Automotive Group, *Infineon Technologies*: "Report from the trenches: Driving a new level of verification excellence for safety-critical designs"

Moderator: **Paul Dempsey**, *Tech Design Forum*, United Kingdom

Wednesday, November 11

Tutorial T13: The How To's of Advanced Mixed-Signal Verification

Tutorial Sponsored By:

cadence

Forum 2+3 **15:30 – 17:00**

Today's modern applications in automotive, wireless, consumer, power management and industrial domains require high degree of interoperability between the analog and digital functionality. Due to strong interdependences as well as the ever-increasing complexity of today's designs, verifying the analog and digital functionality independently can lead to failing silicon. Also, relying on transistor-level simulations in functional verification does not scale well with the challenging and numerous requirements of todays' SoC anymore. Furthermore, power considerations impact architecture and tradeoffs even in mixed-signal design and causes additional challenges to verification.

This tutorial will present state-of-the-art metric-driven verification methodology required to address the ever-increasing, functional verification challenges in mixed-signal designs. The key components of the methodology will be described, including:

- Introduction in Metric-Driven Verification (MDV)
- Unified verification planning and management
- Reusable testbench development with constraint random stimuli, by applying Universal Verification Methodology (UVM) constructs on analog and mixed-signal as well
- Abstraction of analog functionality using Real Number modeling capabilities in Verilog-AMS and SystemVerilog
- Using assertions to automate checking of analog functionality
- Concepts of functional coverage applied in analog domain

The methodology will be demonstrated on real case studies using an N-Fractional PLL.

Presenters:

Kawe Fotouhi, *Cadence Design Systems*, Germany

Ahmed Osman, *Cadence Design Systems*, Germany

John Brennan, *Cadence Design Systems*, USA

Wednesday, November 11

Tutorial T14: UVM Hardware Assisted Acceleration with FPGA Co-emulation

Tutorial Sponsored By:

ALDEC
THE DESIGN VERIFICATION COMPANY

Forum 8 **15:30 – 17:00**

A verification platform (such as an FPGA system) must interoperate with the existing verification environment such as Universal Verification Methodology (UVM). This requirement is the motivation of this tutorial which explains an approach that provides a UVM test environment that is acceleration ready, through the use of the Accellera SCE-MI standard. Delegates will learn how this approach allows tests to be run in simulation and then accelerated on an FPGA Co-emulator through use of a SCE-MI compiler.

The tutorial introduces the FPGA Co-emulator, highlighting the key differences in capability to that of traditional ASIC FPGA prototyping platforms. We will introduce the SCE-MI standard and how its use enables a reusable test environment for simulation and acceleration with an FPGA Co-emulation.

The tutorial provides an example of a UVM test environment, which uses Doulos's Easier UVM coding style and guidelines. We take a step by step approach to demonstrate how to modify the UVM example to enable a test environment that can be simulated in a HDL simulator as well as accelerated with Co-emulation using FPGAs. To enable a common environment a transaction layer is used utilizing SystemVerilog DPI-C & SCE-MI function based use model.

Finally we introduce SCE-MI compilation to convert DPI-C function calls to a fully synthesizable code that can be implemented in a FPGA Co-emulator.

Target Audience: Verification and design engineers with the requirement to accelerate RTL verification tests. No prior experience of FPGA use is required. Familiar with UVM and similar test environments.

Presenters:

Alex Grove, *Aldec*, United Kingdom
Susanne Bar, *eVision Systems*, Germany

Wednesday, November 11

Tutorial Sponsored By:

AMIQ Consulting

Tutorial T15:
SystemVerilog Assertions Verification

Forum 10+11 **15:30 – 17:00**

SystemVerilog Assertions (SVA or simply assertions) are one of the central pieces in functional verification for protocol checking or validation of specific functions. In order to benefit from assertion advantages (fast, synthesizable, non-intrusive, coverable), one must be sure that assertions work as intended. This requires the assertion developer to adhere to an SVA development flow, which stretches from assertion planning, through implementation to assertion verification.

This tutorial guides you through the process of creating robust SVAs with a focus on verification:

- Planning
- Implementation (coding guidelines, common pitfalls)
- Assertion verification with SVAUnit (SVAUnit framework, self-checking tests, debug)
- SVA test patterns

We will use SVAUnit as a platform for SVA verification, since it addresses all identified requirements:

- decouple assertion validation code from assertion definition code
- simplify the generation of a wide range of stimuli, from 1 bit signal toggling to transactions
- provide the ability to reuse scenarios
- provide self-checking mechanisms
- report test status automatically
- integrate with major simulators and regression managers

This approach can be complemented by using a formal engine to explore assertion behavior and discover temporal sequences that cannot be covered.

The tutorial closes with the presentation of SVA test patterns for the most common temporal sequences and scenarios. This helps one better understand how the most simple building blocks of temporal sequences can be verified and, as a consequence, can speed-up SVA validation.

Presenter:

Ionut Ciocirlan, *AMIQ Consulting*, Romania

Andra Radu, *AMIQ Consulting*, Romania

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Wednesday, November 11

Panel Session: Functional Safety in the Automotive Value Chain

Großer Saal (Forum 1+2+3) **17:15 – 18:00**

Electronic content in cars is growing rapidly. The next big vision of human mobility is the autonomous driving car and it will require innovation on an unprecedented scale. That is not only attracting the automotive OEMs but a wide array of companies in the traditional automotive design chain as well as companies without any automotive history. Autonomous driving cars not only increases the electronic content of a car, but makes it obvious that such a system needs to operate safely to prevent human injuries. This includes both normal operation and safe response to unexpected or unplanned events throughout the operational lifetime of the car.

Since cars are not simple systems but rather highly complex assemblies of several systems many different disciplines need to work together. Public standards like the ISO26262 were defined to provide a framework for the players to be able to build such a safe products. The ongoing work in ISO 26262 2nd edition is adding more focus to integrated circuits (in the new ISO 26262-11 part). Still, the design chain up to the complete car is long and every element in the chain not only has its own challenges but also needs to take care indirectly of the challenges of the following chain elements.

The panel "Functional Safety in the Automotive Value Chain" brings together experts of the different elements of the value chain to explore their challenges and viewpoints. The panel covers the following areas:

- EDA – **Jean Marc Forey**, *Synopsys*
- Semiconductor – **Michael Rohleder**, *Freescale*
- Embedded Software – **Frank van den Berg**, *Green Hills Software*
- ISO 26262 – **Riccardo Mariani**, *Yogitech*

Moderator: **Joachim Geishauser**, *Freescale*

Birds-of-a-Feather Sessions

UCIS Coverage Birds-of-a-Feather Meeting

Wednesday, November 11, Forum 2 **18:30 – 19:30**

Building a multi-technology verification methodology (e.g. simulation, formal, emulation, etc.) is becoming both critical and complex. One of the cornerstones of such a methodology is the meaningful collation of coverage from different sources, and it is this objective that Accellera's Unified Coverage Interoperability Standard (UCIS) is aimed. The standard is now being improved to encompass different verification approaches, and the team would like to understand from end-users what exactly is required to make it effective. This is your chance to influence an industry-wide, combined coverage solution for your situation, and we would greatly value your input.

SystemC Birds-of-a-Feather Meeting

Wednesday, November 11, Forum 8 **18:30 – 19:30**

Given the strong SystemC community in Europe, DVCon Europe brings a great opportunity to discuss the current state-of-the art and future trends of SystemC in an informal get-together. Discuss your latest experience and missing features with fellow SystemC experts and members of different Accellera SystemC-related working groups. Possible topics include, but are not limited to: Leveraging C++14 in SystemC – what's possible today and tomorrow? | Connecting the dots – missing pieces in the core language for related standardization efforts (Multi-Language WG, CCIWG, VWG, IEEE P2415, …) | TLM-2.0 beyond memory-mapped interfaces.

DVConnect Reception

One of the main reasons to come to **DVCon Europe** is to start networking with your peers!

The DVConnect Reception gives you a venue to get connected with design and verification experts and to grow your professional network!

Sponsored by:

Date, Time & Location:

Wednesday, November 11, 18:30 – 19:30, Foyer Großer Saal

Gala Dinner

Sponsored by:

Join us for the Gala Dinner, a unique networking event to interact with industry professionals to exchange know-how and learn how other companies tackle their design and verification challenges. Dinner intermezzos and talks:

- Accellera Update
- Synopsys Solutions for Addressing Automotive Verification Challenges

Date, Time & Location:

Wednesday, November 11, 20:00 – 22:30, Ballsaal

Dress code: Business-Casual

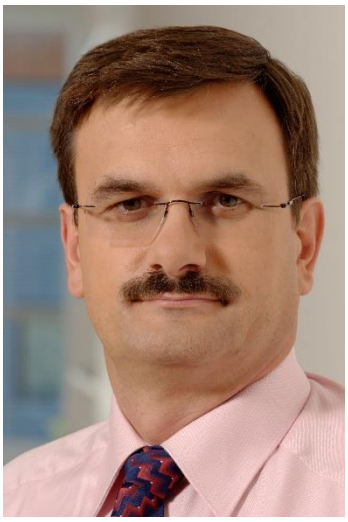
Note: One Gala Dinner ticket is included with your conference registration. You may also purchase an additional Gala Dinner ticket with your registration if you would like to bring a guest.
On-site registration for the dinner is not possible

Program-at-a-Glance – Thursday, Nov. 12

	Track 1 (Forum 1)	Track 2 (Forum 2+3)	Track 3 (Forum 8)
8:30 – 8:45	**Welcome & Overview** (Großer Saal)		
8:45 – 9:35	**Keynote : On the Road to Self-driving Cars** (Großer Saal)		
10:00 – 11:00	Advanced Verification & Validation - 1 TA1.1, TA1.2	System Level Design & Verification - 1 TA2.1, TA2.2	Design for Functional Safety - 1 TP1.1, TP1.2
11:00 – 11:30	**Coffee Break & Exhibition** (Foyer Großer Saal)		
11:30 – 12:30	Advanced Verification & Validation - 2 TA1.3, TA 1.4	System Level Design & Verification - 2 TA2.3, TA2.4	Design for Functional Safety - 2 TP1.3, TP1.4
12:30 – 14:00	**Lunch & Exhibition** (Foyer Großer Saal)		**Poster Session** (Forum 10+11) 12:45 – 13:45
14:00 – 15:30	Advanced Verification & Validation - 3 TA1.5, TA1.6, TA1.7	IP Reuse & Design Automation TA3.1, TA3.2, TA3.3	Analog/Mixed-Signal Design & Verification TA4.1, TA4.2, TA4.3
15:30 – 16:00	**Coffee Break & Exhibition** (Foyer Großer Saal)		
16:00 – 17:00	Advanced Verification & Validation - 4 TA1.8, TA1.9	Low Power Techniques TP2.1, TP2.2	RTL Simulation Techniques TA5.1, TA5.2
17:15 – 17:45	**Best Paper & Poster Award** (Großer Saal)		
17:45 – 18:00	**Closure of the Conference** (Großer Saal)		
18:00	***End of Conference***		

DVCon Europe Keynote

Keynote Speaker: Hans Adlkofer



Vice President Automotive System Group,
Infineon Technologies AG, Neubiberg, Germany

On the Road to Self-driving Cars

Forty years ago there were nearly NO semiconductors in the cars, with the most sophisticated electronics consisting of generators, relays and light bulbs. Today, the car is dominated by electronics, and 80% of the innovation is based on semiconductors. We stand on the border of e-mobility, advanced driver assist systems, and inter-connected cars, and yet, despite 80 million new cars on the road every year, we have the lowest casualty level ever. The number of cars, especially in the fast growing megacities, will require modernized mobility concepts that will have a significant impact on the automotive industry.

Looking 40 years down the road we will see more and larger megacities developing around the world. People will be online 24 hours a day and this will drive a home and office global workplace. These changes will have a major impact on the use of cars. Megacities cannot handle the traffic levels created by private cars and, therefore, the integration of mobility concepts will be a key city planning issue to avoid constant traffic jams, air pollution, and parking problems, in the name of convenient and efficient transport. Flexible and integrated mobility concepts will drive changes, such as car sharing, autonomous driving, and connected car innovations. New car concepts, from 3 wheelers to automated convoys, will emerge.

The semiconductor industry will be challenged to support evolving and emerging requirements that enable self-driving vehicles, by providing semiconductors with high compute power, fast network performance, and redundant features for functionally safe operation. This will require multiple steps of learning by experience, system optimization, and new, innovative technologies in semiconductors. This means consumer and other technologies reapplied to, and new innovations fulfilling, automotive requirements.

Functional safety, cyber security and energy on-demand requirements will drive a reorganization of electronic vehicle architectures and partitioning. Domain control will become standard, with major backbone communication operating between those domains. Vehicles will be connected to other vehicles, as well as the community infrastructure.

This keynote will provide a glimpse into the future, taking you "on the road to self-driving cars."

Biography: Hans Adlkofer studied electronics with a focus on semiconductor technologies. He started his career at National Semiconductor in the marketing department working on ASICs for the automotive industry, before moving to Giesecke & Devrient to develop secure operating systems for smart cards. He was then asked to take charge of the application center for Security and Smart Card ICs at Siemens Semiconductor (today Infineon Technologies), later moving to Singapore to head up the company's business operation for the Asian market. In 2003 he took over responsibility for the Sensors Business Unit at Infineon, and since 2009 he has been leading the system group activities in the Automotive Division of Infineon.

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Technical Sessions Overview

Presentations, 10:00 – 11:00

Session TA1: Advanced Verification & Validation – 1, Forum 1

Session TA2: System Level Design & Verification – 1, Forum 2+3

Session TP1: Design for Functional Safety – 1, Forum 8

Presentations, 11:30 – 12:30

Session TA1: Advanced Verification & Validation – 2, Forum 1

Session TA2: System Level Design & Verification – 2, Forum 2+3

Session TP1: Design for Functional Safety – 2, Forum 8

Poster Session, 12:45 – 13:45

Poster session in Forum 10+11

Presentations, 14:00 – 15:30

Session TA1: Advanced Verification & Validation – 3, Forum 1

Session TA3: IP Reuse & Design Automation, Forum 2+3

Session TA4: Analog/Mixed-Signal Design and Verification – 1, Forum 8

Presentations, 16:00 – 17:00

Session TA1: Advanced Verification & Validation – 4, Forum 1

Session TP2: Low Power Techniques, Forum 2+3

Session TA5: RTL Simulation Techniques, Forum 8

Thursday, November 12

Session TA1: Advanced Verification & Validation – 1

Forum 1 **10:00 – 11:00**

Chair: **Yann Oddos** – *Intel*

TA1.1 **Is Your Testing N-wise or Unwise? Pairwise and N-wise Patterns in SystemVerilog for Efficient Test Configuration and Stimulus**
Jonathan Bromley, Kevin Johnston, *Verilab*

TA1.2 **UVM Light: A Subset of UVM for Rapid Adoption**
Stuart Sutherland, *Sutherland HDL*;
Gordon Allan, Tom Fitzpatrick, *Mentor Graphics*

Session TA2: System Level Design & Verification – 1

Forum 2+3 **10:00 – 11:00**

Chair: **Christian Sauer** – *Cadence*

TA2.1 **Boosting SystemC-based Testbenches with Modern C++ and Coverage-Driven Generation**
Hoang M. Le, Rolf Drechsler, *University of Bremen*

TA2.2 **Virtual Prototyping in SpaceFibre System-on-Chip Design**
Elena Suvorova, Nadezhda Matveeva, **Ilya Korobkov**, Alexey Shamshin, Yuriy Sheynin, *Saint-Petersburg State University of Aerospace Instrumentation*

Session TP1: Design for Functional Safety – 1

Forum 8 **10:00 – 11:00**

Chair: **Harry Foster** – *Mentor Graphics*

TP1.1 **A Meta-Model-Based Approach for Semantic Fault Modeling on Multiple Abstraction Levels**
Michael Schwarz, *TU Kaiserslautern*; Moomen Chaari, Bogdan-Andrei Tabacaru, Wolfgang Ecker, *Infineon Technologies*

TP1.2 **Who Takes the Driver Seat for ISO 26262 and DO 254 Verification?**
Avidan Efody, *Mentor Graphics*

Thursday, November 12

Session TA1: Advanced Verification & Validation – 2

Forum 1 **11:30 – 12:30**

Chair: **Clemens Roettgermann** – *Freescale Semiconductor*

TA1.3 **An Efficient Verification Framework for Audio/Video Interface Protocols**
Noha Shaarawy, Mustafa Khairallah, Khaled Khalifa, Hany Salah, Amr Salah, *Boost Valley*; Maged Ghoneima, *Ain Shams University*

TA1.4 **A Novel Processor Verification Methodology Based on UVM**
Abhineet Bhojak, Tejbal Prasad, **Stephan Herrmann**, *Freescale Semiconductor*

Session TA2: System Level Design & Verification – 2

Forum 2+3 **11:30 – 12:30**

Chair: **Horst Rieger** – *Renesas*

TA2.3 **The Application of Formal Technology on Fixed-Point Arithmetic SystemC Designs**
Sven Beyer, Dominik Strasser, David Kelf, *OneSpin Solutions*

TA2.4 **Automated SystemC Model Instantiation with Modern C++ Features and sc_vector**
Ralph Görgen, *OFFIS*; Philipp A. Hartmann, *Intel*; Wolfgang Nebel, *Carl von Ossietzky University Oldenburg*

Session TP1: Design for Functional Safety – 2

Forum 8 **11:30 – 12:30**

Chair: **Matthias Bauer** – *Infineon Technologies*

TP1.3 **An Automated Formal Verification Flow for Safety Registers**
Holger Busch, *Infineon Technologies*

TP1.4 **Achieve Complete SoC Memory Map Verification Through Efficient Combination of Formal and Simulation Techniques**
Clemens Roettgermann, Peter Limmer, Michael Rohleder, *Freescale Semiconductor*

Thursday, November 12

Session TA1: Advanced Verification & Validation – 3

Forum 1 **14:00 – 15:30**

Chair: **Walter Tibboel** – *NXP*

TA1.5 **Integration of Modern Verification Methodologies in a TCL Test Framework**
Matteo De Luigi, Alessandro Ogheri, *Ogheri Consulting*

TA1.6 **Virtual Models for Software and Firmware Development and Validation of a Complex IP within System Context**
Rocco Jonack, *Intel*

TA1.7 **OSVVM and Error Reporting**
Jim Lewis, *SynthWorks*

Session TA3: IP Reuse & Design Automation

Forum 2+3 **14:00 – 15:30**

Chair: **Oliver Bell** – *Intel*

TA3.1 **Universal Scripting Interface for SystemC**
Rolf Meyer, Jan Wagner, Rainer Buchty, *TU Braunschweig*;
Mladen Berekovic, *C3E, TU Braunschweig*

TA3.2 **An Easy VE/DUV Integration Approach**
Uwe Simm, *Cadence Design Systems*

TA3.3 **Web Template Mechanisms in SOC Verification**
Rinaldo Franco, Alberto Allara, *STMicroelectronics*

Session TA4: Analog/Mixed-Signal Design & Verification

Forum 8 **14:00 – 15:30**

Chair: **Joen Westendorp** – *NXP*

TA4.1 **Comprehensive AMS Verification Using Octave, Real Number Modelling and UVM**
John McGrath, Patrick Lynch, Ali Boumaalif, *Xilinx*

TA4.2 **Integrating a Virtual Platform Framework for Smart Devices**
Valerio Guarnieri, Francesco Stefanni, Franco Fummi, *EDALab*;
Michelangelo Grosso, Davide Lena, *ST-POLITO*;
Angelo Ciccazzo, Giuliana Gangemi, Salvatore Rinaudo, *STMicroelectronics*

TA4.3 **Wave Digital Filter Modeling for Complex Automotive Sensor Load Case Verification**
Andrei Basa, Thang Nguyen, Dirk Hammerschmidt, *Infineon Technologies*

Thursday, November 12

Session TA1: Advanced Verification & Validation – 4

Forum 1 **16:00 – 17:00**

Chair: **Adiel Kahn** – *Synopsys*

TA1.8 **Leveraging the UVM Register Abstraction Layer for Memory Sub-System Verification**
Tudor Timisescu, *Infineon Technologies*; **Uwe Simm**, *Cadence Design Systems*

TA1.9 **Closing the Loop from Requirements Management to Verification Execution for Automotive Applications**
Walter Tibboel, **Jan Vink**, *NXP Semiconductors*

Session TP2: Low-Power Techniques

Forum 2+3 **16:00 – 17:00**

Chair: **Mike Bartley** – *Test and Verification Solutions*

TP2.1 **Power Aware CDC Verification of Dynamic Frequency and Voltage Scaling (DVFS) Artifacts**
Mark Handover, Jonathan Lovett, Kurt Takara, *Mentor Graphics*

TP2.2 **Refining Successive Refinement: Improving a Methodology for Incremental Specification of Power Intent**
Desinghu Ps, Adnan Khan, *ARM*;
Gabriel Chidolue, Erich Marschner, Gustav Bjorkman, *Mentor Graphics*

Session TA5: RTL Simulation Techniques

Forum 8 **16:00 – 17:00**

Chair: **Alexander Rath** – *Infineon*

TA5.1 **Accelerating RTL Simulation Techniques**
Lior Grinzaig, *ADVA Optical Networking*

TA5.2 **Challenges of VHDL X-propagation Simulations**
Karthik Baddam, *Imagination Technologies*; Piyush Sukhija, *Synopsys*

Thursday, November 12

Poster Session

Forum 10+11 **12:45 – 13:45**

Chair: **Mike Bartley** – *Test and Verification Solutions*

P1.1 **New Trends in RTL Verification: Bug Localization, Scan-Chain-Based Methodology, GA-Based Test Generation**
Khaled Mohamed, *Mentor Graphics*

P1.2 **Simplifying UVM in SystemC**
Thilo Voertler, *Fraunhofer IIS/EAS*; Thomas Klotz, **Felix Assmann**, *Bosch Sensortec*; Karsten Einwich, *COSEDA Technologies*

P1.3 **Designing the Future With Efficiency**
Axel Scherer, *Cadence Design Systems*; Junette Tan, *PMC Sierra*

P1.4 **UVM and Emulation: How To Get Your Ultimate Testbench Acceleration Speed-up**
Ahmed Yehia, **Hans van der Schoot**, *Mentor Graphics*

P1.5 **A Concept for Expanding a UVM Testbench to the Analog-centric Toplevel**
Felix Assmann, Axel Strobel, *Bosch Sensortec*;
Hans Zander, *Cadence Design Systems*

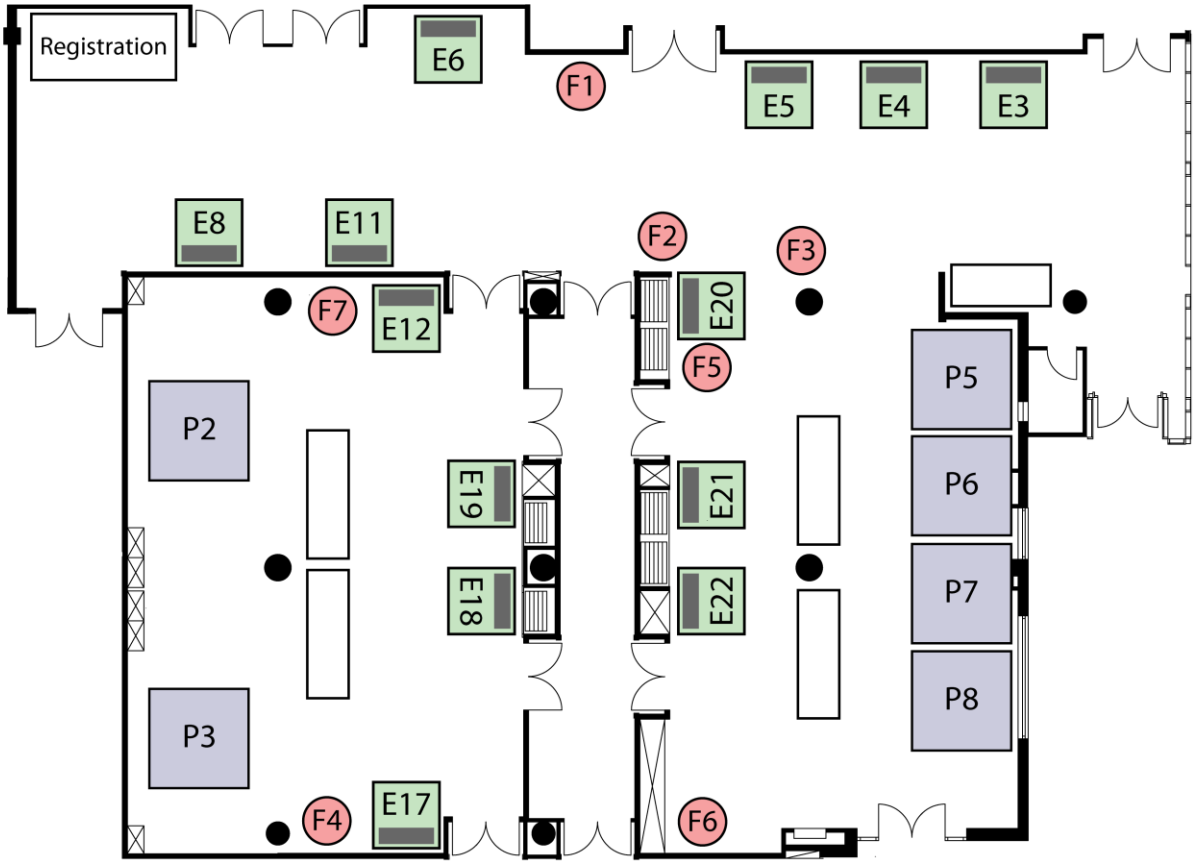
P1.6 **Efficient Constrained Random Generation of Address Blocks**
Meenakshy Ramachandran, *Synopsys*

P1.7 **Paving a Path to Hardware-Based Acceleration in a Single UVM Environment**
Axel Scherer, *Cadence Design Systems*; Mark Azadpour, *Western Digital*

P1.8 **A SystemC-based UVM Verification Infrastructure**
Mike Bartley, Harshavardhan Narla, *Test and Verification Solutions*

DVCon Europe Conference and Exhibition Floor Plan

DVCon Europe Exhibition Floor Plan and Exhibitors List



E21	Aldec	E22	Exostiv Labs
P8	AMIQ EDA	E6	Magillem
F5	Andes	E8	Mathworks
E3	Avery	P5, F1	Mentor Graphics
F7	Boost Valley	P6	OneSpin Solutions
P3	Cadence	F4	Real Intent
E20	COSEDA	E11	SmartDV
E4	Cyient	P2	Synopsys
E12	Dini Group	E5	SyoSil
E19	Dizain-Sync	F2	TVS
E17	Doulos	E18	Verific
F6	ECSI	P7	Vtool
F3	EDALab		

Exhibitor Listing

Aldec

Exhibitor location: E21

www.aldec.com

Established in 1984, Aldec is global industry leader in Electronic Design Verification. Aldec offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, SoC and ASIC Prototyping, Design Rule Checking, IP Cores, Requirements Lifecycle Management, DO-254 Functional Verification and Military/ Aerospace solutions.

AMIQ EDA

Exhibitor location: P8

www.amiq.com

AMIQ EDA provides software tools that enable design and verification engineers to increase the speed and quality of new code development, simplify debugging and legacy code maintenance, accelerate language and methodology learning, improve testbench reliability, extract automatically accurate code documentation, and implement best coding practices.

Its flagship solution, **DVT Eclipse IDE**, is a modern, powerful, and complete code development environment for the e language, SystemVerilog, Verilog, VHDL, and mixed-language projects, which enables engineers to address the increasing complexity in hardware design and verification. It integrates with all major simulators and provides UVM-oriented features that simplify verification environment creation and debugging. The **DVT Debugger** is an optional add-on module to the DVT IDE. It provides advanced debugging capabilities and allows users to perform debugging from the same place where they develop their code.

Verissimo SystemVerilog Testbench Linter is a SystemVerilog coding guideline and UVM compliance checker that enables engineers to perform a thorough audit of their testbenches. It can be used in batch mode or integrated with DVT.

Specador Documentation Generator automatically generates accurate HTML documentation based on effective code compilation and comments analysis. It works in batch mode and uses dedicated language parsers for e, SystemVerilog, Verilog, and VHDL.

AMIQ EDA serves customers around the world and is recognized for its high quality solutions and customer service responsiveness.

Exhibitor Listing

Andes Technology

Exhibitor location: F5

www.andestech.com

Andes Technology Corporation was founded in Hsinchu Science Park, Taiwan in 2005 to develop innovative high-performance/low-power 32-bit processor cores and its associated development environment to serve worldwide rapidly-growing embedded system applications. It delivers the best super low power CPU cores with integrated development environment and associated software and hardware solutions for SoC development. In order to meet demanding requirements of today's electronic devices, Andes delivers configurable software/hardware IP and scalable platforms to respond to customers' needs for quality products and faster time-to-market. Andes' comprehensive CPU includes entry-level, mid-range, high-end, extensible and security families to address full range of embedded electronics products, especially for connected, smart and green applications. For more information about Andes Technology, please visit **www.andestech.com**.

Avery

Exhibitor location: E3

www.avery-design.com

Avery is a leader in functional verification solutions. Our SimXACT is a comprehensive, patented solution to automatically eliminate X bugs in RTL and gate-level simulation due to X-optimism and X-pessimism issues. Our Verification IP providing robust models, protocol checking, compliance testsuites, advanced UVM environment, and verification services for advanced protocols including PCI Express, USB/xHCI, UAS/BOT, UFS/UFSHCI, NVMe, SATA Express, SATA, UniPro, Soundwire, CSI-2, DSI-2, eMMC, SDIO, DDR4/LPDDR4, HBM, HMC, ONFI/Toggle, CAN FD, and ACE/AXI3/AXI4/AHB.

Boost Valley

Exhibitor location: F7

www.boostvalley.com

Boost Valley is a digital design and verification specialized firm, building its own Verification IPs as well as providing senior level quality consultation services in Digital Design/Verification domains. Our goal is to establish strategic alliances designed to help deliver a client-centric, total solutions approach to solving problems, exploiting business opportunities and creating sustainable competitive advantage for our clients.

Exhibitor Listing

Cadence Design Systems

Exhibitor location: P3

www.cadence.com

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software, hardware, IP, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at **www.cadence.com**.

COSEDA

Exhibitor location: E20

www.coseda-tech.com

Located in Dresden, Germany, **COSEDA Technologies GmbH** provides the design environment COSIDE®, which is the perfect tool to develop and design innovative heterogeneous hardware as well as software systems. COSIDE® is the first commercial design environment based on the SystemC and SystemC AMS standards to model and simulate highly complex analog and digital systems. The modeling language SystemC AMS is closing the gap between the analog and digital world and between idea, concept and implementation in the design process of complex electronic systems within a heterogeneous environment. It allows a holistic design approach by considering the different worlds of development jointly. SystemC AMS enables overall system modeling and virtual prototyping. COSIDE® is the way to benefit from it.

Cyient

Exhibitor location: E4

www.cyient.com

Cyient is a well-established global provider of engineering, data analytics, network and operations solutions. Strong capabilities combined with a global network of more than 12,500 associates across 38 global locations enable us to deliver measurable and substantial benefits to major organizations worldwide. Our solutions include product development and life-cycle support, process and network engineering, and data transformation and analytics.

For more than 15 years, we have designed engineering solutions for your semiconductor development challenges, offering concept-to-silicon and system prototype services. We have developed a track record of providing first-pass silicon success in all areas of system-on-chip (SOC) and intellectual property (IP). And we collaborate with leading fabrication houses and EDA tool vendors to offer complete VLSI services for the global semiconductor industry.

Exhibitor Listing

The Dini Group

Exhibitor location E12

www.dinigroup.com

Located in La Jolla, California, **The Dini Group** is a professional hardware and software engineering firm, specializing in high performance digital circuit design and application development for all ASIC prototyping, High Performance Computing, Algorithmic Acceleration and Low Latency Networking projects, with emphasis on BIG FPGA boards.

Dizain-Sync

Exhibitor location: E19

www.dizain-sync.com

With over 25 years of experience, **Dizain-Sync** offers a unique perspective on the combination of EDA, PLM, Design and Educational services.

Dizain-Sync is the best partner to configure the required software to the wishes of the customer and to maintain the design environment to ensure the customer can always trust on an optimal situation.

Dizain-Sync is able to advise, set up and maintain a PLM system and all other activities concerning the control of product development during the design process.

Dizain-Sync's design activities are meant to help out customers at solving complex design challenges. Dizain-Sync can provide companies with the latest technological knowledge. Dizain-Sync can also provide companies with temporary employees to help out during a design project.

Since 1988 Dizain-Sync has been offering a wide range of training classes (Verilog, VHDL, SystemC, SystemVerilog, UVM).

Exhibitor Listing

Doulos

Exhibitor location: E17

www.doulos.com

Doulos is the global leader for the development and delivery of world class training solutions for engineers creating the world's electronic products. Fully independent, Doulos sets the industry standard for the highest quality training programs for design and verification engineers implementing complex SoC and FPGA designs.

Doulos training programs cover the needs of hardware designers, embedded software developers and system design and verification specialists, including courses for C, C++, Embedded Linux, SystemC, Verilog®, SystemVerilog, UVM, VHDL and ARM®-based design.

This year Doulos is celebrating 25 years of providing 'service through excellence', contributing to the success of more than 3000 companies across over 60 countries. The natural partner for leading tool and technology companies, Doulos schedules face-to-face classes across the U.S. and Europe, and delivers in-house and online training programs world-wide. For more information, visit **www.doulos.com**.

ECSI

Exhibitor location: F6

www.ecsi.org

ECSI (European Electronic Chips & Systems design Initiative), an international research association in system design methodology tools, flows and standards, will present results of four innovative R&D collaborative projects:

- **CRAFTERS** (ConstRaint and Application driven Framework for Tailoring Embedded Real-time Systems)
- **PAPP** (Portable and Predictable Performance on Heterogeneous Embedded Manycores)
- **OpenES** (Open ESL Technologies for Next Generation Embedded Systems)
- **CONTREX** (Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties)

Exhibitor Listing

EDALab

Exhibitor location: F3

www.edalab.it

EDALab is a software house committed in the development of the HIFSuite Tools, a set of tools for the automatic manipulation and translation in SystemC/C++ of HDL modules (both VHDL and Verilog). The HIFSuite Tools can be purchased with a commercial license and a demo version for Windows and Linux can be downloaded from the website.

One of the most interesting tools of the suite is the Automatic Abstraction Tool (A2T) that automatically abstracts VHDL and Verilog modules in SystemC TLM or C++ and sets them ready to be simulated inside a Virtual Platform 100x or even 1000x faster than RTL. EDALab also provides design services and consultancy based on HIFSuite tools and targeted for Virtual Platforms and ESL domain.

EDALab s.r.l. is located in Verona, in the north of Italy, and was funded in 2007. Today it employs about 15 people, some of them are connected with the Electronic Design System research group of the University of Verona.

Exostiv Labs

Exhibitor location: E22

www.exostivlabs.com

Located in Belgium, **Exostiv Labs** is a division of Byte Paradigm that focuses on providing innovative debug & verification solutions to the FPGA design community. At Exostiv Labs, it is believed that the ability to see inside the chips is the way to build better design.

Its flagship solution **EXOSTIV™** is the first FPGA in-lab debug solution that provides Gigabyte-range visibility with a minimal footprint on the target chip resources. EXOSTIV™ combines a large storage outside the chip with advanced analysis tools and flexible embedded instrumentation IP, providing up to 200.000 times more visibility over FPGA at system speed.

By allowing deeper captures and providing more flexibility with its instrumentation IP, EXOSTIV™ reduces the number of implementation runs required to find bugs and thereby, reduces the total time spent on FPGA debug and verification.

Exhibitor Listing

Magillem

Exhibitor location: E6

www.magillem.com

Magillem provides to customers in the electronic industry tools and services that drastically reduce the global cost of complex design. Magillem has developed an easy to use, state of the art platform solution to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SoC.

MathWorks

Exhibitor location: E8

www.mathworks.com

MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development. MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields, such as financial services and computational biology. For more information visit **mathworks.com**

Mentor Graphics

Exhibitor location: P5, F1

www.mentor.com

Mentor Graphics delivers the most comprehensive Enterprise Verification Platform (EVP), which combines Questa® for high performance simulation, verification management and coverage closure, low-power verification with UPF, CDC, Formal Verification, accelerated functional coverage, and processor-based hardware verification, Veloce® emulation platform and OS3 operating system, and the Visualizer™ debug environment, to deliver performance and productivity improvements ranging from 400X to 10,000X. For more information visit **www.mentor.com**.

Exhibitor Listing

OneSpin Solutions

Exhibitor location: P6

www.onespin-solutions.com

OneSpin Solutions is a pioneer of advanced formal techniques to solve practical verification challenges. The company's award winning, leading technology enables a versatile range of verification solutions. Products include easy to use, automated apps for the early detection of design issues and targeted problems, comprehensive coverage-driven property analysis for rigorous testing, and high accuracy equivalency checking for large FPGAs. OneSpin is on the forefront of formal technical leadership in areas such as Safety Critical design verification and C-based algorithm verification.

Real Intent

Exhibitor location: F4

www.realintent.com

Real Intent is the leading provider of static verification software for sign-off of SoC and FPGA designs. Meridian CDC provides complete analysis and debug of clock-domain crossing and reset-domain crossing issues; Ascent Lint is the fastest and lowest-noise RTL linter available in the market. Ascent XV provides complete analysis of all x-propagation and power-up in only hours and replaces simulation. Ascent IIV autoformal analyzer finds RTL bug automatically without testbenches.

SmartDV

Exhibitor location: E11

www.smart-dv.com

SmartDV creates high quality standard and custom protocol verification intellectual property (VIP), memory models and simulation acceleration VIP products designed to work with coverage-driven verification flows. The company's mission is to provide high-quality IP along with industry-best support at lower cost and to help remove limited licensing constraints, speeding up regressions and time to market. All SmartDV VIPs ship with a compliance test suite and are native UVM (or any language that a customer prefers) without any wrappers, which increases performance and simplifies debugging. Each VIP also is independently developed and verified against external design IP for highest quality. SmartDV has customers from wireless/mobile, storage, automotive, memory, networking and other domains.

For information on SmartDV's VIP portfolio, see **www.smart-dv.com/products.html**.

Exhibitor Listing

Synopsys

Exhibitor location: P2

www.synopsys.com

Synopsys is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at **www.synopsys.com**.

SyoSil

Exhibitor location: E5

www.syosil.com

SyoSil is a consulting company holding broad expertise within the field of System-on-Chip and ASIC solutions, including specification, methodologies, design and verification. We are specialized in verification strategies, advanced EDA verification tools including formal methods (property checking) and EDA tool languages/methodologies such as SystemVerilog/UVM.

TVS

Exhibitor location: F2

testandverification.com

TVS has over 130 hardware verification and software testing engineers working throughout Europe, Asia and the US. We help companies to reduce their time-to-market and improve product quality through tailored products and services for software testing and hardware verification.

Using well-defined technical and management processes executed by experts and supplemented by TVS tools, TVS is trusted by companies around the world to deliver efficient, effective solutions for both software testing and hardware verification.

TVS's flexible execution model delivers cost-effective resource when and where it is needed

Exhibitor Listing

Verific

Exhibitor location: E18

www.verific.com

Support your own RTL tools with **Verific's** industry standard (System)Verilog, VHDL, and UPF parsers! Verific Design Automation has provided (System)Verilog and VHDL front-ends to EDA, FPGA, and semiconductor computers for many years. With more than 60 active licensees worldwide, Verific's parsers are found everywhere. And all our APIs are available in Python, Perl, and C++.

Vtool

Exhibitor location: P7

www.thevtool.com

Vtool is a comprehensive functional verification platform that shortens the ever increasing ASIC and FPGA verification cycle, providing an efficient, reusable and maintainable verification process. The all-in-one interface brings together all parts of your team and all verification elements to create a sleek and convergent process from plan formulation through testbench implementation and debug.

Vtool fully integrates with existing SystemVerilog UVM and verification IPs technology, saving money and engineering effort by streamlining the verification process as a whole, for faster time-to-tapeout. Built-in architectural guidance cuts down the time that is usually spent in reuse, integration, team share, maintenance of millions of code-lines and debugging of the verification environment itself. This robust verification environment saves over 50% of the verification team's work time.

Best Paper and Poster Award and Form

DVCon Europe conference & exhibition attendees are entitled to vote for the "**DVCon Europe Best Paper and Poster**" awards. Please use this form, or any of the forms distributed at the conference, to share your vote:

Best Paper and Best Poster Award Sponsored by:

AMIQ EDA

Your Name: _____

Your Badge ID: _____

Best Paper # and Title: _____

Best Poster # and Title: _____

Please submit your vote in the "Best Paper and Poster" Box in the Foyer. The award ceremony takes place on Thursday, November 12 at 17:15 in the Großer Saal.

Please note the following rules and conditions:

- You cannot vote on your own or co-authored paper or poster
- You can only vote once. Multiple forms of the same attendee are excluded
- You can only vote on a paper or poster given at DVCon Europe

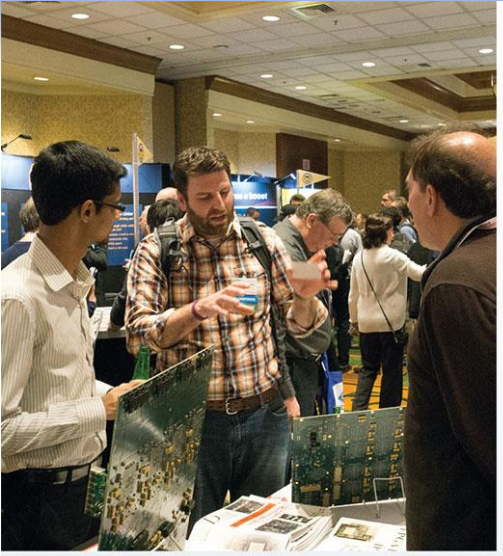
Tutorials and Proceedings Distribution

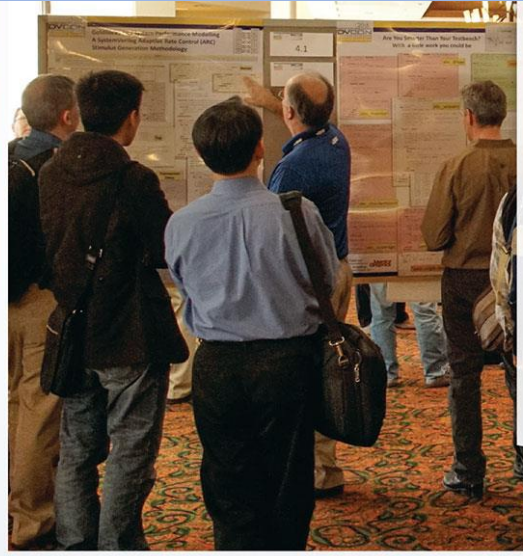
DVCon Europe proceedings and tutorials will be delivered electronically online via a username and password. To access the tutorials or proceedings, visit:

www.dvcon-europe.org/proceedings
Username = Email address
Password = Registration ID

You will receive a personal registration ID by email prior to the event to access the material you are eligible to view. Note that DVCon Europe will not distribute material via USB stick or CD.

Exhibiting Companies





2016
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES

February 29 - March 3, 2016 • DoubleTree Hotel, San Jose, CA

The Premier Conference for Design & Verification Engineers

Conference Dates

FEBRUARY 29 - MARCH 3, 2016

Conference Schedule

Monday, February 29
- Accellera Day Tutorials
- Exhibits

Tuesday, March 1
- Technical Sessions
- Keynote Speaker
- Exhibits

Wednesday, March 2
- Technical Sessions
- Panel Discussions
- Exhibits

Thursday, March 3
- Tutorials

Exhibition Dates

FEBRUARY 29 - MARCH 2, 2016

Exhibition Hours

Monday, February 29.....5:00 - 7:00pm

Tuesday, March 1.....2:30 - 6:00pm

Wednesday, March 2.....2:30 - 6:00pm

WHY ATTEND?

- DVCon continues to be the premier conference for design and verification engineers of all experience levels.
- Compared to larger and more general conferences, DVCon affords attendees a concentrated menu of technical sessions—tutorials, papers, poster sessions and panels—focused on design and verification hot topics.
- In addition to participation in high quality technical sessions, DVCon attendees have the opportunity to take part in the many informal, but often intense, technical discussions that pop-up around the conference venue among 800+ design and verification engineers and engineering managers.
- Networking Opportunities among peers is possibly the greatest benefit to DVCon attendees.
- DVCon attendees will have access to the vendors of advanced design and verification tools, IP/VIP and services who exhibit at the conference.

Sponsored by: accellera SYSTEMS INITIATIVE

View full conference details:
DVCon.org

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