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2014 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

October 14 -15, 2014
Hilton Munich City
Munich, Germany

Conference Program & Exhibition Guide

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Welcome to DVCon Europe

Martin Barnasconi
NXP Semiconductors
General Chair
DVCon Europe 2014

I am honored to invite you to the first **Design and Verification Conference and Exhibition** in **Europe**! On behalf of the DVCon Europe Steering Committee and the **Accellera Systems Initiative**, I welcome you to participate in this brand new conference in Europe on the application of Electronic Design Automation (EDA) standards, languages and methodologies for the design and verification of electronic systems and integrated circuits.

DVCon has been a very popular conference in Silicon Valley for more than 20 years. It's about time to bring this successful conference to Europe, offering a new venue where technical experts and industries can network; interact with EDA tool, IP and service providers; and focus on the learning and sharing of practical experiences in design and verification.

We've designed DVCon Europe for *you*, the users of EDA languages, tools, methodologies and standards, by creating an attractive program around the following themes:

- System Level Design
- Verification & Validation
- IP Reuse and Design Automation
- Mixed-Signal Design and Verification
- Lower Power Design and Verification

A true highlight in the program is the tutorial day on Tuesday, bringing you 14 fantastic tutorials to choose from. The morning session contains user-driven tutorials, whereas in the afternoon the tutorials are moderated by the EDA tool and service providers.

The program committee was delighted with the enormous number of submissions for this new conference, and it enabled them to create a strong technical program on Wednesday, with various paper sessions and a poster session. You are invited to vote on the best paper and poster, which will be announced at the closure of the conference.

DVCon Europe also brings a vendor exhibition. On Tuesday and Wednesday you can meet with EDA tool companies, training institutes and service providers to get in-depth demonstrations of their products and solutions. Benefit from this unique occasion of having many companies active in design and verification under one roof!

Finally, I would like to thank *you*, the users and vendors, for helping to shape DVCon Europe, by submitting papers or tutorials, and visiting the conference! I am looking forward to experiencing a vibrant and successful DVCon Europe, together with you.

Martin Barnasconi

2014 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

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Conference & Exhibition Highlights

DVCon Europe Opening and Overview:

Tuesday, October 14, 9:00 – 9:20, Ballroom Strauss A+B

Tutorials:

Tuesday, October 14, 9:30 – 17:30:

Ballroom Strauss A, Ballroom Strauss B, Salon Bialas + Studer

DVConnect Networking Reception:

Tuesday, October 14, 19:00 – 20:00, Foyer Strauss & Corridor

Accellera Dinner:

Tuesday, October 14, 20:00 – 22:30, Ballroom Strauss A+B

Note: Only for attendees who registered for this event.

Keynote:

Wednesday, October 15, 9:00 – 9:50, Ballroom Strauss A+B

Technical Presentations & Poster Session:

Wednesday, October 15:

Technical presentations: 10:00 – 17:00

Poster session: 12:45 – 13:45

Ballroom Strauss A, Ballroom Strauss B, Salon Bialas, Salon Studer

Best Paper and Best Poster Award:

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Exhibition:

Tuesday, October 14 & 15, Foyer Strauss & Corridor, Prime Exhibition Hours:

11:00 – 11:30, 13:00 – 14:00, 15:30 – 16:00, 17:30 – 20:00

Wednesday, October 15, Foyer Strauss & Corridor, Prime Exhibition Hours:

11:00 – 11:30, 12:30 – 14:00, 15:30 – 16:00

Registration Information

Registration Hours:

Tuesday, October 14: 8:00 – 17:00, Foyer Strauss

Wednesday, October 15: 8:00 – 12:00, Foyer Strauss

Registration Sponsored by:

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Registration Type	Registration Fee
Full Conference (**2 days**) Accellera Member	349€
Full Conference (**2 days**) Non-Member	399€
Tutorial Day (**1 day**, Oct. 14 only) Accellera Member	249€
Tutorial Day (**1 day**, Oct. 14 only) Non-Member	299€

All prices are in Euros, excluding tax (VAT).

Full conference (2 day) registration includes:

- DVCon Europe Conference entry fee (2 days)
- DVCon Europe Exhibition (2 days)
- Access to conference proceedings: web page with papers, presentations, keynotes
- Lunch on October 14 and 15
- Coffee breaks on October 14 and 15

Tutorial day (1 day) registration includes:

- DVCon Europe Conference entry fee on Tuesday, October 14 only (1 day)
- DVCon Europe Exhibition on Tuesday, October 14 only (1 day)
- Access to tutorial proceedings via website
- Lunch on October 14
- Coffee breaks on October 14

Additional registration options include:

- Accellera Dinner – October 14, 20:00 – 22:30. Space is limited to the first 180 participants registered for the dinner. Supplementary cost for the dinner: 20€

FDL registration

DVCon Europe participants get discounted registration rates to FDL. Please register at **www.ecsi/fdl** or visit the on-site FDL registration desk.

Hotel Information

DVCon Europe takes place at Hilton Munich City. Hilton Munich City is located close to downtown Munich, with only a 10 minute walk to visit the city center. The hotel is easy to reach by S-Bahn (Rosenheimer Platz) and 35 minutes by train from Munich Airport (Franz Josef Strauss).

Hotel address:

Hilton Munich City
Rosenheimer Strasse 15
81667 Munich, Germany
Tel: +49 (0)89 48 040

How to reach Hilton Munich City

From the airport by car: Turn on to Highway A92 then take Highway A9, signed for Munich. Follow the Highway until the exit for Munich East. Continue straight, then turn left onto Ludwigsbruecke and follow Rosenheimer Strasse directly to the hotel entrance. Distance to hotel appox. 35 km. Driving time appox. 30 min.

From the airport by train (S-Bahn): Take the S-Bahn "S8" from Munich Airport towards Munich center. The train station can be found between Terminals 1 and 2. Trains depart every 20 minutes, with a direct connection to station "Rosenheimer Platz" station reachable in 35 minutes. The Hilton Munich City hotel is situated directly above the station. Follow the signs to "Gasteig" and take the elevator to the lobby of the hotel. For this trip you need a one-way ticket of 4 zones, which currently costs 10.40 EUR. Alternatively, you might consider the Airport-City Day Ticket, which is a day ticket for the entire MVV network, valid from the moment you purchase until 6am the following day. There are also multi-day and partner tickets.

Estimated price by Taxi from Munich Airport: 60 EUR.

Conference Sponsor

Accellera Systems Initiative, the proud sponsor of DVCon Europe, is an independent organization with the mission to provide design and verification standards required by systems, semiconductor, IP and design tool companies to enhance a front-end design automation process. We collaborate with our community of members to deliver the standards that lower the cost of designing commercial EDA, IC and embedded systems solutions. As a result of its partnership with the IEEE, Accellera standards are transferred to the IEEE Standards Association for formalization and ongoing change control.

Accellera Systems Initiative: A New Synergy for Standards

System, software, and semiconductor design are converging to meet the increasing challenges to create complex integrated circuits and systems on chips. This convergence has brought to the forefront the need for a single organization to facilitate the creation of system-level, semiconductor design and verification standards. Accellera addresses the needs of the system and semiconductor designers who must find new and smarter ways to create and produce increasingly complex chips. The organization is creating more comprehensive standards that benefit the global electronic design community.

Membership

Accellera's members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera and for information on how to join us, please visit our website at **www.accellera.org**.

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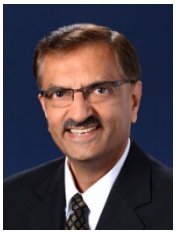

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Program-at-a-Glance – Tuesday, Oct. 14

	Ballroom Strauss A	Ballroom Strauss B	Salon Bialas	Salon Studer
9:00 – 9:20	**Welcome & Overview** (Ballroom Strauss A+B)			
9:30 – 11:00	T1 European SystemC User Group Meeting • SystemC Update • UVM-SystemC • Virtual Platforms for Automotive	T2a Advanced UVM (1/2) • Demystifying the UVM Configuration • Database - Behind the Scenes of the UVM Factory	T3 An Introduction to using Event-B for Cyber-Physical System Specification and Design	T4a Enabling Energy Aware System Level Design with UPF-Based System Level Power Models (1/2)
11:00 – 11:30	**Coffee Break & Exhibition** (Foyer Strauss & Corridor)			
11:30 – 13:00	T5 Virtual Prototyping using SystemC TLM-2.0	T2b Advanced UVM (2/2) • Architecting Effective UVM Stimulus & Sequence Hierarchies • Advanced UVM Register Modeling & Performance	T6 Requirements-driven Verification Methodology for Standards Compliance	T4b Enabling Energy Aware System Level Design with UPF-Based System Level Power Models (2/2)
13:00 – 14:00	**Lunch & Exhibition** (Foyer Strauss & Corridor)			
14:00 – 15:30	T7 Easier UVM – Making Verification Methodology more Productive **DOULOS**	T8 The How To's of Metric Driven Verification to Maximize Verification Productivity **CADENCE**	T9 Creating Portable Tests with a Graph-Based Test Specification **MENTOR GRAPHICS**	T10 Attack Your SoC Power Challenges with Virtual Prototyping **SYNOPSYS**
15:30 – 16:00	**Coffee Break & Exhibition** (Foyer Strauss & Corridor)			
16:00 – 17:30	T11 Algorithm Verification with Open Source and SystemVerilog **AMIQ CONSULTING**	T12 Revolutionary Debug Techniques to Improve Verification Productivity **CADENCE**	T13 Architecting your UVM Testbench for Simulation/ Acceleration Reuse to enable Block to System Verification Productivity **MENTOR GRAPHICS**	T14 Extending Proven Digital Verification Techniques for Mixed-Signal SoCs with VCS AMS **SYNOPSYS**
17:30 – 19:00	**Exhibition** (Foyer Strauss & Corridor)			
19:00 – 20:00	**DVConnect Networking Reception & Exhibition** (Foyer Strauss & Corridor)			
20:00 – 22:30	**Accellera Dinner** (Ballroom Strauss A+B)			

Tutorial Overview

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2014 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

Tuesday, October 14

Tutorial T1: European SystemC User Group Meeting

Ballroom Strauss A **9:30-11:00**

Part 1: SystemC Standards Update

SystemC has become the industry standard language to model Virtual Platforms. This tutorial will start with a SystemC update and overview about recent standardization activities from the different Accellera Working Groups, giving a condensed overview about status and plans around SystemC.

Presenters:

Trevor Wieman, *Intel Corporation*, United States

Philipp Hartmann, *OFFIS*, Germany

Part 2: UVM-SystemC Application in the Real World

This presentation introduces the Universal Verification Methodology (UVM) built in SystemC/C++ (UVM-SystemC) to advance current system-level verification practices. UVM-SystemC enables the creation of a structured, modular, configurable and reusable testbench environment. Unlike other initiatives to create UVM in SystemC, the presented proof-of-concept class library uses identical constructs as defined in the UVM standard for test and sequence creation, verification component and testbench configuration and execution by means of simulation. In a nutshell, the talk describes the concepts of UVM-SystemC and shows how they can be applied to real-world designs from the digital and mixed-signal domains.

Presenters:

Stephan Schulz, **Thilo Vörtler**, *Fraunhofer IIS/EAS*, Germany

Part 3: Virtual Platforms for Automotive: Use Cases, Benefits and Challenges

Nine years after the first SystemC specification the automotive domain has discovered the world of executable HW models. Its characteristics such as long product cycles, safety critical applications and the automotive industry ecosystem offer distinctive use cases but also implicate distinctive challenges. Both aspects are addressed in this contribution. However it is not confined to the point of view of HW developers, but aims for including the view of embedded SW developers and system integrators.

Presenter:

Angela Kramer, *Robert Bosch GmbH*, Germany

Tuesday, October 14

Tutorial T2: Advanced UVM

Ballroom Strauss B **Part A: 9:30 – 11:00, Part B: 11:30 – 13:00**

This tutorial provides intermediate and advanced users of the Universal Verification Methodology (UVM) with some more in-depth material on key topics which will help take their understanding and effectiveness to the next level. It is aimed at engineers with a good understanding of SystemVerilog and either OVM or UVM and with some practical experience. UVM beginners may also find the content interesting although the details could be somewhat overwhelming; at any rate, it should raise awareness and provide some good reference material for the future.

After a very brief introduction to UVM in order set the scene, the tutorial takes a more detailed look at four topics that have been selected based on Verilab's combined experience of interacting with engineers and implementing pragmatic UVM solutions on many projects at different clients:

- Demystifying the UVM Configuration Database
- Behind the Scenes of the UVM Factory
- Effective Stimulus & Sequence Hierarchies
- Advanced UVM Register Modeling & Performance

A deeper understanding of these key aspects of UVM provides the verification engineer with the leverage necessary to go beyond the beginner level and excel at applying UVM concepts to a wide variety of applications. By delving into base-class code and concepts we demonstrate how cool UVM is and replace some of the awe with a pragmatic appreciation of what is going on behind the scenes.

Presenters:

Mark Litterick, *Verilab,* Germany

Jason Sprott, *Verilab,* United Kingdom

Jonathan Bromley, *Verilab,* United Kingdom

Vanessa Cooper, *Verilab,* United States

Tuesday, October 14

Tutorial T3: An Introduction to using Event-B for Cyber-Physical System Specification and Design

Salon Bialas **9:30 – 11:00**

Cyber-physical systems (CPS) are integrations of computing and physical mechanisms engineered to provide physical services including transportation, energy distribution, manufacturing, medical care and management of critical infrastructure. CPS present significant challenges for systems modelling and verification. Event-B is a proof-based modelling language and method that enables the systematic development of specifications using a formal notion of refinement. The Rodin platform is the Eclipse-based IDE that provides automated support for Event-B model-based development, refinement and mathematical proof. The Event-B formal modelling and verification method and the associated open source Rodin toolset integrates powerful automated proof and model checking capabilities and has a large user base of more than twenty industrial organisations.

In this tutorial, we present a methodical approach to CPS development with Event-B which allows the notions of synchronisation and communication to be introduced in a lightweight manner at the specification level so that it is feasible to begin hybrid, continuous/discrete co-simulation at an early stage of CPS development. The CPS model is further refined to a fully timed, component-based architectural representation, from which a concrete, synchronous, cycle-accurate model of the system controller and suite of assertions can be derived and mapped directly to a software or hardware implementation (e.g., VHDL, SystemVerilog, C).

This work is funded by the FP7 project ADVANCE (287563), Advanced Design and Verification Environment for Cyber-Physical System Engineering (**www.advance-ict.eu**).

Presenters:

John Colley, *University of Southampton*, United Kingdom

Michael Butler, *University of Southampton*, United Kingdom

Tuesday, October 14

Tutorial T4: Enabling Energy-Aware System Level Design with UPF-Based System Level Power Models

Salon Studer **Part A: 9:30 – 11:00, Part B: 11:30 – 13:00**

Power has become a primary concern in electronic systems design, on par with functionality and performance. Minimizing power consumption and heat generation while maximizing battery life and system lifetime is essential in today's systems. Modeling power consumption for typical system usage scenarios early in the design process enables architectural tradeoffs that can have a very large impact on total power consumption, including the tailoring of firmware to make the most effective use of power management features of the hardware. Specification of power intent for the power management of low power systems has been addressed by the IEEE 1801 Unified Power Format (UPF) standard, but no standards have been developed yet for system level power modeling. This tutorial will provide an overview of system level power modeling goals, approaches, and challenges, together with a summary of ongoing work in the IEEE 1801 UPF working group to extend UPF hierarchical power state modeling capabilities to support system level power modeling and architectural power intent specifications.

Several challenges need to be addressed to produce a useful system level power model. Composition of the hardware/software/system must be modeled with an appropriate balance between abstraction and detail to enable efficient yet accurate application.

UPF today is defined to apply to design hierarchies defined in SystemVerilog or VHDL. To support system level power modeling, extensions to apply to SystemC or to a more abstract model of the system hierarchy may be appropriate. UPF power states could then be attributed with power consumption formulae to support power-state-based computation of system power consumption across the design hierarchy. The IEEE 1801 WG is currently working on defining such extensions to enable system level power modeling based on UPF.

Presenters:

Ellie Burns, *Mentor Graphics*, United States
Alan Gibbons, *Synopsys*, United Kingdom
Richard Scales, *Intel*, France
Josefina Hobbs, *Synopsys*, United States
John Biggs, *ARM*, United Kingdom
Erich Marschner, *Mentor Graphics*, United States

Tuesday, October 14

Tutorial T5: Virtual Prototyping using SystemC TLM-2.0

Ballroom Strauss A **11:30 – 13:00**

This tutorial will start with a short review of SystemC, particularly with respect to its status and adoption across the industry, and will then describe how the SystemC TLM-2.0 standard is being used to enable software virtual prototyping for the purposes of architectural performance modeling and software development.

It is now six years since the first release of the TLM-2.0 standard back in 2008. Since that time, we've discovered that TLM-2.0 actually works! There are now many examples of the TLM-2.0 standard being used to create virtual platforms at both the loosely-timed and approximately-timed levels, and to support model interoperability at the transaction-level. The most advanced features of TLM-2.0 are being exploited to fine-tune the trade-off between model execution speed and accuracy. The SystemC TLM-2.0 standard has even inspired certain features of UVM, the Universal Verification Methodology for SystemVerilog, where it is used in the context of passing transactions between SystemVerilog and SystemC.

The main focus of this tutorial will be to explain some of the central ideas of the TLM-2.0 standard and to emphasize the benefits that TLM-2.0 brings for creators and users of virtual prototypes. This tutorial will be of interest to engineers who want a technical overview of TLM-2.0 and to managers who want an appreciation of its significance in the market.

Presenter:

John Aynsley, *Doulos*, United Kingdom

Tuesday, October 14

Tutorial T6: Requirements-driven Verification Methodology for Standards Compliance

Salon Bialas **11:30 – 13:00**

Requirements-driven verification is based on ensuring that feature-level requirements are adequately verified by tracing such requirements through to verification tasks. It is similar to Coverage-driven Verification from the sense that it is metric-driven but differs significantly because the metrics derive from requirements rather than verification goals. Requirements-driven verification is also required for compliance with the increasing number of standards that control development of hardware for domains such as automotive (ISO26262) and avionics (DO254).

The tutorial will cover what the development standards mandate in development and how it can be delivered through requirements-driven verification methodology:

- Requirements engineering
- Requirements at a hierarchical level
- Requirements of good quality
- Requirements mapping
- No loss, incorrect translation or loss of context through the Requirements tree
- Requirements need to be proven to be implemented and working

The tutorial will use an automotive example (lane crossing) to cover the three main issues regarding standards compliance and how they are covered through a requirements-driven verification methodology.

Attendees of the tutorial will learn how to apply a requirements-driven verification methodology and how that can be used to ensure compliance to hardware development standards such as ISO26262 and DO254. Tooling will be considered from a supporting perspective but the main topic will be methodology and compliance.

Presenters:

Mike Bartley, *Test and Verification Solutions*, United Kingdom

Serrie Chapman, *Test and Verification Solutions*, United Kingdom

Tutorial Sponsored By:

Tutorial T7: Easier UVM – Making Verification Methodology More Productive

Ballroom Strauss A **14:00 – 15:30**

This tutorial gives a short introduction to UVM, the Universal Verification Methodology for SystemVerilog. UVM is introduced by taking advantage of *Easier UVM*, a set of coding guidelines and a code generator that creates UVM code compliant to those guidelines. *Easier UVM* is an effective way of learning and adopting UVM, and furthermore the *Easier UVM* guidelines and code generator are freely available for use after the tutorial. *Easier UVM* was created to help individuals and project teams learn and then become productive with UVM as quickly as possible.

This tutorial is suitable for total beginners and for people with some experience of UVM. To get the most from this tutorial, attendees should have some familiarity with SystemVerilog.

In this tutorial we will start by introducing UVM and explaining its background and motivation. We will then briefly introduce the main technical features of UVM one-by-one, showing detailed code examples. The focus will be on the big picture and the overall organisation of the UVM verification environment. We will explain the prescriptive approach taken by the *Easier UVM* guidelines for the use of SystemVerilog interfaces, UVM agents, sequences, virtual sequences, scoreboards, and tests, putting a particular emphasis on the need to consider verification component reuse at every stage. We explain how to make proper use of the configuration database by using configuration objects in a disciplined way, which means having one configuration object per component and passing configuration information strictly down the hierarchy from parent to child.

Presenter:

John Aynsley, *Doulos*, United Kingdom

Tuesday, October 14

Tutorial T8: The How To's of Metric Driven Verification to Maximize Verification Productivity

Tutorial Sponsored By:

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Ballroom Strauss B **14:00 – 15:30**

Metric Driven Verification (MDV) is a productivity enhancement over the tried and true coverage driven verification, for purposes of functional verification of RTL designs. MDV is used by a majority of chip suppliers, but often only for specific parts of a chip, in a somewhat limited way, and mostly in the context of simulation-only environments. Metrics is the language of functional verification, applicable at any stage of a design. Metrics can be used on the variety of verification engines necessary today to achieve improved verification productivity. So while MDV is highly codified and repeatable with simulation engines and the variety of coverage metrics used at the IP level, how does this extend to formal and acceleration engines, and from IP level to subsystem and full SOC level verification?

Cadence has matured and extended the MDV Methodology it pioneered in 2004 to address the new challenges and issues discussed above. The methodology and approach is tool independent, and will have significance no matter which vendor's tools you are using, as the concepts and strategies are universally applicable.

The scope of this MDV tutorial is ambitious and vast. It will present and demonstrate the major factors of functional verification, from IP level to SOC level, from simulation to acceleration, from practical methodology guidelines at different stages of integration, to human and tool factors essential to be managed.

Presenters:

John Brennan, *Cadence*, United States

Matt Graham, *Cadence*, Canada

Tuesday, October 14

Tutorial T9: Creating Portable Tests with a Graph-Based Test Specification

Tutorial Sponsored By:

Mentor Graphics

Salon Bialas **14:00 – 15:30**

There is a growing emphasis on SoC- and system-level testing as the number of processor cores in designs increases. Verification using high-level verification languages (HVLs), such as SystemVerilog, in simulation is still critical at the block level. However, verification must now extend to drive embedded software running on the processor cores, and run in simulation, emulation, FPGA prototypes, and even first silicon.

System level verification engineers do not enjoy the benefits of a standardized testbench language such as SystemVerilog, nor a standard class library methodology such as UVM. Unlike their IP block level verification engineering counterparts, system level verification engineers are left to a variety of languages and methodologies.

This tutorial will provide an overview of a graph-based test description language that raises the level of verification abstraction to address system level challenges. While random testing techniques break down, and directed testing techniques remain manual, a graph-based test specification solves the system level verification challenge. It raises the level of abstraction in describing both system level stimulus and verification goals (metrics), while not restricting system level verification teams to a pre-determined language or methodology.

Among other benefits, using a graph-based approach enables the highest degree of verification re-use, from IP block to sub-system to full-system level verification. It supports verification in SystemVerilog, Verilog, VHDL, C, C/C++, assembly, and even other non-traditional base languages. And it also can be extended from simulation to emulation to FPGA prototyping, and even silicon validation.

This tutorial will provide an introduction to the stimulus and metrics description and will also show how it enables these benefits and more.

Presenters:

Mark Olen, *Mentor Graphics*, United States

Matthew Ballance, *Mentor Graphics*, United States

Rebecca Granquist, *Mentor Graphics*, United States

Tuesday, October 14

Tutorial T10: Attack Your SoC Power Challenges with Virtual Prototyping

Tutorial Sponsored By:

SYNOPSYS®

Salon Studer **14:00 – 15:30**

High-end application like wireless communications, multi-media, networking, or the emerging micro-server/data-center market are posing enormous challenges on the SoC design to meet performance, power, and cost requirements. For the SoC architect, it is crucial to understand how design decisions impact power and performance of their SoC architecture in the face of complex and dynamic application workloads. Hardware-software partitioning, power domain definition, and dynamic voltage and frequency scaling cannot be determined in isolation.

In this session we will introduce how virtual prototypes enable early quantitative analysis of power and performance trade-offs to determine the right SoC architecture. We will highlight how Synopsys Platform Architect and application workload modeling are used to make power-aware architecture design decisions long before software is available, including:

- How to partition the SoC application into fixed hardware accelerators and software executing on processors, determining the optimal number and type of each CPU, GPU, DSP and accelerator
- How to partition SoC components into a set of power domains to adjust voltage and frequency at runtime in order to save power when components are not needed
- How to confirm the expected performance/power curve for the optimal architecture

Illustrations will be provided from real-life case-studies and application examples.

Presenter:

Stefan Thiel, *Synopsys*, Germany

Tuesday, October 14

Tutorial Sponsored By:

Tutorial T11: Algorithm Verification with Open Source and SystemVerilog

Ballroom Strauss A **16:00 – 17:30**

The verification of algorithmic intensive designs, for example digital signal processing cores or encryption units, requires complex mathematical models. Implementation and validation of mathematical golden models using existing verification languages can be very complicated as they are not optimized for mathematical functions and algorithms. Coding even simple algorithms can be a nightmare, the resulting models need thorough validation and most probably will not provide the desired simulation performance.

We can use numerical computing languages and tools like GNU Octave, Matlab or Mathematica to code mathematical models in order to dramatically speed up the verification environment development and reduce the risk of algorithm implementation bugs, as well as increase the simulation performance.

This tutorial is intended for verification engineers that must validate algorithmic designs. It presents the detailed steps for implementing a SystemVerilog verification environment that interfaces with a GNU Octave mathematical model. It describes the SystemVerilog – C++ communication layer with its challenges, such as proper creation and activation or piped algorithm synchronization handling. The implementation is illustrated for NCsim, VCS and Questa. This tutorial leads you through the detailed steps of setting up the environment and writing code for algorithm verification using GNU Octave and SystemVerilog:

- About the functional verification of a numerical algorithm
- Overview of SystemVerilog, UVM, Octave and DPI
- DUT: Keccak-SHA-3 cryptographic hash function
- Verification environment architecture
- Octave Installation
- Keccak-SHA-3 implementation in Octave
- Interface between SystemVerilog – Octave C/C++ using DPI-C
- The Octave shared library
- Assemble the pieces
- Running simulations and regressions

Presenters:

Daniel Ciupitu, *AMIQ Consulting*, Romania

Andra Socianu, *AMIQ Consulting*, Romania

Tuesday, October 14

Tutorial T12: Revolutionary Debug Techniques to Improve Verification Productivity

Tutorial Sponsored By:

cadence®

Ballroom Strauss B **16:00 – 17:30**

Still debugging using older conventional methods such as printf? Traditional post-process debug techniques can be valuable; however, many limitations, such as those related to performance or a lack of interactive features like source-level stepping, make debugging difficult. Cadence has integrated the best of both worlds: post-process and interactive debug capabilities in a novel multi-language, "interactive" post-process debug solution that can help you fix bugs in minutes instead of hours or days.

So, what's this "interactive" post process debug stuff anyways? It can easily be defined as a combination of interactive and post-process debug integrated into a single debug environment. The designer and/or the verification engineer needs to run their simulation only once after the bug has been detected. The secondary run records all needed debug data needed for the user to isolate the bug. No need to run multiple sets of simulations to find the bug… *A significant savings in debug time*!

What you will learn:

- Advantages of the new "interactive" post-process debug technique over the traditionally separate interactive and post-process debug modes that can improve overall debug productivity by 40 – 50%
- Unique advantages of using SimVision for debug of class-based environments, including UVM debug

Who should attend:

- Verification engineers/leads, designers, and managers who recognize that debug is taking an increasingly larger share of the overall design time and are interested in improving overall debug productivity and predictability
- Design and verification engineers looking to increase their knowledge of class-based debug capabilities

Presenter:

Nadav Chazan, *Cadence Design Systems*, Israel

Tuesday, October 14

Tutorial T13: Architecting SystemVerilog UVM Testbenches for Simulation and Emulation Reuse to Boost Block-to-System Verification Productivity

Tutorial Sponsored By:

Salon Bialas **16:00 – 17:30**

When adopting hardware emulation to boost SystemVerilog testbench performance and improve verification productivity, it is highly desirable that the paradigm of reuse underlying UVM works effectively in the context of emulation to continue to reap the reuse benefits as one moves from block to sub-system and system level.

This tutorial lays out a methodology for developing emulation-ready UVM testbenches with the following fundamental principles:

- **Interoperability**: The ability to run the same testbench interchangeably in both pure simulation and emulation; the proposed methodology encompasses a unified codebase and flow portable between emulation and conventional simulation.
- **Flexibility**: Among the key benefits of SystemVerilog for verification, and at the heart of UVM, is the object-oriented modeling paradigm for the creation of dynamic, reusable, hierarchical verification components and testbenches; the proposed methodology continues to provide these modeling benefits of SystemVerilog and UVM.
- **Performance**: The assurance to get optimal emulation performance without hampering simulation performance; the proposed methodology justifies adoption by the possible acceleration gains, mounting to several orders of magnitude speed-up.

The methodology presented enables vertical reuse in practice, from block-level towards UVM-based system-level verification. Smaller block and chip-level tests can continue to be run on a software simulator while the longer tests and system-level tests can now be run much faster using an emulator within the same unified UVM framework. Furthermore, coverage metrics from tests run in both simulation and emulation can be combined to ensure unified coverage closure before design tape-out. The advantages are evident in terms of performance, completeness of the verification process, and significantly reduced engineering time to build and maintain an emulation-ready verification environment and infrastructure.

Presenters:

Hans van der Schoot, *Mentor Graphics*, United States

Ellie Burns, *Mentor Graphics*, United States

Tuesday, October 14

Tutorial T14: Extending Proven Digital Verification Techniques for Mixed-Signal SoCs with VCS AMS

Tutorial Sponsored By:

SYNOPSYS®

Salon Studer **16:00 – 17:30**

The growth in mixed-signal System-on-Chip (SoC) designs is driven by many factors including cost, performance and power consumption. To deal with these constraints, a mixed-signal verification solution must offer not only performance and flexibility but also superior verification techniques with methodologies. By coupling industry-best performance engines with native integration of advanced technologies for functional and low-power verification, Synopsys VCS AMS offers a unique mixed-signal verification solution for complex mixed-signal SoCs.

This highly technical tutorial presents how the VCS AMS mixed-signal verification solution provides superior performance and flexibility. It was developed around best-in-class methodologies to extend proven digital verification techniques into mixed-signal designs, thus the VCS-AMS users experience a paradigm shift in verification. The solution encompasses, but is not restricted to, capabilities for time efficient simulations using "Save and Restore" technology, aligned with the SV1800 industry standard syntax for "SystemVerilog nettype" constructs, represented as a holistic methodology within AMS Testbench that is underpinned by extremely successful UVM library.

The breadth and depth of usage of the individual portions within the solution are explained by real user case studies: extensive usage of VCS AMS Save and Restore for boosting productivity by STMicroelectronics and performance driven VCS AMS behavioral modeling flow by Micronas.

Presenters:

Helene Thibieroz, *Synopsys*, United States

Adiel Khan, *Synopsys*, United Kingdom

Pierluigi Daglio, *STMicroelectronics*, Italy

Gernot Koch, *Micronas*, Germany

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DVConnect Networking Reception

One of the main reasons to come to **DVCon Europe** is to start networking with your peers!

The DVConnect Networking Reception gives you a venue to get connected with design and verification experts and to grow your professional network!

Sponsored by:

OneSpin Solutions

Date, Time & Location:

Tuesday, October 14, 19:00 – 20:00, Foyer Strauss & Corridor

Accellera Systems Initiative Dinner

Join us for the Accellera Dinner, a unique networking event to interact with industry professionals to exchange know-how and learn how other companies tackle their design and verification challenges. The main theme during the dinner evening is:

Sponsored by:

accellera SYSTEMS INITIATIVE™

Promoting European EDA Standardization Together with Accellera

During a tasteful 3-course dinner, short industry stories will be presented that explain the reasoning behind the creation of new EDA standards for design and verification and the role of Accellera Systems Initiative to assist in further developing and deploying these standards.

Date, Time & Location:

Tuesday, October 14, 20:00 – 22:30
Ballroom Strauss A + B

Note: Registration closes on **October 3**;
On-site registration for the dinner is not possible

Program-at-a-Glance – Wednesday, Oct. 15

	Ballroom Strauss A	Ballroom Strauss B	Salon Bialas + Studer
9:00 – 9:50	**Keynote** (Ballroom Strauss A+B)		
10:00 – 11:00	Analog/Mixed-Signal Design & Verification - 1 T 1.1, T 1.2	Advanced Verification - 1 T 2.1, T 2.2	IP Reuse & Design Automation - 1 T 3.1, T 3.2
11:00 – 11:30	**Coffee Break & Exhibition** (Foyer Strauss & Corridor)		
11:30 – 12:30	Analog/Mixed-Signal Design & Verification - 2 T 1.3, T 1.4	Advanced Verification - 2 T 2.3, T 2.4	IP Reuse & Design Automation - 2 T 3.3, T 3.4
12:30 – 14:00	**Lunch & Exhibition** (Foyer Strauss & Corridor)		**Poster Session** (Bialas + Studer) 12:45 – 13:45
14:00 – 15:30	System Level Design & Verification - 1 T 4.1, T 4.2, T 4.3	Advanced Verification - 3 T 5.1, T 5.2, T 5.3	Low-Power Methodologies T 6.1, T 6.2, T 6.3
15:30 – 16:00	**Coffee Break & Exhibition** (Foyer Strauss & Corridor)		
16:00 – 17:00	System Level Design & Verification - 2 T 4.4, T 4.5	Advanced Verification - 4 T 5.4, T 5.5	Verification Management T 7.1, T 7.2
17:10 – 17:30	**Closure and Best Paper & Poster Award** (Ballroom Strauss A+B)		
17:30	***End of Conference***		

Keynote Speaker

Bernd Adler

Wireless CTO & Div. Vice President
Platform Engineering Group
Intel Mobile Communications

Tomorrow's Smart Mobile Systems - by the Power of Ten

The development of advanced mobile communication and multimedia devices face unprecedented challenges. "Internet of Things", "Smart Everything", or "Everything connected" are the new buzzwords characterizing future applications. Their cornerstone will be highly integrated System-on-Chip (SoC) solutions offering a wide range of features at lowest costs and minimal energy consumption. These advanced SoCs cannot be mastered without an end-to-end optimization of the entire development process with improved EDA standards, methodologies and tools. Advanced system features result in a skyrocketing complexity of firmware and software. At the same time, the innovation cycles are constantly shrinking. These contradicting requirements can only be reconciled through a dramatically increased development efficiency.

Today's system and software development is based on virtual prototyping, enabling early feature development where hardware and software can evolve together, including investigations on different system architectures. In addition, silicon, package and printed circuit board need to be developed concurrently to meet the requirements of simultaneously active communication technologies, without sacrificing an optimum system cost position. The final system integration and verification is not possible without extremely high technical expertise and a close collaboration across the entire system.

This keynote will cover: 1) the change in system properties, 2) the evolution in product development and their challenges, and 3) the requirements for the next generation EDA standards, tools and solutions.

Biography

Bernd Adler has held the position of RF Chief Scientist and Head of Wireless System Engineering at Intel Mobile Communications Group Wireless System Engineering activities engineering, line management, product management and site management positions at Infineon Technologies for over 12 years working on cellular transceivers for CDMA, WCDMA, WIMAX and LTE as well as 2G monolithic integration activities paving the way to ultra low cost products. Before this he held RF engineering positions working on modules and oscillators for Base stations. He received his diploma (electrical engineering) in 1989.

Technical Sessions Overview

Presentations, 10:00 – 11:00

Session T1: Analog/Mixed-Signal Design and Verification – 1

Session T2: Advanced Verification – 1

Session T3: IP Reuse & Design Automation – 1

Presentations, 11:30 – 12:30

Session T1: Analog/Mixed-Signal Design and Verification – 2

Session T2: Advanced Verification – 2

Session T3: IP Reuse & Design Automation – 2

Presentations, 14:00 – 15:30

Session T4: System Level Design & Verification – 1

Session T5: Advanced Verification – 3

Session T6: Low Power Methodologies

Presentations, 16:00 – 17:00

Session T4: System Level Design & Verification – 2

Session T5: Advanced Verification – 4

Session T7: Verification Management

Poster Session, 12:45 – 13:45

Topic areas:

Analog/Mixed-Signal Design and Verification

System Level Design & Verification

Advanced Verification

Low Power Methodologies

Verification Management

Wednesday, October 15

Session T1: Analog/Mixed-Signal Design and Verification – 1

Ballroom Strauss A **10:00 – 11:00**

Chair: **Frans Theeuwen** – *NXP Semiconductors*

T1.1 **Accelerated SOC Verification Using UVM Methodology for a Mix-signal Low Power Design**
Giuseppe Scata, Ashwini Padoor – *Texas Instruments*
Vladimir Milosevic – *ELSYS Eastern Europe*

T1.2 **A Framework for AMS Verification IP Development with SystemVerilog, UVM and Verilog-AMS**
Jeganath Gandhi Rajamohan, **Mike Bartley** – *Test and Verification Solutions*

Session T2: Advanced Verification – 1

Ballroom Strauss B **10:00 – 11:00**

Chair: **Matthias Bauer** – *Infineon Technologies*

T2.1 **Implementation of a Closed Loop CDC Verification Methodology**
Andrew Cunningham, Ireneusz Sobanski – *Intel*

T2.2 **A Pragmatic Approach to Meta-Stability Aware Simulation**
Joseph Bulone – *Kalray*
Roger Sabbagh – *Mentor Graphics*

Session T3: IP Reuse & Design Automation – 1

Bialas + Studer **10:00 – 11:00**

Chair: **Christian Sauer** – *Cadence Design Systems*

T3.1 **A Meta-Modeling-Based Approach for Automatic Generation of Fault-Injection Processes**
Bogdan-Andrei Tabacaru, Moomen Chaari, Wolfgang Ecker – *Infineon Technologies and Technische Universität München*
Thomas Kruse – *Infineon Technologies*

T3.2 **A Methodology for Vertical Reuse of Functional Verification from Subsystem to SoC level with Seamless SoC Emulation Testing**
Pranav Kumar, Digvijay Pratap Singh – *STMicroelectronics*
Ankur Jain – *Mentor Graphics*

Wednesday, October 15

Session T1: Analog/Mixed-Signal Design and Verification – 2

Ballroom Strauss A **11:30 – 12:30**

Chair: **Frans Theeuwen** – *NXP Semiconductors*

T1.3 **UVM Ready: Transitioning Mixed-Signal Verification Environments to Universal Verification Methodology**
Arthur Freitas, Regis Santonja – *Freescale Semiconductor*

T1.4 **NVVM: A Netlist-Based Verilog Verification Methodology for Mixed-Signal Design**
Jiping Qiu, Kurt Schwartz – *Texas Instruments*

Session T2: Advanced Verification – 2

Ballroom Strauss B **11:30 – 12:30**

Chair: **Clemens Roettgermann** – *Freescale Semiconductor*

T2.3 **The Universal Translator - A Fundamental UVM Component for Networking Protocols**
David Cornfield – *AppliedMicro*

T2.4 **Practical Experience in Automatic Functional Coverage Convergence and Reusable Collection Infrastructure in UVM Verification**
Roman Wang – *Advanced Micro Devices*
Mike Bartley, Suresh Babu – *Test and Verification Solutions*

Session T3: IP Reuse & Design Automation – 2

Bialas + Studer **11:30 – 12:30**

Chair: **Christian Sauer** – *Cadence Design Systems*

T3.3 **A Real World Application of IP-XACT for IP Packaging – Bridging the Usability Gap**
Philip Todd – *Dialog Semiconductor*

T3.4 **Generation of UVM Compliant Test Benches for Automotive Systems Using IP-XACT with UVM-SystemC and SystemC AMS Extensions**
Ronan Lucas, Emmanuel Vaumorin – *Magillem*
Philippe Cuenot – *Continental*
Yao Li, Zhi Wang, Marie-Minerve Louërat, Jean-Paul Chaput, François Pecheux, Ramy Iskander – *Université Pierre et Marie Currie / LIP6*
Martin Barnasconi – *NXP Semiconductors*
Thilo Vörtler and Karsten Einwich – *Fraunhofer IIS/EAS*

Wednesday, October 15

Session T4: System Level Design & Verification – 1

Ballroom Strauss A **14:00 – 15:30**

Chair: **Oliver Bell** – *Intel*

T4.1 **VP Performance Optimization**
Rocco Jonack, Juan Lara Ambel – *Intel*

T4.2 **Simulation and Debug of Mixed Signal Virtual Platforms Enabling Hardware-Software Co-Development**
Vincent Motel, Alexandre Roybier, Serge Imbert – *Cadence Design Systems*

T4.3 **UVM-SystemC based Hardware in the Loop Simulations for Accelerated Co-Verification**
Paul Ehrlich, Thilo Vörtler – *Fraunhofer IIS/EAS*
Thang Nguyen – *Infineon Technologies*

Session T5: Advanced Verification – 3

Ballroom Strauss B **14:00 – 15:30**

Chair: **Mike Bartley** – *Test and Verification Solutions*

T5.1 **The Top Most SystemVerilog and UVM Constrained Random Gotchas**
Ahmed Yehia, **Gabriel Chidolue** – *Mentor Graphics*

T5.2 **Versatile UVM Scoreboarding**
Jacob Sander Andersen, Peter Jensen, Kevin Steffensen – *Syosil*

T5.3 **Reboot your Reset Methodology: Resetting Anytime with the UVM Reset Package**
Courtney Schmitt – *Analog Devices*
Phu Huynh, Stephanie McInnis, **Uwe Simm** – *Cadence Design Systems*

Session T6: Low Power Methodologies

Bialas + Studer **14:00 – 15:30**

Chair: **Laurent Maillet-Contoz** – *STMicroelectronics*

T6.1 **Combining Static and Dynamic Low Power Verification for the Power-Aware SoC Sign-off**
Himanshu Bhatt, Prashant Mallikarjun, **Adiel Khan** – *Synopsys*

T6.2 **Complex Low Power Verification Challenges in NextGen SoCs: Taming the Beast!**
Abhinav Nawal, Gaurav Jain, **Joachim Geishauser** – *Freescale Semiconductor*

T6.3 **Power Aware Models: Overcoming Barriers in Power Aware Simulation**
Mohit Jain, J.S.S.S. Bharath, Amit Singh, Vishal Bhimani – *STMicroelectronics*
Amit Srivastava, Bharti Jain – *Mentor Graphics*

Wednesday, October 15

Session T4: System Level Design & Verification – 2

Ballroom Strauss A **16:00 – 17:00**

Chair: **Philipp Hartmann –** *OFFIS*

T4.4 **CRAVE 2.0: The Next Generation Constrained Random Stimuli Generator for SystemC**
Hoang M. Le – *University of Bremen*
Rolf Drechsler – *University of Bremen and DFKI GmbH*

T4.5 **Enriching UVM in SystemC with AMS Extensions for Randomization and Coverage**
Thilo Vörtler, Karsten Einwich – *Fraunhofer IIS/EAS*
Yao Li, Zhi Wang, Marie-Minerve Louërat, Jean-Paul Chaput, François Pecheux, Ramy Iskander – *Université Pierre et Marie Currie / LIP6*
Martin Barnasconi – *NXP Semiconductors*

Session T5: Advanced Verification – 4

Ballroom Strauss B **16:00 – 17:00**

Chair: **Matthias Bauer** – *Infineon Technologies*

T5.4 **Connecting a Company's Verification Methodology to Standard Concepts of UVM**
Frank Poppen – *OFFIS*
Marco Trunzer, Jan-Hendrik Oetjens – *Robert Bosch*

T5.5 **Introduction to Next Generation Verification Language - Vlang**
Puneet Goel – *Coverify*
Sumit Adhikari – *NXP Semiconductors*

Session T7: Verification Management

Bialas + Studer **16:00 – 17:00**

Chair: **Laurent Maillet-Contoz** – *STMicroelectronics*

T7.1 **Connecting Enterprise Applications to Metric Driven Verification**
Matt Graham, **John Brennan** – *Cadence Design Systems*
Gergely Sass – *NXP Semiconductors*

T7.2 **Requirements-driven Verification Methodology (for Standards Compliance)**
Serrie Chapman, Mike Bartley – *Test and Verification Solutions*

Wednesday, October 15

Poster Session

Bialas + Studer **12:45 – 13:45**

Analog/Mixed-Signal Design & Verification

P1.1 **Power-Aware Verification in Mixed-Signal Simulation**
Atul Pandey – *Mentor Graphics*
Mattias Welponer, Gregor Kowalczyk – *Infineon Technologies*

P1.2 **With Great Power Comes Great Responsibility: A Method to Verify PMIC's Using UVM-MS**
Dor Spigel, Moshik Hershcovitch – *Microsemi*

Advanced Verification

P2.1 **A Guide to Using Continuous Integration within the Verification Environment**
Jason Sprott, André Winkelmann, Gordon McGregor – *Verilab*

P2.2 **An Effective Design and Verification Methodology for Digital PLL**
Biju Viswanathan, Rajagopal P C, Jobin Cyriac, Ramya Nair, Joseph J Vettickatt – *Network Systems and Technologies*

P2.3 **Data Path Verification on Cross-domain with Formal Scoreboard**
Liu Jun – *Intel*

P2.4 **OSVVM: Advanced Verification for VHDL**
Jim Lewis – *SynthWorks*

P2.5 **RTL2RTL Formal Equivalence: Boosting the Design Confidence**
M Achutha KiranKumar V, Aarti Gupta, Ss Bindumadhava – *Intel*

IP Reuse & Design Automation

P3.1 **Automating Netlist Modifications Required by Functional Safety**
Harald Lüpken, Dirk Hönike, Michael Rohleder – *Freescale Semiconductor*

P3.2 **Reusable Processor Verification Methodology Based on UVM**
Mustafa Khairallah – *Boost Valley*
Maged Ghoneima – *Ain Shams University Cairo*

P3.3 **Pedal Faster! Or Make Your Verification Environment More Efficient. You Choose**
Rich Edelman, Raghu Ardeishar, Rohit Jain, **Gabriel Chidolue** – *Mentor Graphics*

Wednesday, October 15

Poster Session (continued)

Bialas + Studer **12:45 – 13:45**

System Level Design & Verification

P4.1 **An Open and Fast Virtual Platform for TriCore-based SoCs Using QEMU**
Bastian Koppelmann, Bernd Messidat, Markus Becker, Christoph Kuznik – *CLAB, University of Paderborn*
Wolfgang Mueller, Christoph Scheytt, – *Heinz Nixdorf Institute, University of Paderborn*

P4.2 **Understanding the Effectiveness of your System-Level SoC Stimulus Suite**
Robert Fredieu, Andreas Meyer – *Mentor Graphics*
Alan Hunter – *ARM*

P4.3 **Hardware/Software Co-Simulation of SPI Enabled ASICs and Software Drivers for Fault Injection and Regression Tests**
Elias Kyrlies-Chrysoulidis, Thomas Guertler, Andreas Plange,
Matthias Auerswald – *Continental*
Josef Schmid – *iSyst*

P4.4 **ISO 26262: Better be Safe with Modelling and Simulation on System-Level**
Joachim Hößler – *ikv++ technologies*
Sven Johr – *TWT GmbH*
Thang Nguyen – *Infineon Technologies*
Stephan Schulz – *Fraunhofer IIS/EAS*
Gert-Jan Tromp – *Dizain-Sync*

Low Power Methodologies

P6.1 **Low Power Verification Methodology Using UPF Query Functions and Bind Checkers**
Madhur Bhargava, Durgesh Prasad – *Mentor Graphics*

Verification Management

P7.1 **Advancing Traceability and Consistency in Verification and Validation**
Walter Tibboel, Martin Barnasconi – *NXP Semiconductors*

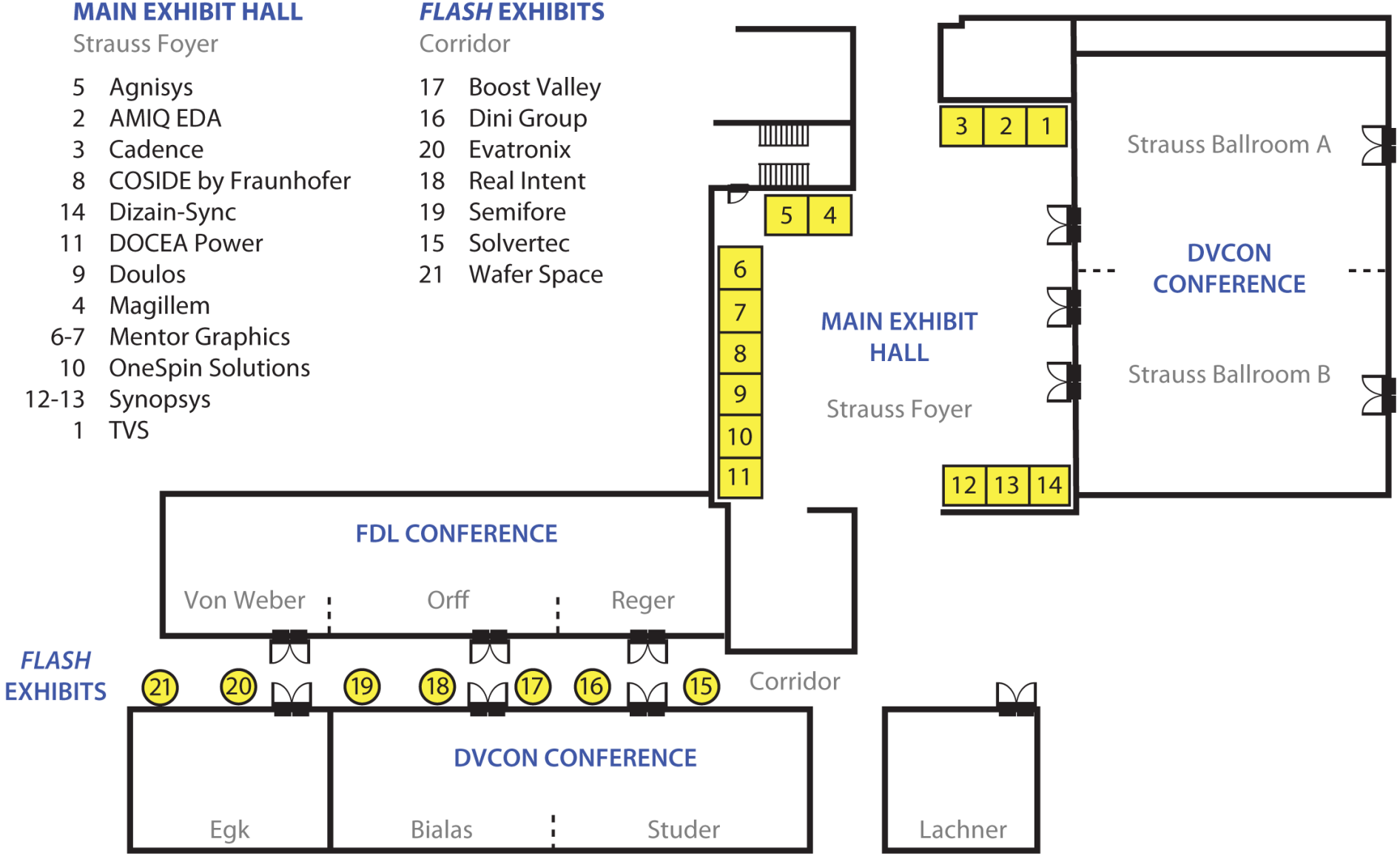
DVCon Europe Floorplan and Exhibitors List

MAIN EXHIBIT HALL
Strauss Foyer

5	Agnisys
2	AMIQ EDA
3	Cadence
8	COSIDE by Fraunhofer
14	Dizain-Sync
11	DOCEA Power
9	Doulos
4	Magillem
6-7	Mentor Graphics
10	OneSpin Solutions
12-13	Synopsys
1	TVS

FLASH EXHIBITS
Corridor

17	Boost Valley
16	Dini Group
20	Evatronix
18	Real Intent
19	Semifore
15	Solvertec
21	Wafer Space



DVCon Europe Exhibitors

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Agnisys	5
AMIQ EDA	2
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Dizain-Sync	14
DOCEA Power	11
Doulos	9
Evatronix	20
Magillem	4
Mentor Graphics	6-7
OneSpin Solutions	10
Real Intent	18
Semifore	19
Solvertec	15
Synopsys	12-13
TVS	1
Wafer Space	21

Exhibitor Listing

Agnisys

Exhibitor location #5

www.agnisys.com

Agnisys helps engineers implement semiconductor design and verification using standardized SystemVerilog and the Universal Verification Methodology – faster and with higher accuracy.

IDesignSpec can capture designs in an executable form and generate UVM, synthesizable RTL, SystemC, C Headers, IP-XACT, SystemRDL, etc.

DVinsight enables you to create SV/UVM code in a refreshingly new way. Its ability to provide visual guidance and its advance warning system makes it an indispensable companion for serious UVM code developers.

IVerifySpec is an enterprise class system that enables teams to collaborate and verify complex IP/SoCs. Historic simulation data, coupled with real-time information enables teams to get a holistic view of the verification status enabling faster verification.

Agnisys Inc. was established in 2007 in MA. Agnisys is the winner of Innovative EDA tool award at the VLSI conference. Its patented technologies have been tru sted by hundreds of users in various IP and SoC companies.

AMIQ EDA

Exhibitor location #2

www.amiq.com

AMIQ EDA provides software tools that enable design and verification engineers to increase the speed and quality of new code development, simplify legacy code maintenance, and implement best coding practices.

Its solution, **DVT Eclipse IDE** is a modern, powerful, and complete code development environment for the *e* language, SystemVerilog, Verilog, VHDL, and mixed-language projects. It integrates with all major simulators and provides UVM-oriented features that simplify verification environment creation and debugging.

Verissimo SystemVerilog Testbench Linter is a SystemVerilog coding guidelines and UVM compliance checker that enables engineers to perform an enhanced audit of their testbenches. It can be used in batch mode or integrated with DVT.

Specador Documentation Generator automatically generates accurate HTML documentation based on effective code compilation and comments analysis. It works in batch mode and uses dedicated language parsers for *e*, SystemVerilog, Verilog, and VHDL.

AMIQ EDA serves customers around the world and is recognized for its high quality solutions and customer service responsiveness.

Exhibitor Listing

Boost Valley

Flash Exhibitor location #17

www.boostvalley.com

Boost Valley is an engineering consulting company providing clients with digital design and verification services including a portfolio of verification IPs. Our goal is to establish strategic alliances designed to help deliver a client-centric, total solutions approach to solving problems, exploiting business opportunities and creating sustainable competitive advantage for our clients.

Cadence Design Systems

Exhibitor location #3

www.cadence.com

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software, hardware, IP, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at **www.cadence.com**.

COSIDE by Fraunhofer

Exhibitor location #8

www.coside.de

COSIDE® – THE DESIGN ENVIRONMENT FOR HETEROGENEOUS SYSTEMS

The design environment **COSIDE® by Fraunhofer** is the perfect tool to develop and design innovative heterogeneous hardware as well as software systems. COSIDE® is the first commercial design environment based on the SystemC and SystemC AMS standards to model and simulate highly complex analog and digital systems.

The modeling language SystemC AMS is closing the gap between the analog and digital world and between idea, concept and implementation in the design process of complex electronic systems within a heterogeneous environment. It allows a holistic design approach by considering the different worlds of development jointly.

SystemC AMS enables overall system modeling and virtual prototyping. COSIDE® is the way to benefit from it.

Exhibitor Listing

The Dini Group

Flash Exhibitor location #16

www.dinigroup.com

Located in La Jolla, California, **The Dini Group** is a professional hardware and software engineering firm, specializing in high performance digital circuit design and application development for all ASIC prototyping, High Performance Computing, Algorithmic Acceleration and Low Latency Networking projects, with emphasis on BIG FPGA boards.

Dizain-Sync

Exhibitor location #14

www.dizain-sync.com

With over 25 years of experience, **Dizain-Sync** offers a unique perspective on the combination of EDA, PLM, Design and Educational services.

Dizain-Sync is the best partner to configure the required software to the wishes of the customer and to maintain the design environment to ensure the customer can always trust on an optimal situation.

Dizain-Sync is able to advise, set up and maintain a PLM system and all other activities concerning the control of product development during the design process.

Dizain-Sync's design activities are meant to help out customers at solving complex design challenges. Dizain-Sync can provide companies with the latest technological knowledge. Dizain-Sync can also provide companies with temporary employees to help out during a design project.

Since 1988 Dizain-Sync has been offering a wide range of training classes (Verilog, VHDL, SystemC, SystemVerilog, UVM).

Exhibitor Listing

DOCEA Power

Exhibitor location #11

www.doceapower.com

DOCEA Power offers software solutions to optimize the power and thermal behavior of electronics systems (System-on-Chips, Systems-in-Package, boards or complete devices) from an architectural perspective.

Aceplorer enables power architects to model, simulate and analyze the coupled power/thermal behavior of electronics systems. Aceplorer is used by major IC and OEM design and architecture teams to provide early power estimates, secure specifications, for power budget tracking over the whole design cycle and to speed up power management verification.

The **ThermalProfiler** provides thermal experts and power architects who need to simulate more realistic (transient) worst case scenarios with a tool for fast thermal profiling. The ThermalProfiler is used to avoid over-design or thermal runaway issues by simulating the coupling between power and temperature.

Doulos

Exhibitor location #9

www.doulos.com

Doulos is the global leader for the development and delivery of world class training solutions for engineers creating the world's electronic products. Fully independent, Doulos sets the industry standard for the highest quality training programs for design and verification engineers implementing complex SoC and FPGA designs.

Doulos training programs cover the needs of hardware designers, embedded software developers and system design and verification specialists, including courses for C, C++, Embedded Linux, UML, SystemC™, Verilog®, SystemVerilog, VHDL and ARM®-based design.

For over 20 years Doulos has provided 'service through excellence', contributing to the success of nearly 3000 companies across 58 countries. The natural partner for leading tool and technology companies, Doulos schedules classes across the U.S. and Europe, as well as in India, and delivers in-house and online training programs world-wide. For more information, visit **www.doulos.com**.

Exhibitor Listing

Evatronix

Exhibitor location #20

www.evatronix.com

Evatronix SA, established in Poland in 1991, provides computer aided design and manufacturing solutions for mechanical and electronic system development. Company provides FPGA-In-the-Loop solution which incorporates hardware and software mechanisms to enable fast and efficient verification of HDL designs within the MathWorks' MATLAB®/Simulink® environment. The FIL supports design co-simulation combining HDL Verifier with a series of FPGA development boards. Evatronix offers also an Emulation Environment System, called E3, for IP verification, which provides 100% visibility of DUT registers in FPGA during the emulation process. More information about Evatronix is available at **www.evatronix.com**.

Magillem

Exhibitor location #4

www.magillem.com

Magillem provides to customers in the electronic industry tools and services that drastically reduce the global cost of complex design. Magillem has developed an easy to use, state of the art platform solution to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SoC.

Mentor Graphics

Exhibitor location #6-7

www.mentor.com

Mentor Graphics delivers the most comprehensive and unified advanced Enterprise Verification Platform available: including Questa® for high performance simulation and debug, verification management and coverage closure, low-power verification with UPF, CDC, Formal Verification, accelerated functional coverage, processor-based hardware verification and Veloce® for high-performance system verification emulation. This comprehensive solution supports OVM and UVM. For more information visit **www.mentor.com**.

Exhibitor Listing

OneSpin Solutions

Exhibitor location #10

www.onespin-solutions.com

OneSpin Solutions is a pioneer of advanced formal verification. Its award-winning technology was incubated at Infineon and has had 300 development years applied to it. OneSpin's products include easy to use, automated solutions for the early detection of design issues, comprehensive coverage-driven property analysis for rigorous testing, and high accuracy equivalency checking for large FPGAs and ASICs. Many leading electronic companies have relied on OneSpin to achieve the highest possible verification quality on hundreds of designs over the tightest schedules.

Real Intent

Flash Exhibitor location #18

www.realintent.com

Real Intent is the leading provider of EDA software to accelerate Early Functional Verification and Advanced Sign-off of digital designs. It provides comprehensive clock-domain crossing verification, advanced RTL analysis and sign-off solutions to eliminate complex failure modes of SoCs. The Meridian and Ascent product families lead the market in performance, capacity, accuracy and completeness.

Real Intent offers two product families — **Ascent** for early functional verification before simulation or synthesis; and **Meridian** for advanced sign-off verification not possible with simulation or static timing analysis.

Real Intent has sales offices in the USA and Japan, and distributors in Europe, India, Israel, Korea and Taiwan.

Semifore

Flash Exhibitor location #19

www.semifore.com

Semifore Inc., "The Addressmap Experts," provides the CSRSpec language and the CSRCompiler, a complete register design solution for hardware, software, verification, and documentation. Collaboratively manage your design from a single source specification. CSRSpec, SystemRDL, IP-XACT, or Spreadsheet inputs generate: Verilog and VHDL RTL; Verilog, or C headers; Perl, IEEE IP-XACT; SystemVerilog for UVM, VMM and OVM; HTML web pages; and Word or Framemaker documentation. Only Semifore gives your entire team a complete, correct, up-to-date register design ecosystem.

Exhibitor Listing

Solvertec

Flash Exhibitor location #15

www.solvertec.de

Solvertec enables RTL designers to identify and fix the sources of errors in complex digital chip designs with just a few clicks. Solvertec's unique EDA solution "Debug!t" integrates seamlessly into the user's existing verification flow and performs a root cause analysis of the sources of a design error. Debug!t pinpoints the RTL designer to just those lines in the HDL code where bug corrections are possible. Thus, Solvertec accelerates the process of functional verification of complex chip designs by orders of magnitude by reducing the chip design debug process from even days to minutes.

Synopsys

Exhibitor location #12-13

www.synopsys.com

Synopsys, Inc. (Nasdaq:SNPS) provides products and services that accelerate innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor intellectual property (IP), Synopsys' comprehensive, integrated portfolio of system-level, IP, implementation, verification, manufacturing, optical and field-programmable gate array (FPGA) solutions help address the key challenges designers face such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in quickly bringing the best products to market while reducing costs and schedule risk. For more than 25 years, Synopsys has been at the heart of accelerating electronics innovation with engineers around the world having used Synopsys technology to successfully design and create billions of chips and systems. The company is headquartered in Mountain View, California, and has approximately 90 offices located throughout North America, Europe, Japan, Asia and India.

Exhibitor Listing

TVS

Exhibitor location #1

testandverification.com

TVS helps companies to reduce their time-to-market and improve product quality through tailored products and services for software testing and hardware verification. Using well-defined technical and management processes executed by experts and supplemented by TVS tools, TVS is trusted by companies around the world to deliver efficient, effective solutions for both software testing and hardware verification.

With offices throughout Europe and Asia, TVS's flexible execution model delivers cost-effective resource when and where it is needed. Peter Hughes, VP Mobile Nvidia, commented, "TVS is very flexible. We've worked with the team a long time and we have the confidence they will deliver every time."

Wafer Space

Exhibitor location #21

www.waferspace.com

Wafer Space is one of the premier Product and Design Services companies which provides Semiconductor and Embedded Design Services.

With its own robust and well tested flows in Design Verification and the capability and experience to execute very complex designs from test planning through closure, Wafer Space has made a mark for itself in the semiconductor industry in less than 3 years. Wafer Space has expertise in all areas of Verification from test planning to methodologies like UVM, architecture of complex environments, Static Formal Verification, expert knowledge of High Speed Interfaces and proficiency in Low Power Verification.

A world class engineering team, intensive knowledge in Chip Design, Embedded Software and Hardware, steadfast focus on quality and the ability to execute complex turnkey projects, is what differentiates Wafer Space from its competition. Currently, Wafer Space has design centers in Bangalore, India and Hillsboro, Oregon, USA.

Best Paper and Poster Award and Form

DVCon Europe conference & exhibition attendees are entitled to vote for the "**DVCon Europe Best Paper and Poster**" awards. Please use this form, or any of the forms distributed at the conference, to share your vote:

Your Name: _____

Your Badge ID: _____

Best Paper # and Title: _____

Best Poster # and Title: _____

Please submit your vote in the "Best Paper and Poster" Box in the Foyer. The award ceremony takes place on Wednesday, October 15 at 17:10 in Ballroom Strauss A+B.

Please note the following rules and conditions:

- You cannot vote on your own or co-authored paper or poster
- You can only vote once. Multiple forms of the same attendee are excluded
- You can only vote on a paper or poster given at DVCon Europe

FDL

FDL 2014
October 14-16, 2014
Munich, Germany

General Chair:
Frank Oppenheimer, OFFIS
Program Chair:
Julio Medina, U de Cantabria

Forum on specification and Design Languages

FDL is co-located with DVCon Europe: *you can take the advantage of it and participate in FDL!*

Forum on specification & Design Languages (FDL) is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modelling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Modelling and specification concepts push the development of new design and verification methodologies to ESL (Electronic System Level) thus providing a means for model-driven and automated design of complex electronic systems in a variety of application domains.

Main Conference Sessions

- Natural Language Processing for Requirements Formalization
- Requirements
- Predictability
- SystemC Modelling and Simulation
- Parallel Simulation and Verification
- Parallel Architectures
- Formal Models & Verification
- Power
- UVM in AMS Verification tutorial
- Future Challenges in the AMS Domain

Complete FDL Program: www.ecsi.org/fdl

Exhibiting Companies

2015 DESIGN AND VERIFICATION™

DVCON

CONFERENCE AND EXHIBITION

UNITED STATES

PREMIER CONFERENCE FOR DESIGN & VERIFICATION ENGINEERS

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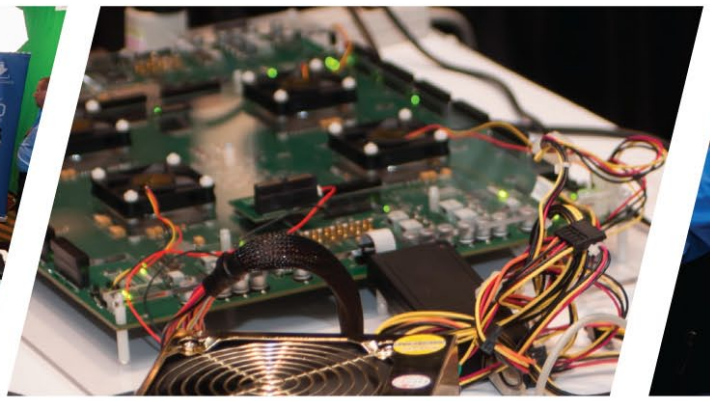

DVCon Conference Dates:

MARCH 2 - 5, 2015

Monday	Tuesday	Wednesday	Thursday
• Tutorials • Exhibits	• Technical Sessions • Keynote Speaker • Exhibits	• Technical Sessions • Panel Discussions • Exhibits	• Tutorials

DVCon Exhibition Dates:

MARCH 2 - 4, 2015

Monday.....5:00 - 7:00pm
Tuesday.....2:30 - 6:00pm
Wednesday...2:30 - 6:00pm

Doubletree, San Jose, CA

WHY ATTEND?

- DVCon continues to be the premier conference for design and verification engineers of all experience levels.
- Compared to larger and more general conferences, DVCon affords attendees a concentrated menu of technical sessions—tutorials, papers, poster sessions and panels—focused on design and verification hot topics.
- In addition to participation in high quality technical sessions, DVCon attendees have the opportunity to take part in the many informal, but often intense, technical discussions that pop-up around the conference venue among 800+ design and verification engineers and engineering managers.
- Networking Opportunities among peers is possibly the greatest benefit to DVCon attendees.
- DVCon attendees will have access to the vendors of advanced design and verification tools, IP/VIP and services who exhibit at the conference.

CONFERENCE PROGRAM LIVE & REGISTRATION OPEN

December 10, 2014

VIEW FULL CONFERENCE DETAILS

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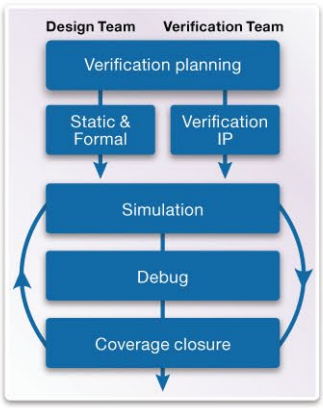

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