

2019
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
EUROPE

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HOLIDAY INN MUNICH CITY CENTRE

29 - 30 OCTOBER 2019

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WELCOME TO DVCON EUROPE 2019



DVCon Europe 2019

Welcome Message from DVCon Europe General Chair,
Joachim Geishauser

General Chair - *NXP Semiconductors*

A warm welcome to DVCon Europe 2019!

I am pleased to welcome you to the 2019 edition of the Design and Verification Conference & Exhibition in Europe!

Also this year DVCon Europe will highlight applications and trends in system-level design and verification of electronic systems and integrated circuits. DVCon Europe is a technical and industry-centric conference where users, experts, and professionals meet to share best practices on methodologies, technologies and EDA standards such as UVM, SystemC, Portable Stimulus, IP-XACT, and more.

DVCon Europe, together with Accellera's co-located SystemC Evolution Day, offers you a unique opportunity to escape from your daily work environment and learn from your peers in the industry. To address the multi-disciplinary challenges our industry is facing, DVCon Europe has broadened its scope in the call for papers and tutorials, by including embedded software. The program contains two tutorials that address the software view. This is not matching the ratio we see in the systems we create, but also a marathon run starts with the first step, and the first step is most often the most difficult. The first software tutorial covers the co-verification of safety critical software and hardware. The second software centric tutorial is exploring the software development in the exciting drone application space.

Besides the software topic, the sixth edition of DVCon Europe offers again a fully packed 2-day technical program including tutorials, panels, keynotes, presentations, and an attractive exhibition. Both days start with an exciting keynote speech held by a prominent industry speaker. This year we invited NXP and Ericsson to present their vision and developments in the Automotive, 5G and Semiconductor markets.

The keynote from NXP will explore how to cope with the demanding computation needs in applications like fully autonomous cars. On the other hand the keynote from Ericsson will enlighten such applications from the 5G perspective.

A forward-looking panel will discuss how Artificial Intelligence could reshape the verification landscape. We expect a lively discussion with the audience to explore how AI could be applied in the daily lives of design and verification engineers. A second panel will examine the use of formal verification, portable stimulus and fault injection techniques in leading automotive flows and will discuss the most effective approaches, as well as identify what is lacking for thorough verification for automotive and other safety-critical applications.

We continue the tradition to have SystemC Evolution Day co-located with DVCon Europe. This year the event takes place the day after DVCon Europe, on 31 October, also at the Holiday Inn. This full day event will focus on system simulation technology, transaction-level modeling, and model creation. If you are a system-level modeling enthusiast, expert or beginner, SystemC Evolution Day is the place to be!

Finally, I would like to thank all authors, presenters, panelists, reviewers and steering committee members for their hard work, passion and commitment to shape an interesting and high-quality program. DVCon Europe brings a strong program thanks to you!

The DVCon Europe steering committee and Accellera wish you a warm welcome and an enjoyable DVCon Europe 2019!

A handwritten signature in black ink that reads "Joachim Geishauser".

Joachim Geishauser

DVCon Europe 2019 General Chair

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Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other “smart” electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

Membership

Accellera members directly influence development of the most important and widely used standards in electronic design. Member companies protect and leverage their investment in design languages through their funding of a proven, effective and responsible organization. In addition, our members have a higher level of visibility in the EDA industry as active participants in Accellera-sponsored activities and as contributors to its decisions, which impact the EDA industry. For a full list of technical activities that are supported by Accellera, and for information on how to join us, please visit our website at www.accellera.org.

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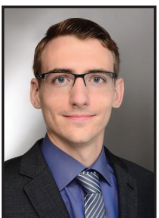
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CONFERENCE DETAILS



REGISTRATION HOURS

Location: Großer Saal Foyer

Tuesday, 29 October ----- 07:30 - 19:30

Wednesday, 30 October ----- 07:30 - 18:00

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DVCON EUROPE 2019 EXPO

Location: Großer Saal

Tuesday, 29 October ----- 10:00 - 19:00

Wednesday, 30 October ----- 10:00 - 18:30

TUTORIALS & PROCEEDINGS DISTRIBUTION

DVCon Europe Conference Papers and Tutorial presenter slides will be delivered electronically.

To access: <http://proceedings.dvcon-europe.org>

Username and password will be provided to registered conference attendees

ATTENDEE BREAKS

Location: Großer Saal

Tuesday, 29 October

08:00 - 08:30

09:30 - 10:00

11:30 - 11:45

15:45 - 16:00

Wednesday, 30 October

07:30 - 08:00

10:30 - 10:45

14:45 - 15:15

NETWORKING RECEPTIONS

Location: Großer Saal

One of the main reasons you came to DVCon Europe: NETWORKING! Introduce yourself and leave DVCon Europe with a broader professional network!

Tuesday, 29 October ----- 17:30

Wednesday, 30 October ----- 17:30

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Follow **@DVConEurope** on Twitter and tweet **#DVConEurope** about your experience and highlights at the conference!

Don't miss DVCon on Facebook at

<https://www.facebook.com/dvconeurope>

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Enjoy free Wi-Fi at DVCon Europe! Connect to the Conference Wi-Fi via:

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BEST PAPER VOTING

Vote for your favorite paper using this link: <https://dvcon-europe.org/vote> or scanning QR Code at the conference.

All votes need to be completed by 17:30 on Wednesday, 30 October, to be tallied. Award will be announced in the closing ceremony from 17:30 to 18:15 on Wednesday, 30 October, in the Exhibit Hall.

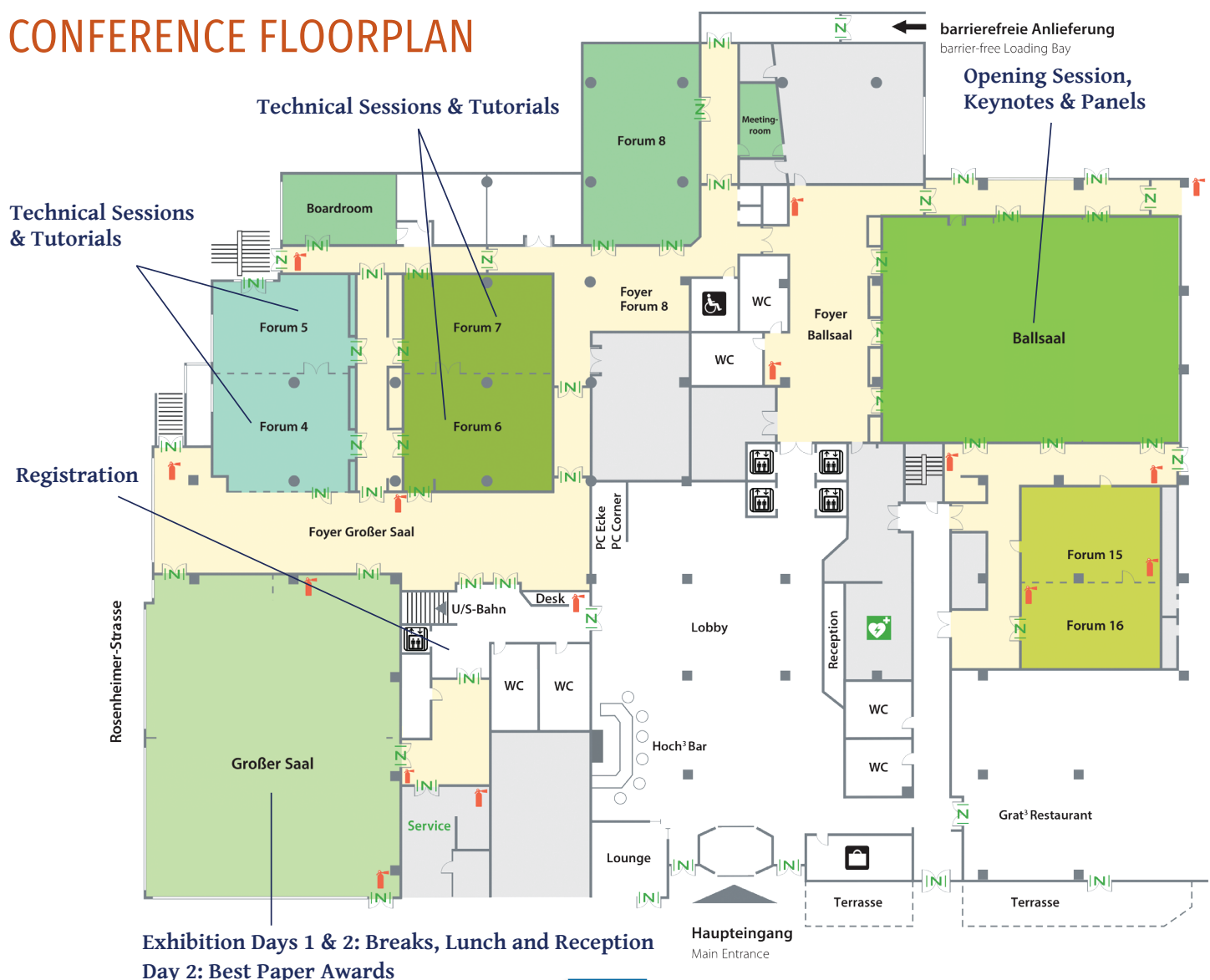
BEST PAPER AWARD ANNOUNCEMENT

Join us on Wednesday, 30 October at 17:30 in the Exhibit Hall for the Closing Ceremony and announcement of the Best Paper Awards.

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CONFERENCE FLOORPLAN



TUESDAY'S AGENDA

08:00 - 08:30	 Welcome Coffee Service Room: Großer Saal Foyer			
08:30 - 08:45	Opening Session Room: Ballsaal			
08:45 - 09:30	Keynote: Safe Computing at the Edge - Lars Reger, NXP Semiconductors Room: Ballsaal			
09:30 - 10:00	 Attendee Breat Room: Großer Saal Foyer			
10:00 - 11:30	Tutorial 1 - Building Smart SoCs - Using Virtual Prototyping for the Design and SoC Integration of Deep Learning Accelerators Room: Forum 4	Tutorial 2: RISC-V Compliance and Verification Techniques for Processor Cores Including Optional Custom Extensions Room: Forum 5	Tutorial 3: Advance your Design and Verification Flow Using IP-XACT Room: Forum 6	Tutorial 4: Applying Design Patterns to Maximise Verification Reuse @Block, Subsystem and System-on-Chip Level Room: Forum 7
10:00 - 19:00	DVCon Europe Expo Room: Großer Saal			
11:30 - 11:45	 Attendee Break Room: Großer Saal			
11:45 - 13:15	Tutorial 5: Early Performance Verification of Embedded Inferencing Systems Using Open-Source SystemC NVIDIA MatchLib Room: Forum 4	Tutorial 6: 5G New Radio Explained: From 3GPP 5G Standard Fundamentals To 5G-Enabled Verticals Room: Forum 5	Tutorial 7: UVM-SystemC – Functional Coverage & Constrained Randomization Room: Forum 6	Tutorial 8: QED & Symbolic QED: Pre-Silicon Verification, Post-Silicon Validation, Industrial Results Room: Forum 7
13:15 - 14:15	Luncheon Room: Großer Saal			
14:15 - 15:45	Tutorial 9: Next Gen System Design and Verification for Transportation Room: Forum 4 Thank you to our Sponsor Mentor A Siemens Business	Tutorial 10: RISC-V Integrity: A Guide for Developers and Integrators Room: Forum 5 Thank you to our Sponsor onespin making electronics reliable	Tutorial 11: Unified Functional Safety Verification Platform for ISO 26262-Compliant Automotive Designs Room: Forum 6 Thank you to our Sponsor SYNOPSYS	Tutorial 12: Cadence® vManager TM Platform and Virtuoso® ADE Verifier: Leading Edge Technologies Provide the Methodology for Mixed-Signal Verification Closure Room: Forum 7 Thank you to our Sponsor cadence
15:45 - 16:00	 Attendee Break Room: Großer Saal			
16:00 - 17:30	Tutorial 13: Solve Software Coding Challenges with Exciting New Drone Technology Room: Forum 4 Thank you to our Sponsor NXP	Tutorial 14: Safety and Security Aware Pre-Silicon Hardware / Software Co-Development Room: Forum 5 Thank you to our Sponsor Green Hills SOFTWARE	Tutorial 15: Revitalizing Automotive Safety Hard and Soft Error Approaches Room: Forum 6 Thank you to our Sponsor OPTIMA	Tutorial 16: Be a Sequence Pro to Avoid Bad Con Sequences Room: Forum 7 Thank you to our Sponsor verilab
17:30	DVCon Europe Reception & Expo Room: Großer Saal			

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Welcome Coffee Service

Time: 8:00 - 8:30 | Room: Großer Saal Foyer

Opening Session

Time: 08:30 - 08:45 | Room: Ballsaal



Keynote: Safe Computing at the Edge

Time: 8:45 - 9:30 | Room: Ballsaal

Speaker:

Lars Reger - NXP Semiconductors

Advances in two areas have spurred the evolution of electronics in the last few years: connectivity on the one, storage and processing power of the cloud on the other. They were the starting point for manufacturers to make their devices smarter: from a wristwatch to a connected vehicle. Smarter than a stand-alone device could ever be, and in addition, capable of self-learning.

However, the cloud has reached its limits: to reliably monitor an entire production site or drive a fully autonomous car through traffic, processing all data in the cloud becomes simply too slow, too bandwidth-hungry, and too insecure as a single point of service. Therefore, edge computing is where the action is and will be, directly at the smart device.

Mastering edge computing with the right level of safety and security is critical to the deployment of artificial intelligence in the mass market. The Keynote from Lars Reger will explore the challenges on the route to an ever smarter, on-demand world.

Biography: Lars Reger, Senior Vice President, is Chief Technology Officer at NXP Semiconductors. As CTO, Lars is responsible for managing new business activities and R&D in the focus markets of Automotive, Industry 4.0., Internet of Things, Mobile, and Connectivity & Infrastructure. NXP has the broadest processor portfolio for the Internet of Things and is the world's largest chip supplier to the automotive industry. NXP and its global team of experts drive the development of autonomous, securely connected vehicles and accelerate the introduction of smart and securely connected devices for the Internet of Things through its outstanding edge computing expertise. Before joining NXP, Lars gained deep insight into the microelectronics industry with a focus on the automotive sector. He began his career with Siemens Semiconductors as Product Engineer in 1997. His past roles at Infineon included Head of the Process and Product Engineering departments, Project Manager for Mobile System Chips, and Director of IP Management. Prior to joining NXP as CTO of the automotive division in 2008, he was responsible for business development and product management within the Connectivity Business Unit at Continental. In December 2018 Lars was appointed CTO and has since then been responsible for the overall technology portfolio of NXP.

Attendee Break

Time: 9:30 - 10:00 | Room: Großer Saal Foyer

Tutorial 1: Building Smart SoCs - Using Virtual Prototyping for the Design and SoC Integration of Deep Learning Accelerators

Time: 10:00 - 11:30 | Room: Forum 4

Organizer:

Holger Keding - *Synopsys, Inc.*

Artificial Intelligence enables a whole new range of applications in the areas of Virtual and Augmented Reality, robotics, IoT, healthcare, retail and logistics, mobile, automotive, and others. In particular, Deep Neural Networks (DNNs) have enabled quantum leaps in brain-like functions such as speech and image recognition. Today, the training of Neural Networks is typically performed in data centers on standard GPU architectures, which are optimized for highest throughput, but there is still need to provide much higher performance. Also the inference of Neural Networks would greatly benefit from tailored architectures to deliver faster responses, both in the data center as well as for embedded applications. However, the design of tailored SoC platforms for training and inference of Artificial Intelligence applications is very challenging:

- The fast pace of innovation and differentiation of AI applications requires high flexibility in the underlying architecture to support evolving AI algorithms with varying number of layers, filters, channels, and filter sizes.
- The execution of AI algorithms like Neural Network graphs requires very high computational performance and memory bandwidth.
- Embedded applications, especially mobile devices, need to have low power consumption. Even for data-centers, the power efficiency is the dominant cost factor.

In the past, scaling power and performance of programmable architectures came for free by moving to smaller technology nodes. However, as Moore's Law does no longer deliver 2x transistors every 2 years at same price, the necessary improvements in power, performance, and flexibility need to come from better architectures:

- Customization of the micro-architecture to the algorithmic kernels
- Designing the macro-architecture with the right level of block-level parallelism to achieve the desired throughput.
- Selecting the best data flow for the Neural Network based on the data handling characteristics. Typical data flows are weight stationary, output stationary, no local reuse, or row stationary.
- Optimizing the implementation of the data transfers with tailored DMA engines and local buffering to get the most out of the limited bandwidth to the external memory. This is particularly important, because most Neural Network algorithms are memory-bandwidth limited.

This tutorial will show how Virtual Prototyping can help to design accelerators for deep learning and integrate them in the SoC context.

Speaker:

Holger Keding - *Synopsys, Inc.*



Tutorial 2: RISC-V Compliance and Verification Techniques for Processor Cores Including Optional Custom Extensions

Time: 10:00 - 11:30 | Room: Forum 5

Organizer:

Kevin McDermott - Imperas Software Ltd.

For traditional single or closed sourced instruction set architectures (ISAs), compliance to the ISA specification is addressed during the internal development. With the new, open standard RISC-V ISA, the compliance situation is different. In addition to the multiple IP providers many will also exploit the capability with the open ISA to add custom instructions or other optimizations. Compliance testing therefore has become mission-critical for the RISC-V ecosystem to accommodate the wide adoption and support of compatible features while retaining the optimizations that the ISA permits.

For other ISAs compliance testing has been addressed by the processor IP vendor, and as a result methodologies and tools for compliance testing have been kept internal, and are not readily available to the industry in general.

Verification of an Open ISA also needs to address the addition of custom instructions and extensions as well as all the standard options and configuration features.

The tutorial covers RISC-V Compliance testing and Verification with Instruction stream and cloud based testing.

Part #1 - Imperas

This tutorial presentation introduces the methodologies being developed for compliance and verification testing of RISC-V, including a framework for development of additional tests, the development of the tests, reference models, and configurations for the RISC-V specification subsets.

Compliance and Verification based on free reference simulator for development and test of hardware including the analysis of the completeness and specification coverage of current compliance tests. Use cases are examined, including testing compliance on various proprietary RTL designs, open source RTL designs, FPGAs, SoCs, ISS models and software tools, with detailed analysis of the issues experienced.

This tutorial presentation will answer the key question on what to do on day 1 when you receive a RISC-V implementation – after “Hello World” run the full compliance and verification flow against the Golden Imperas model.

Part #2 - Google

Introduction and overview of test flow and framework based on a free open source instruction generator for UVM-based RISC-V Processor Verification.

Verification based on instruction generator and comparison between RTL under test and a reference simulator.

Test results include examples from multiple popular open source processors with detailed reports and highlights.

Part #3 - Metrics

The RISC-V Open ISA is different from the established single-sourced ISA in a number of aspects. This tutorial presentation will review the changing role of EDA design flows and addresses the needs of all participants in the SoC IP supply chain to contribute towards the DV task.

IP Core providers, open source options, in-house developments, plus options for all participants to modify and extend instructions or extensions – now everyone needs access to verification frameworks.

Can cloud based tools help address the expected demand and flexibility for verification capacity?

Speakers:

Simon Davidmann - Imperas Software Ltd.

Lee Moore - Imperas Software Ltd.

Doug Letcher - Metrics Technology, Inc.

Richard Ho - Google, Inc.



Tutorial 3: Advance your Design and Verification Flow Using IP-XACT

Time: 10:00 - 11:30 | Room: Forum 6

Organizer:

Martin Barnasconi - *NXP Semiconductors*

The IP-XACT standard defined in IEEE 1685 provides an XML schema to capture meta-data of intellectual property (IP), and facilitates design flow automation for specification, design, integration, verification and documentation of complex electronic systems composed of hardware and software. IP-XACT has become an established technology supported by IP and EDA solution providers and semiconductor companies and design centers have adopted IP-XACT for design flow automation.

In this tutorial, different companies active in IP-XACT standardization and usage will share their experiences on the application, capabilities on IP-XACT and explain how it can enrich and complement existing design and integration strategies.

IP provider ARM will demonstrate how they support the IP-XACT eco-system. ARM will present how IP-XACT is used in the IP creation process and how their IP deliveries apply AMBA bus-definitions captured in IP-XACT. With the support of the ARM Socrates tooling, they deliver IP-XACT updates to established IPs. ARM supports the IP-XACT standardisation by providing the M3 Design Start system. They will conclude their presentation with a roadmap update.

EDA solution provider Magillem Design Services will share a global picture on IP-XACT usage in the SoC design domain, and introduce its vision on how IP-XACT is enabling integration of said design into the larger ecosystem. User company Texas Instruments will highlight how IP-XACT can simplify and accelerate cross-functional alignment throughout the incremental phases of IP or SoC development. Furthermore, the long-term benefits of an IP-XACT-based automation flow will be shown on the example of customer-facing documentation and CMSIS-compliant software collaterals.

User company Texas Instruments will highlight how IP-XACT can simplify and accelerate cross-functional alignment throughout the incremental phases of IP or SoC development. Furthermore, the long-term benefits of an IP-XACT-based automation flow will be shown on the example of customer-facing documentation and CMSIS-compliant software collaterals.

Speakers:

Edwin Dankert - *Arm, Ltd.*

Max Albrecht - *Texas Instruments, Inc.*

Robert Lessmeier - *Texas Instruments, Inc.*

Vincent Thibaut - *Magillem Design Services*

Tutorial 4: Applying Design Patterns to Maximise Verification Reuse @Block, Subsystem and System-on-Chip Level

Time: 10:00 - 11:30 | Room: Forum 7

Organizer:

Paul Kaunds - *Sondrel Ltd*

Verification Planning, Verification Environment development and achieving coverage closure goals on time and under budget are the most challenging assignments in functional verification.

In this tutorial, we will provide an in-depth analysis of various planning, implementation, debug and coverage closure challenges faced in functional verification at block level, subsystem and system-on-chip level. By taking relevant

examples we will demonstrate how these issues can be either avoided or solved by applying Design Patterns, mainly Environment, Stimulus and Analysis Patterns. We will also highlight some of the benefits like configurability and reusability of UVM and C code.

Speakers:

Revati Bothe - *Sondrel Ltd.*

Jesvin Johnson - *Sondrel Ltd.*

Exhibit Floor Open

Time: 10:00 - 19:00 | Room: Großer Saal

Attendee Break

Time: 11:30 - 11:45 | Room: Großer Saal

Tutorial 5: Early Performance Verification of Embedded Inferencing Systems Using Open-Source SystemC NVIDIA MatchLib

Time: 11:45 - 13:15 | Room: Forum 4

Organizer:

Russell Klein - Mentor, A Siemens Business

Machine learning is being applied to an increasing number of embedded systems. While some systems may be able to send inferencing tasks to the cloud, many will be required to perform inferencing on board. With constrained compute resources and limited power inferencing algorithms need to be carefully designed to balance the need for performance while remaining within a strict power budget.

Inferencing algorithms often rely on multi-dimensional convolutions, which generate large amounts of intermediate data. In fact, the design of the memory architecture and the management of the data movement in the system may be more impactful on performance and power consumption than the architecture of the computational units themselves.

However, waiting until RTL is available to evaluate the performance of the inferencing engine is often too late in the design cycle. Further, evaluating multiple architectures at the RTL level is too time consuming and expensive for most projects.

This tutorial will teach developers to use NVidia Matchlib to perform throughput accurate analysis of an inferencing system using C++/SystemC, prior to the development of RTL. NVidia MatchLib is a new open-source library of C++/SystemC components that can be used to model a system in a way that throughput can be verified early in the design cycle.

To concretely illustrate these concepts, an example based on the implementation of a “wake word” inferencing system will be explored. Wake word systems continuously monitor an incoming audio stream for a specific word, using a trained neural network to identify the specific word or phrase. Once the word is identified, the embedded system is brought to life. For battery powered systems, the continuously running convolutional neural network must be as power efficient as possible, while meeting hard real-time requirements. We will demonstrate the example design running in SystemC using Matchlib using open source tools and IP.

Speakers:

Stuart Swan - Mentor, A Siemens Business

Herbert Taucher - Siemens AG

Tutorial 6: 5G New Radio Explained: From 3GPP 5G Standard Fundamentals To 5G-Enabled Verticals

Time: 11:45 - 13:15 | Room: Forum 5

Organizer:

Oliver Bell - Intel Germany GmbH

While 2019 is the year of 5G smartphone and 5G network launches, 5G indeed enables a manifold of innovations in vertical segments and new user experiences that will transform our world and our daily lives. Among the most prominent vertical segments fuelled by 5G are: Industrial IOT, Automotive, and Immersive Media. Autonomous robots on the industrial shop floor, latency-critical factory automation and industrial control stand for the requirements in Industrial IOT. Autonomous driving, remote control of vehicles, and 5G New Radio vehicle-to-everything (NR-V2X) will transform the Automotive segment. Finally, immersive media offered at large Sports events or consumed as Virtual Reality content at home,

Cloud gaming, as well as Augmented Reality enable great new experiences and collaboration techniques.

This tutorial has been developed by representatives of Intel's 5G standardization and prototyping teams and will provide an introduction to 3GPP Release 15/16 for enhanced mobile broadband (NR eMBB), ultra-reliable low latency communication (NR URLLC), NR-V2X, and system aspects involving Multi-access Edge Computing (MEC) while explaining how the standard's capabilities and system aspects interplay for Industrial IOT, Automotive, and Immersive Media.

Speaker:

Michael Faerber - Intel Germany GmbH

Tutorial 7: UVM-SystemC - Functional Coverage & Constrained Randomization

Time: 11:45 - 13:15 | Room: Forum 6

Organizer:

Stephan Gerth - Bosch Sensortec GmbH

UVM-SystemC is an implementation of the Accellera UVM standard originally implemented in SystemC. Standardization efforts of UVM for SystemC (named UVM-SystemC) have gained momentum to the point that multiple public review releases were released in the past years.

UVM-SystemC can be used with CRAVE, a C++ and SystemC constraint randomization library. However, standardized functional coverage aspects are currently missing within UVM-SystemC. In the meantime, AMIQ publicly released FC4SC, a functional coverage library aimed at SystemC under Apache License, which closes this important gap.

This tutorial will introduce the basic concepts and will give in-depth examples on how to apply CRAVE & FC4SC with UVM-SystemC, to address the current challenges in ESL design and verification environments.

Currently, the Accellera VWG is working on the standardization of a common randomization layer and a definition of functional coverage for UVM SystemC.

This tutorial will be presented in three sections. In the first introductory section, several key mechanisms of constraint randomization and functional coverage in UVM contexts are shown to bring the audience to a common basic knowledge level. The basic concepts of the Universal Verification Methodology (UVM) will be presented and how constrained randomization and functional coverage can improve verification efforts. The knowledge on how to effectively combine and apply UVM, constrained randomization and functional coverage are the key to enable the verification of complex systems. Additionally, the re-use aspect of optimal verification results will be shown, especially when the design-under-test changes but contains similar interfaces.

The past and current standardization efforts within the Accellera Verification Working Group will be presented to show the evolution of UVM-SystemC within the working group. Further

motivation and examples are given, showing how SystemC users can benefit from a standardized UVM implementation within their SystemC environment in their daily verification needs, especially considering an updated constrained randomization implementation and a publicly available functional coverage implementation. The current state of the proof-of-concept implementation will be shown and how it can be applied in current design flow setups.

The second part of the tutorial will present in-depth examples: First a combined application of constrained randomization and functional coverage using the above-mentioned libraries with UVM-SystemC, and second, a verification IP library approach by extensively relying on the re-use aspect of UVM-SystemC in addition to functional coverage for verification sign-off.

The final section will discuss the ongoing development of the proof-of-concept implementation and the language reference manual to show clearly where UVM-SystemC is headed and what has been already achieved in the past activities. As a closing item, future standardization topics, such as constrained randomization and functional coverage, within the Accellera Verification Working Group and further application fields of UVM-SystemC will be discussed to give the audience an outlook.

The intended audience includes managers, system and verification engineers and architects with a basic knowledge in SystemC and/or UVM, which are interested to further improve their system-level verification practices.

Speakers:

Muhammad Hassan - Univ. of Bremen

Stephan Gerth - Bosch Sensortec GmbH

Thilo Vörtler - COSEDA Technologies

Manuel Soto - Fraunhofer IIS, Institutsteil EAS

Dragos Dospinescu - AMIQ



Tutorial 8: QED & Symbolic QED: Pre-Silicon Verification, Post-Silicon Validation, Industrial Results

Time: 11:45 - 13:15 | **Room:** Forum 7

Organizer:

Subhasish Mitra - *Stanford Univ.*

This tutorial presents an end-to-end approach to pre-silicon verification and post-silicon validation of digital systems: the Quick Error Detection (QED) technique for post-silicon validation and debug, and the Symbolic QED technique for pre-silicon verification. Several industrial case studies (from AMD, Infineon, Intel and Freescale/NXP) will be covered. Practical experience in using these techniques for pre-silicon verification of safety-critical automotive designs at Infineon will be emphasized.

QED drastically reduces error detection latency, the time elapsed between the occurrence of an error caused by a bug and its manifestation as an observable failure. Symbolic QED combines QED principles with a formal engine for both pre- and post-silicon validation. These techniques are effective for logic design bugs and electrical bugs inside processor cores, hardware accelerators, and uncore components (cache controllers, memory controllers, interconnection networks or power management units).

Results from several commercial and open-source designs demonstrate:

1. For billion transistor-scale designs, Symbolic QED detects and localizes difficult logic design bugs automatically in only a few (3-7) hours during pre-silicon verification.

2. For open-source RISC-V processor cores, Symbolic QED detects (previously unknown) real logic design bugs within minutes automatically.
3. An industrial case study on commercial automotive designs (at Infineon) shows that Symbolic QED detects all difficult logic design bugs while enabling 60-fold improvement in verification productivity (2 person-days using Symbolic QED vs. several person-months using conventional industrial flow).
4. QED drastically improves error detection latencies of post-silicon validation tests by up to 9 orders of magnitude, from billions of clock cycles to very few clock cycles, and simultaneously improves bug coverage.
5. QED-aided debug techniques automatically localize bugs in billion-transistor-scale designs during post-silicon debug, e.g., one can automatically narrow down the location of an electrical bug to a handful of flip-flops (~18 for a design with 1 million flip-flops), in only a few (~9) hours.

Speakers:

Subhasish Mitra - *Stanford Univ.*

Eshan Singh - *Stanford Univ.*

Keerthikumara Devarajegowda - *Infineon Technologies AG*

Lunch

Time: 13:15 - 14:15 | **Room:** Großer Saal



Tutorial 9: Next Gen System Design and Verification for Transportation

Time: 14:15 - 15:45 | **Room:** Forum 4

Organizer:

Rebecca Granquist - *Mentor, A Siemens Business*

Increased intelligence and autonomy of next-generation transportation products are driving the ICs behind those moving machines to become some of the most advanced semiconductor products in the industry. As a result, this is disrupting how you design, verify and develop these ICs.

Starting with design, the entrance of machine learning using neural networks and inference solutions has demonstrated the need to quickly develop these highly algorithmic designs. Validation of those algorithms, performance targets, and power consumption demands new solutions that can simulate the complex, heterogeneous systems with real world interactions. Beyond just ensuring the IC operates correctly, functional safety standards, like ISO 26262 for automotive, are enforcing state-of-the-art practices, strict processes and evidence for compliance to ensure the delivered capabilities are functionally safe. The days of separating functional workflow development from the safety workflow has passed. It is imperative that safety be at the forefront when determining the methodologies and tools to deploy in the creation of your transportation application.

The intersection of these challenges is delivering advanced features on-time, within budget all while simultaneously ensuring the IC will not malfunction.

This tutorial will demonstrate how to use these next-generation IC development practices to build and validate smarter, safer ICs. Specifically, it will look at:

- How to use High-Level Synthesis (HLS) to accelerate the design of smarter ICs
- How to use emulation to provide a digital twin validation platform beyond just the IC
- How to use develop functionally safe ICs

Speakers:

Richard Pugh - *Mentor, A Siemens Business*

Bryan Ramirez - *Mentor, A Siemens Business*

Petri Solanti - *Mentor, A Siemens Business*

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Tutorial 10: RISC-V Integrity: A Guide for Developers and Integrators

Time: 14:15 - 15:45 | **Room:** Forum 5

Organizer:

Tom Anderson - *OneSpin Solutions GmbH*

RISC-V is changing the game for IP providers and SoC designers. Providers can offer commercial cores without the need to acquire expensive rights, while open-source implementations are already available. SoC teams that want to use RISC-V processors have several choices today, with even more options expected soon. The sheer number of companies and products using RISC-V guarantees a rich ecosystem and a good opportunity for industry disruption.

However, design integrity is a challenge for both core developers and core integrators. To be successful, IP vendors must produce products that compete against long-established processor families with decades of proven silicon. RISC-V cores must be thoroughly verified as functionally correct using third-party solutions so that different cores all satisfy the Instruction Set Architecture (ISA) and other requirements. Integrators must be certain that available cores are fully compliant, and many will want to re-verify the one they choose.

Verifying that a RISC-V core meets the ISA and does what it is supposed to do is only one aspect of integrity.

It is also critical to prove that the core does not do anything that it is not supposed to do. Hardware Trojans or other unintended logic can be inserted at multiple points in the development

process. Showing that the RISC-V core can be trusted requires proving that no such issues exist. Only formal verification has the potential to prove both ISA compliance and trust.

Trojans can be used by malicious agents to compromise a chip during operation, but some types of unintentional design errors can also provide an attack gateway. Analysis of the RISC-V core can prove that no such vulnerabilities exist and that the design is secure. Safety must also be addressed since many RISC-V designs are used in safety-critical applications. Standards such as ISO 26262 place demanding requirements on chip designs so that they will continue to function even in the presence of random errors such as Alpha particle hits.

This tutorial provides guidance for RISC-V core vendors who need to verify their IP, developers of cores for internal consumption, engineers evaluating cores for possible use, and SoC teams integrating RISC-V cores from internal or external sources. It covers the complete scope of RISC-V core and SoC integrity: functional correctness (compliance to the ISA), safety, security, and trust. It includes examples of actual bugs found in open-source implementations of RISC-V cores and RISC-V-based SoCs.

Speaker:

Nicolae Tusinschi - *OneSpin Solutions GmbH*

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making electronics reliable

Tutorial 11: Unified Functional Safety Verification Platform for ISO 26262-Compliant Automotive Designs

Time: 14:15 - 15:45 | Room: Forum 6

Organizer:

Joerg Richter - Synopsys, Inc.

Automotive has evolved into one of the fastest growing parts of the worldwide semiconductor industry, and automotive semiconductor content is exploding, driven by many advanced SoCs powering autonomous drive, infotainment, and vehicle communication systems. The “traditional” automotive electronics are not standing still either, with advanced drivetrains and sophisticated safety and ADAS systems creating demand for even-larger and more integrated SoCs.

As automotive electronic systems become ever more complex, the potential impact on the safety of vehicles' occupants and bystanders becomes a critical consideration for these systems. ISO 26262, the functional safety standard for road vehicles was created to guide the development of electrical and electronic systems for automobiles, and was recently released in a 2nd edition. For IP and SoC companies, ISO 26262 product development at the hardware level guidelines are particularly important – from a verification perspective, it lays out a set of requirements for functional safety that need to be understood and followed, and which are in addition to best-practice functional verification methodologies.

State-of-the-art functional safety verification must be performed, with the objective of determining the product's ability to safely manage random faults that may arise during its lifecycle. This is a different verification objective compared to functional verification. To achieve the needed qualification in shortest amount of time, various technologies like static, formal, simulation and emulation must be combined in a unified functional safety platform.

This tutorial will provide a practical, hands-on overview of the following:

- ISO 26262 considerations for SoC and IP design verification, customer insights and today's challenges
- Unique challenges for automotive SoC and IP verification engineering teams
- Best practice methodologies for functional safety verification
- Unified functional safety platform with
- FMEA (Failure Mode Effect Analysis) planning to FMED (Diagnostic) A management
- Static methods to estimate fault and diagnostic coverage
- Formal methods to prune the fault set and guide coverage closure
- Fault injection testing with simulation and emulation
- Annotation of diagnostic data
- Conclusions and QA

Speaker:

Joerg Richter - Synopsys, Inc.

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Tutorial 12: Cadence® vManager™ Platform and Virtuoso® ADE Verifier: Leading Edge Technologies Provide the Methodology for Mixed-Signal Verification Closure

Time: 14:15 - 15:45 | **Room:** Forum 7

Organizer:

Kawe Fotouhi - Cadence Design Systems, GmbH

In today's SoC designs, the level of interaction between analog structures and digital logic is increasing dramatically. The pure "divide-and-conquer" approach to design and verification has proven not to be enough anymore. The analog/digital interdependency creates a requirement for a more integrated and sophisticated approach to mixed-signal verification.

For good reasons, mixed-signal verification teams are working in different environments and domains:

- The pure analog verification is based on transistor-level circuits being designed as schematics and simulated within the analog design environment.
- In the digital domain, metric-driven verification based on UVM methodology has become a quasi-standard.
- At the SoC level, you need a way to quickly model your design with enough accuracy for your application. Real number modelling (RNM) allows you to take the best from both worlds.

A predictable verification closure flow requires an efficient planning and metrics management using automated checks and coverage at the block, chip, and system levels simultaneously. New ISO standards like 26262, advanced-node technologies, and the requirements for verification quality, forced industry leaders to seek for a more formalized methodology – including analog.

Cadence provides two domain specific platforms to accomplish verification closure: Cadence® vManager™ platform and the Virtuoso® ADE product suite. In the latest releases, these platforms can synchronize the verification plans and results data in real-time which enables a full qualification of a mixed-signal verification signoff.

Cadence vManager™ Metric-Driven Signoff Platform, an automated verification planning and management solution, is the lead tool in the digital flow. The tool deploys execution runs, sets up analysis views, organizes and debugs errors, and generates additional verification scenarios.

Virtuoso® ADE Assembler and Verifier allow users to do analog verification planning, synchronize and check specification values, automate their analog verification, and get a global view of the status of different team members. With the new link to vManager, these analog contributions are an integral part of the chip verification process.

The heart of the verification is communication and planning. The "vplan" is the central document to align the different teams and structure the results. The new connection between ADE Verifier and vManager allows the user to develop the vplan as a joint effort using both tools for all 3 domains: analog, digital and RNM. This capability allows analog and digital engineers to continue to work in their familiar environments while working together on the same plan. The results are accessible in a single cockpit enabling an efficient sign off process and tracking for all domains.

Attendees to this tutorial will gain practical knowledge on how to enable the development of a joint verification plan for the corresponding domains. Furthermore, the tutorial shows how analog and digital verification-execution and verification plan-refinement is done inside ADE Verifier in parallel with vManager. Verification results and the plans are synchronized within the vManager to track the overall verification progress in real-time.

Speakers:

Walter Hartong - Cadence Design Systems, GmbH

Kawe Fotouhi - Cadence Design Systems, GmbH

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Attendee Break

Time: 15:45 - 16:00 | **Room:** Großer Saal

Tutorial 13: Solve Software Coding Challenges with Exciting New Drone Technology

Time: 16:00 - 17:30 | Room: Forum 4

Organizer:

Joachim Geishauser - NXP Semiconductors

HoverGames, an interactive and challenging coding competition, unites talented developers across the globe to address some of the biggest challenges facing society – by building on the HoverGames development platform for autonomous drones and rovers! Participants will confront universal issues like disaster management, health crises, environmental protection, wildlife conservation and more.

This tutorial will introduce the NXP Drone Development Kit, which includes everything to build a flying robot. This drone isn't a toy flyer, but a specialized hardware and software development platform based on PX4, the largest commercially deployed open source flight stack worldwide. The technology you learn to use in this tutorial is transferrable to real-world commercial applications because it uses off-the-shelf NXP products used in automotive and industrial applications.

The first section of the tutorial will present the hardware of the drone itself and introduces the NXP board RDDRONE-FMUK66, the flight management unit (FMU) based on NXP's Kinetis K66 microcontroller. In addition, the FMU board contains NXP sensors, automotive CAN bus transceivers, as well as the new two-wire automotive ethernet transceivers.

The second part of the tutorial will explain the software ecosystem using the Dronecode environment including PX4 software flight stack which will run on the Kinetis K66. The flight control software QGroundControl is explained, which is used to set up and configure the drone to make it ready to fly including mission planning.

In the last part of the tutorial, a simple PX4 application example is created, and the audience is encouraged to perform some hands-on programming. It will explain the basic concepts and APIs required for app-development using PX4. The example uses the PX4 Software-in-the-loop (SIL) simulator and the PX4 source code and development toolchain from Github. For those who have a RDDRONE-FMUK66 or other PX4-compatible flight controller, the firmware can be uploaded to the board.

This tutorial uses a preconfigured Ubuntu Linux virtual machine image, including the tools for editing, building and debugging software for the RDDRONE-FMUK66 and other HoverGames hardware. Attendees are encouraged to download and install this virtual machine prior to the start of this tutorial.

Learn more about the challenge on www.hovergames.com

Get the drone kit on www.nxp.com/hovergamesdrones

Download the HoverGames virtual machine on <https://nxp.gitbook.io/hovergames/downloads>

Speaker:

Martin Barnasconi - NXP Semiconductors

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Tutorial 14 - Safety and Security Aware Pre-Silicon Hardware/Software Co-Development

Time: 16:00 - 17:30 | Room: Forum 5

Organizer:

Stephan Janouch - Green Hills Software, Inc.

Simultaneously developing and testing both software and SoC designs before silicon is available can help to reduce the time and cost of building embedded devices. Merging the software and hardware development before silicon saves time and money by enabling to get the embedded product to market faster. This tutorial illustrates a new pre-silicon development process for concurrent SoC and software development and verification for safety and security critical systems, composed of a safety-certified RTOS and advanced C/C++ development tools that continuously support SoC verification from the

earliest functional execution (through Virtual Prototyping), RTL simulation, emulation and FPGA prototype stages on the path to first silicon. The convergence of a traditional software development environment and a hardware development and verification platform brings more safety, security and verified reliability while establishing a more mature software enablement foundation for customers by the time they get their hands on first silicon.

Speakers:

Frank Schirrmeister - Cadence Design Systems, Inc.

Nikola Velinov - Green Hills Software, Inc.

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Tutorial 15: Revitalizing Automotive Safety Hard and Soft Error Approaches

Time: 16:00 - 17:30 | Room: Forum 6

Organizer:

Habib Karam - *Optima Design Automation*

This tutorial is appropriate for any engineers or engineering managers concerned with automotive safety fault analysis. Optima Design Automation will explore new approaches, based on their high-performance fault simulation technology platform, for analyzing both permanent faults (or Hard Errors), together with transient faults (or Soft Errors) that have significantly improved real design flows at leading semiconductor companies. The tutorial will include the exploration of real results. Attendees will be exposed to new methods and approaches that could improve their fault analysis solutions.

Random fault analysis for safety-critical automotive semiconductors remains a laborious and difficult task. Fault analysis using current fault simulation tools simply takes too long and can result in indeterminate coverage metrics. Some fault types are hard to analyze at all.

Proving that devices meet the ISO 26262 ASIL-C/D safety tolerances has always been difficult. Using traditional fault simulation, even when augmented with formal verification tools, weeks of analysis are required to ensure that safety mechanisms eliminate a high proportion of dangerous faults.

Hard errors include permanently stuck at 1 or 0 faults, bridging faults between two signals, or tristate signals. Proving >99% of these faults either does not affect the operation or may be eliminated by safety mechanisms is required for ASIL-D certification. Achieving this level of coverage using regular fault simulation has proven extremely difficult, to the point where many organizations have given up with this requirement.

Soft errors or transient faults are even harder to analyze using these techniques. Transient faults are handled mostly by using selective hardening, where a proportion of flip-flops are altered such that they "swallow" transient errors. These hardened flops are expensive in terms of silicon area and power consumption so qualifying the design such that a minimal number of flops are hardened to achieve required coverage is important. However, this level of analysis is hard to achieve with basic fault simulation.

Optima Design Automation has taken a new approach to both hard error and soft error analysis. The company has developed a new form of fault simulation technology that provides multi-

orders of magnitude performance improvement over other fault analyzers. Using this as a platform it is possible to drive more effective approaches to analyze both Hard and Soft Error faults.

This tutorial will detail how permanent and transient faults may be handled more effectively and quickly than previously possible.

For Hard Errors, the structural analysis will be performed that categorizes fault types and provides a more effective fault pruning before fault-simulation execution. The fault simulator runs and operates in a fraction of the time of previous tools. With this faster operation, it is possible to rapidly update the Software Test Library to provide more effective tests and prove out faults more quickly.

With this method, greater coverage may be achieved, but this is still potentially not to the level required. An additional coverage boosting mechanism may be employed to identify coverage holes and fill them relatively automatically.

The tutorial will also include Soft Error analysis, with the aim of producing an optimal set of flip flops to be hardened providing ASIL-D coverage with minimal power and silicon area increase. This methodology involves an iterative fault simulation process usually too expensive. However, the approach presented in this tutorial, coupled with high-performance simulation, will provide the ultimate flip-flop configuration.

The tutorial will use presentations and demonstrations. Real results from end-users will be shown alongside the tutorial sections.

The agenda:

- The current state of the art in Automotive Safety Fault Analysis
- Hard Error fault detection, grading and coverage boosting
- Soft Error analysis and selective hardening optimization
- Real design results

Speaker:

Jamil Mazzawi - *Optima Design Automation*

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Tutorial 16: Be a Sequence Pro to Avoid Bad Con Sequences

Time: 16:00 - 17:30 | Room: Forum 7

Organizer:

Mark Litterick - Verilab, Inc.

The Universal Verification Methodology (UVM) is widely accepted as the industry standard for verification of chip designs. While UVM has many features to help with the challenges of verifying complex designs, UVM sequences for stimulus arguably have the most impact on verification quality. Despite the maturity and widespread success of UVM across many projects, evidence has shown that UVM sequences are typically not applied to their fullest potential. This is largely due to a lack of published resources with guidance on how to define large-scale sequence libraries to solve more complex verification challenges. The consequences are seen in typical projects where large collections of ad-hoc sequences create additional problems for engineering teams instead of helping them tape out bug-free designs on schedule. These challenges include additional unnecessary complexity, insufficient control of stimulus for tests, and limited reuse.

In addition to the general problems of ad-hoc sequence libraries, UVM sequences are vital to success in several ways that are often overlooked. There is little guidance on how to apply sequences for controlling continuous streams of data over time. This includes digital streaming data, analog stimulus, and clock generation. Sequences also serve as an API to engineering teams who must create verification plans, manage test regressions, triage debug tasks, report project status, and manage risks to meet schedules. An inadequate sequence API to support these tasks frequently creates workflow bottlenecks as teams struggle to transfer knowledge, isolate problems, and transparently report status to project stakeholders.

Finally, UVM sequences will continue to be used by teams that are considering adopting the newer Portable Stimulus methodology. In order to successfully integrate high-level portable stimulus with a simulation-based testbench, an adequate UVM sequence API is vital. This workshop addresses all these problems by providing guidelines based on extensive project experience applying UVM sequences in a variety of situations, from small block-level testbenches to complex integrations with challenging reuse and usability demands.

Workshop Content

• Sequence Library Guidelines

We outline a sequence API layering strategy that provides better encapsulation for UVCs, reduces complexity for test writers, and allows better reuse of sequences within a sequence library (and between derivative projects). We then give implementation guidelines that most impact the problems of complexity, control and reuse in a sequence library. These guidelines include a comparison of different constraint model techniques and recommendations for which are most ideal for certain testbench goals.

• Sequences for Streaming Data

We give guidelines on controlling continuous streams of values over periods of time. Examples include clock generation with jitter and skew, steaming data to external digital interfaces, and analog stimulus. In these cases, we need fine grained control over the input patterns. This allows us to validate interesting combinations of stimulus that might otherwise be hard to do from a UVM sequence.

• Improving Verification Productivity

In addition to managing the technical challenges of large sequence libraries, we show how to use sequences to improve verification productivity. We show how to use sequences to isolate design features for easier debug, regression management, and better coverage control. These techniques directly improve the visibility of project status to stakeholders and allow flexibility to adapt to changing schedules.

• Portable Stimulus Considerations

We show how a well-designed sequence API is vital for adoption of a Portable Stimulus workflow. Teams who are currently using portable stimulus, or are considering using it in the future, can save time and effort by ensuring upfront that their sequence library directly supports both UVM test suites and portable stimulus.

Speakers:

Mark Litterick - Verilab, Inc.

Jeff Vance - Verilab, Inc.

Jeff Montesano - Verilab, Inc.





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DVCon Europe Reception & Expo

Time: 17:30 - 19:00 | Room: Großer Saal

WEDNESDAY'S AGENDA

07:30 - 08:00	 Welcome Coffee Service Room: Großer Saal Foyer			
08:00 - 08:15	Opening Session Room: Ballsaal			
08:15 - 09:00	Keynote: Enabling Technologies and the Future of Networks - Preeti Nagarajan, Ericsson Room: Ballsaal			
09:15 - 10:30	Panel: Imagining How Artificial Intelligence Could Reshape the Verification Landscape Room: Ballsaal			
10:00 - 18:30	Exhibit Floor Open Room: Großer Saal			
10:30 - 10:45	 Attendee Break Room: Großer Saal			
10:45 - 12:15	Session 1 - UVM-1 Room: Forum 4	Session 2 - SystemC Room: Forum 5	Session 3 - Generating Stimulus Room: Forum 6	Session 4 - Advanced Verification 1 Room: Forum 7
12:15 - 13:15	Luncheon Room: Großer Saal Foyer			
13:15 - 14:45	Session 5 - PSS Room: Forum 4	Session 6 - RISC-V and Advanced ISS Room: Forum 5	Session 7 - Formal Verification Room: Forum 6	Session 8 - SOC Verification Room: Forum 7
14:45 - 15:15	 Attendee Break Room: Großer Saal			
15:15 - 16:45	Session 9 - UVM-2 Room: Forum 4	Session 10 - Emulation Room: Forum 5	Session 11 - System Level Design Room: Forum 6	Advanced Verification 2 Room: Forum 7
16:45 - 17:30	Panel: Applying the New Breed of Automotive Specific, Next-Generation Verification Technologies Room: Ballsaal			
17:30 - 18:30	Closing Session & Best Paper Award Room: Großer Saal			Thank you to our Sponsor 

Welcome & Coffee Service

Time: 07:30 - 08:00 | Room: Großer Saal Foyer

Opening Session

Time: 08:00 - 08:15 | Room: Ballsaal



Keynote: Enabling Technologies and the Future of Networks

Time: 8:15 - 9:00 | Room: Ballsaal

Speakers:

Preeti Nagarajan - Ericsson

Network traffic grows at a near exponential rate, and available spectrum to the Communications Service Providers will increase significantly. Operators will need to add 30% capacity every year while keeping both OPEX and CAPEX under control. In addition, the network architecture is further impacted by disaggregation, openness and virtualization. Ericsson Business Area Networks Wanted Position is to create highly scalable, cost competitive, modular platforms offering lowest total cost of ownership, best user experience & smooth network transformation to 5G.

Clarity in architecture, from customer need to deployment, is essential in order to increase quality in the field, with zero faults vision and reduced lead time from customer need to network deployment, while at the same time evolving networks to leverage and deliver the best in automation through pro-active network insights and analytics enabled solutions.

Product differentiation, depending on innovation and new technologies, is also to an increasing extent dependent on efficient development and delivery of fundamental enabling technologies, ranging from simple cooling solutions for a complex system all the way up to SoC and SW technologies. The digitalization of several functions on sub-system level increases the importance of the SoC in a system. As the need increases, we also see that the industry landscape supporting several enabling technologies including SoCs is consolidating.

This Keynote will delve into the dilemma of quicker innovation

needed in enabling technologies to support complex systems in a consolidating and geo-politically polarized industry landscape.

Biography: Preeti Nagarajan is Head of Strategy for Networks at Ericsson since December 2018. She is responsible for the business development of the networks operations and provides strategic direction to how the company invests in existing and future networks portfolio.

Prior to her role, she headed up R&D for multi-standard radio and indoor products, contributing to advancing the company vision through innovation, technology, and sustainable business solutions. She also led Industry Area Telecom at group level working with diverse telecom strategies, and thought leadership for next-generation technologies such as 5G.

Nagarajan joined Ericsson in 2006 as a systems engineer and trainee. She has held various leadership positions as well as worked within customer project management, strategic product management and portfolio strategy in Sweden and in Japan. Prior to Ericsson she worked with broadband access networks and was a network engineer intern at Verizon in the US.

She graduated from Madras University with a Bachelor of Engineering in Electronic Engineering. She holds a Dual Master's degree from University of North Texas and has specialization in Wireless Communication from KTH Royal Institute of Technology.

Her interests include antenna spotting, cycling, photography and singing.

Panel: Imagining How Artificial Intelligence Could Reshape the Verification Landscape

Time: 9:15 - 10:30 | Room: Ballsaal

Moderator:

Balachandran Rajendran - Dell EMC

A crowd-pleasing panel about Artificial Intelligence (AI) and Machine Learning (ML) at DVCon U.S. will be continued at DVCon Europe as chip design verification experts explore various scenarios to determine if the verification landscape needs to be modified. They will debate whether the current verification flow is equipped to handle the requirements of this emerging area estimated at more than 80 startups working on accelerator chips used across all market segments, including automotive and wireless. Further discussion will explore whether AI techniques pushing traditional CPU and GPU architectures to a different level will create an upheaval in chip

design, chip design verification and embedded software that would require a new methodology and tools.

Panelists come from such noted semiconductor companies as Arm, Dell EMC, dividiti Limited and T&VS, all of whom have AI chip development efforts under way. Audience members will be encouraged to bring questions and opinions to ensure a lively and thought-provoking panel session.

Panelists:

Dan Coley - Arm, Ltd.

Rajeev Dutt - Dimensional Mechanics, Inc.

Anton Lokhmotov - Dividiti Limited

Gabriele Pulini - Mentor, A Siemens Business

Mike Bartley - Test and Verification Solutions

Exhibit Floor Open

Time: 10:00 - 18:30 | Room: Großer Saal

Attendee Break

Time: 10:30 - 10:45 | Room: Großer Saal

Session 1 - UVM-1

Time: 10:45 - 12:15 | Room: Forum 4

Chair:

Mark Litterick - Verilab

- 1.1 **A 360 Degree View of Reusability Combatbetween UVM Callbacks and UVM Factory-A Case Study**
Vikas Billa - Intel Technology India Pvt. Ltd.

- 1.2 **EURP - Enhanced UVM Register Package**
Abhishek Jain - Qualcomm India Pvt. Ltd.

- 1.3 **Random Stimuli Models for UVM RAL**
Jacob Sander S. Andersen, Laura Montero - SyoSil ApS
Lars Viklund - Axis Communications AB

Session 2 - SystemC

Time: 10:45 - 12:15 | Room: Forum 5

Chair:

Christian Sauer - Cadence Design Systems, Inc.

- 2.1 **Integrating Parallel SystemC Simulation into Simics® Virtual Platform**
Daniel M. Mendoza - Univ. California Irvine,
Ajit Dingankar - Intel Corp.
Zhongqi Cheng, Rainer Doemer - Univ. of California, Irvine

- 2.2 **SystemC-to-Verilog Compiler: a Productivity-Focused Tool for Hardware Design in Cycle-Accurate SystemC**
Mikhail Moiseev, Roman Popov, Ilya Klotchkov - Intel Corp.

- 2.3 **Pythonized SystemC - a Non-Intrusive Scripting Approach**
Eyck Jentzsch, Rocco Jonack - MINRES® Technologies GmbH

Session 3 - Generating Stimulus

Time: 10:45 - 12:15 | Room: Forum 6

Chair:

Alexander Rath - Infineon Technologies AG

- 3.1 **A Generic Approach for Handling Sideband Signals**
Salman Tanvir - Infineon Technologies
Markus Brosch - Infineon Technologies AG

- 3.2 **The Powerful Synergy Between UVM and PSS**
Sharon Rosenberg - Cadence Design Systems, Inc.

- 3.3 **Generic Testbench/Portable Stimulus/Promotability**
Revati S. Bothe, Jesvin Johnson - Sondrel Ltd.

Session 4 - Advanced Verification 1

Time: 10:45 - 12:15 | Room: Forum 7

Chair:

Clemens Röttgermann - Exida

- 4.1 **Addressing Asynchronous FIFO Verification Challenge**
Anchal Gupta, Ashish Hari, Sulabh Kumar Khare, **Joerg Schoeppe** - Mentor, A Siemens Business

- 4.2 **Agile and Dynamic Functional Coverage Using SQL on the Cloud**
Filip Dojcinovic - Veriest Solutions Ltd.

- 4.3 **Transaction-Based Testing with OSVVM and the OSVVM Model Library**
Jim W. Lewis - SynthWorks Design, Inc.
Patrick Lehmann - PLC2 GmbH

Lunch

Time: 12:15 - 13:15 | Room: Großer Saal

Session 5 - PSS

Time: 13:15 - 14:45 | Room: Forum 4

Chair:

Andrei Vintila - AMIQ

5.1 Results Checking Strategies with the Accellera Portable Test & Stimulus Standard

Tom Fitzpatrick, **Matthew Ballance** - Mentor, A Siemens Business

5.2 Portable Stimuli Over UVM, Using Portable Stimuli in HW Verification Flow

Efrat Shneydor - Cadence Design Systems, Inc.

Slava Salnikov - Bar-Ilan Univ.

Liran Kosovizer - Texas Instruments, Inc.

Shlomo Greenberg - Ben Gurion University

5.3 Designing a PSS Reuse Strategy

Matthew Ballance - Mentor, A Siemens Business

Session 6 - RISC-V and Advanced ISS

Time: 13:15 - 14:45 | Room: Forum 5

Chair:

Matthias Bauer - Infineon Technologies

6.1 Gathering Memory Hierarchy Statistics in QEMU

Clement Deschamps - GreenSocs Ltd, CNRS/Grenoble INP/UJF

Frédéric Pétrot - Univ. Grenoble Alpes

Mark Burton - GreenSocs Ltd.

Eric Jenn - IRT Saint-Exupéry

6.2 Open Source Solution for RISC-V Verification

Mikhail Chupilko, **Alexander Kamkin**, Alexander

Protsenko - Ivannikov Institute for System Programming of the RAS

6.3 Automate and Accelerate RISC-V Verification by Compositional Formal Methods

Yean-Ru Chen, **Cheng-Ting Kao**, Yi-Chun Kao, Tien-Yin

Cheng, Chun-Sheng Ke, Chia-Hao Hsu - National Cheng Kung Univ.

Session 7 - Formal Verification

Time: 13:15 - 14:45 | Room: Forum 6

Chair:

Anamaria Hutuleac - NXP Semiconductors

7.1 Semi-Formal Reformulation of Requirements for Formal Property Verification

Katharina Ceesay-Seitz, Hamza Boukabache, Daniel

Perrin - CERN - European Organization for Nuclear Research

7.2 Retrascope: Open-Source Model Checker for HDL Descriptions

Alexander Kamkin, Mikhail Lebedev, **Sergey Smolov** - Ivannikov Institute for System Programming of the RAS

7.3 ISO 26262:2018 Fault Analysis in Safety Mechanisms

Jörg Grosse, Mark Hampton, Sergio Marchese, Neil

Rattray - OneSpin Solutions GmbH

Jörg Koch - Renesas Electronics Europe GmbH

Alin Zagardan - Renesas Electronics America

Session 8 - SOC Verification

Time: 13:15 - 14:45 / Room: Forum 7

Chair:

Harry Foster - *Mentor, A Siemens Business*

8.1 Overcoming Challenges in SoC RTL Verification of USB Subsystem

Tijana R. Mistic - *Elsys Eastern Europe d.o.o.*
Marko J. Mistic - *Univ. of Belgrade*

8.2 Enabling Digital Mixed-Signal Verification of Loading Effects in Power Regulation using SystemVerilog User-Defined Nettype

Alvaro Caicedo, Sebastian Fritz - *Texas Instruments, Inc.*

8.3 Covering the Last Mile in SoC-Level Deadlock Verification

Jef Verdonck, **Konstantinos Liatakis**, Khaled Nsaibia - *u-blox AG*
Dhruv Gupta, Sagar Dewangan, Tarun Upadhyay,
HarGovind Singh, **Roger Sabbagh** - *Oski Technology, Inc.*

Attendee Break

Time: 14:45 - 15:15 / Room: Großer Saal

Session 9 - UVM-2

Time: 15:15 - 16:45 / Room: Forum 4

Chair:

Uwe Simm - *Cadence Design Systems, Inc.*

9.1 UVM Based Hardware/Software Co-Verification of a HW Coprocessor via Host Execution Techniques

Francois Cerisier - *Aedvoices Consulting*
Arnaud Grasset - *Thales Research and Technology*

9.2 Customizing UVM Agent to Support Multi-Layered TDM & Protocols

Amit Pessach - *Veriest Solutions Ltd.*

9.3 Methodology for Checking UVM VIPs

Milan Vlahovic - *Veriest Solutions Ltd.*

Session 10 - Emulation

Time: 15:15 - 16:45 / Room: Forum 5

Chair:

Mark Burton - *GreenSocs*

10.1 Leveraging Hardware Emulation to Accelerate SoC Verification in Multi-Physics Automotive Simulation Environment Via the Functional Mock-up Interface

Pierre-Guillaume Le Guay, Henrique Vicente De Souza,
Caaliph Andriamisaina, Emmanuel Molina Gonzalez,
Tanguy Sassolas - *CEA-LIST: Lab. for Integration of Systems and Technology*

10.2 Developing Dynamic Resource Management System in SoC Emulation

Sunchang Choi, **Sangwoo Noh**, Seonghee Yim, Seonil Choi - *Samsung Electronics Co., Ltd.*

10.3 A Novel Performance Evaluation Methodology using Virtual Prototyping and Emulation

Woojoo Kim, Hyunjae Woo, Jongmin Lee, Seonil Brian Choi - *Samsung Electronics Co., Ltd.*

Session 11 - System Level Design

Time: 15:15 - 16:45 / Room: Forum 6

Chair:

Karsten Einwich - *COSEDA Technologies*

11.1 SysML Based Architecture Definition and Platform Generation Flow

Ralph G3rgen, Erwin de Kock - *NXP Semiconductors*

11.2 Development of Flexi Performance Analysis Platform for MultiSoC Networking Systems

Srinivasan Reddy Devarajan, Anant Raj Gupta - *Intel Corp.*

11.3 A Mixed-Signal System Design Methodology using SystemC-AMS for Automotive Audio Power Amplifiers

Skule Pramm, Joen Westendorp, Quino Sandifort - *NXP Semiconductors*

Session 12 - Advanced Verification 2

Time: 15:15 - 16:45 | Room: Forum 7

Chair:

Raik Brinkmann - *OneSpin Solutions*

12.1 Unified Test Writing Framework for Pre and Post Silicon Verification

Rahulkumar Patel, Pablo Cholbi, Sivasubrahmanya Evani, Raman K - *Analog Devices, Inc.*

12.2 Processing Deliberate Verification Errors During Regression Quis Custodiet Ipsos Custodes / Who Will Check the Checkers?

Alastair Lefley, Roger Witlox, Clemens Süßmuth - *ams AG*
Thomas Ziller, Kawe Fotouhi - *Cadence Design Systems, GmbH*

12.3 Don't Forget the Protocol! A CDC Protocol Methodology to Avoid Bugs in Silicon

Abdelouahab Ayari, Sukriti Bisht, Sulabh K. Khare, Ashish Hari, Kurt Takara - *Mentor, A Siemens Business*

Attendee Break

Time: 16:30 - 16:45 | Room: Großer Saal

Panel: Applying the New Breed of Automotive Specific, Next-Generation Verification Technologies

Time: 16:45 - 17:30 | Room: Ballsaal

Moderator:

Paul Dempsey - *Tech Design Forum*

The Automotive ISO 26262 standard specifies rigorous verification flows. To date, existing technologies have been used to meet this challenge. This is evolving as verification tools and methodologies, such as formal verification, portable stimulus, accelerated fault simulation and Electronic System Level (ESL), drive next-generation automotive verification.

A safety-critical verification flow meets requirements set by functional safety standards such as ISO 26262, defining a design and verification process for safety-critical hardware projects and setting rules for a design's robustness. Applying these standards using traditional tools adds months onto a typical development flow, while still not delivering to these exacting requirements. Companies are innovating with automotive safety as a consideration, leveraging state-of-the-art technologies and abstract methodologies to accelerate and increase the quality of automotive flows.

Formal verification, Portable Stimulus, tools for system optimization and next-generation fault analysis are examples of these new approaches that make sense in the ISO 26262 world. Methodology evolutions, including a shift to ESL, also help. This panel will examine these techniques and their use today in leading automotive flows and consider the most effective approaches.

Attendees can expect a lively panel about technologies and advanced systems available to meet the stringent safety-critical industry standards. They will attempt to identify what's lacking for thorough verification, no matter what the application.

Panelists:

Dr. Ashish Darbari - *Axiomise Ltd.*
Dave Kelf - *Breker Verification Systems, Inc.*
Bill Bunton - *Intel Corp.*
Jamil Mazzawi - *Optima Design Automation*

Closing Reception & Best Paper Award

Time: 17:30 - 18:30 | Room: Großer Saal

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EVOLUTION DAY

31 OCTOBER 2019 | MUNICH | GERMANY

SystemC Evolution Day 2019

Thursday, 31 October

Time: 08:30 - 17:30 | Room: Forum 8

The fourth SystemC Evolution Day is a full-day, technical workshop on the evolution of SystemC standards to advance the SystemC ecosystem. In several in-depth sessions, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for inclusion in Accellera/IEEE standards.

SystemC Evolution Day is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance SystemC standards.

Organization team:

- Oliver Bell, *Intel, Corp. (Chair)*
- Martin Barnasconi, *NXP Semiconductors*
- Andrew Stevens, *Infineon*
- Ola Dahl, *Ericsson*
- Philipp A. Hartmann, *Intel, Corp.*
- Volkan Esen, *Infineon*
- Ingo Feldner, *Bosch*
- Tran Nguyen, *ARM*
- Manfred Thanner, *NXP Semiconductors*
- Jerome Cornet, *ST*

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08:30 - 09:00	 Welcome Coffee Service - Hosted by Accellera
09:00 - 09:30	Introduction and SystemC Working Groups Standardization Update
09:30 - 10:15	SystemC and Digital Twin: Good Match or Not? <i>Martin Barnasconi, NXP</i>
10:15 - 10:45	 Coffee Break - Hosted by Accellera
10:45 - 12:30	Simulation, Kernel Technology, Tracing
10:45 - 11:15	Pushing the Limits of Standard-Compliant Parallel SystemC Simulation <i>Rainer Doemer, Univ. of California, Irvine</i>
11:15 - 12:00	Synchronizing Simulators, and Save and Restore <i>Mark Burton, GreenSocs</i>
12:00 - 12:30	Improving the Usability and Performance of Tracing in SystemC <i>Rauf Salimi, Philipp Hartmann, Intel</i>
12:30 - 13:45	Lunch Break - Courtesy of Accellera; Cadence; Mentor, a Siemens Business; and Synopsys
13:45 - 15:00	TLM, Interoperability, Metrics
13:45 - 14:10	Methodology for Defining Bus Specific Programmer's View Extensions to TLM2.0 <i>Umesh Sisodia, Prince Arora, CircuitSutra Technologies Pvt Ltd</i>
14:10 - 14:35	Follow-up on GP Extension Standard, Clock and Reset SC Standard <i>Joachim Geishauser, NXP</i>
14:35 - 15:00	SystemC Modeling Metrics <i>Ingo Feldner, Tim Kraus, Bosch</i>
15:00 - 15:30	 Coffee Break - Hosted by Accellera
15:30 - 17:00	Model Creation, High Level Synthesis
15:30 - 16:15	Re-envisioning CCI Inspection <i>Bill Bunton, Philipp Hartmann, Intel; Michael Lebert, Ola Dahl, Ericsson</i>
16:15 - 17:00	Advanced Assertion Checking in SystemC High-Level Synthesis Flows <i>Bob Condon, Intel</i>
17:00 - 17:30	Wrap-up & Closing

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Exhibit Hours:

Tuesday, 29 October ----- 10:00 - 19:00

Wednesday, 30 October ----- 10:00 - 18:30

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ATTENDEE BREAKS

Location: Großer Saal
Tuesday, 29 October

11:30 – 11:45

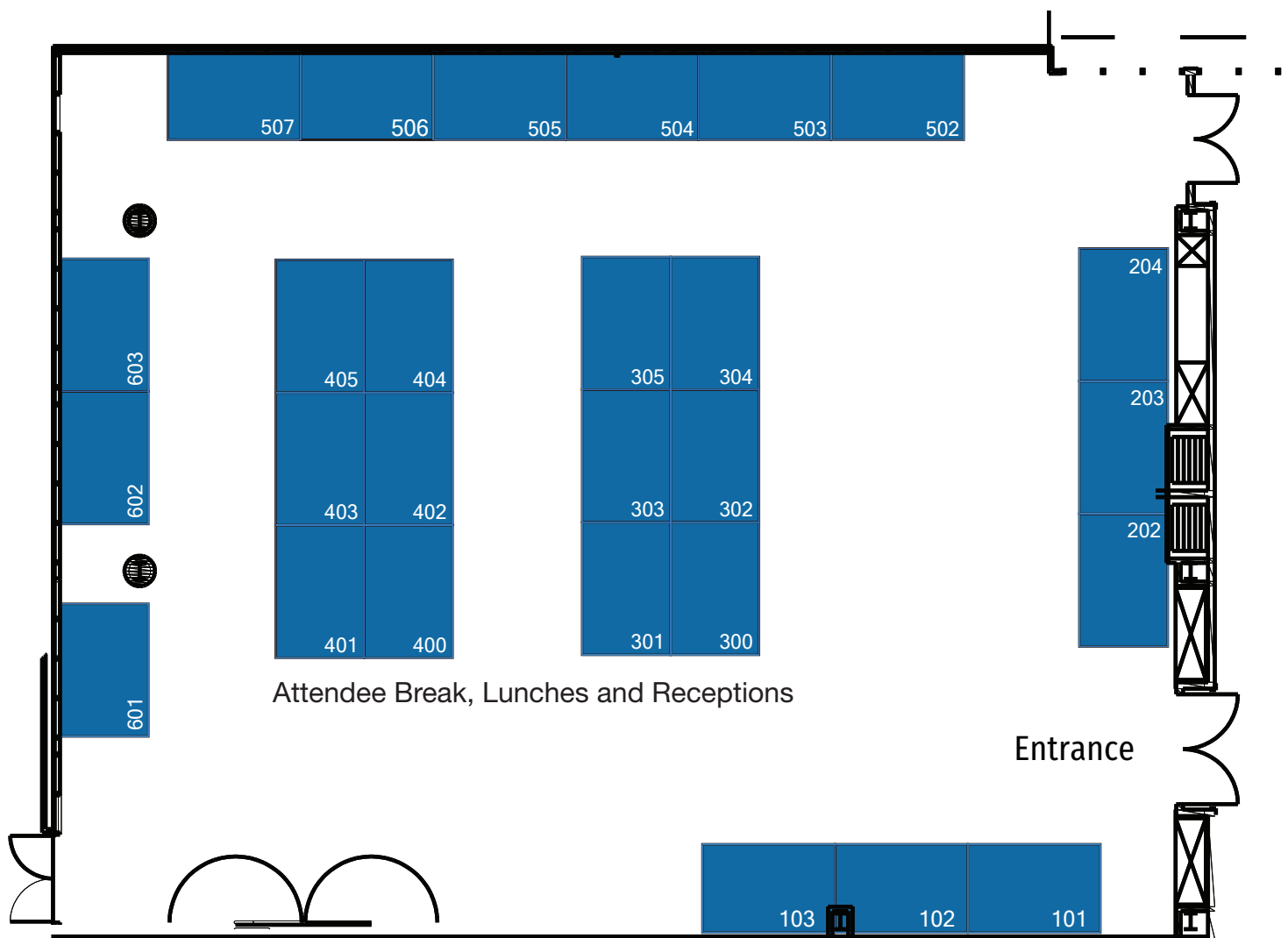
15:45 – 16:00

Wednesday, 30 October

10:30 – 10:45

14:45 – 15:15

EXHIBIT FLOOR



EXHIBITORS



Agnisys, Inc.

Booth: 301 | www.agnisys.com

Agnisys Inc. is a leading supplier of Electronic Design Automation software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for system-on-chip and intellectual property enabling faster design, verification, firmware, and validation. Agnisys is based in Boston, Massachusetts, with R&D centers in the United States and India.



Aldec, Inc.

Booth: 405 | www.aldec.com

Established in 1984, Aldec is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design and Mixed-Language Simulation (VHDL, Verilog, SystemVerilog/UVM), FPGA-based Hardware-Assisted Verification, SoC and ASIC Prototyping, Emulation, Design Rule Checking, Clock Domain Crossing, VIP Transactors, Requirements Lifecycle Management, Embedded Development Kits, High-Performance Computing/Acceleration, DO-254 Functional Verification and Military/Aerospace solutions.



AMIQ EDA srl

Booth: 503 | www.amiq.com

AMIQ EDA provides tools - DVT Eclipse IDE, DVT Debugger Add-On, Verissimo Linter, and Specador Documentation Generator - that enable design and verification engineers increase the speed and quality of new code development, simplify legacy code maintenance, accelerate language and methodology learning, and improve source code reliability. Working with 100+ companies in 30+ countries, AMIQ EDA is recognized for its high quality products and customer service responsiveness.



ANKASYS

ANKASYS

Booth: 402 | www.ankasys.com

ANKASYS is a microelectronics design and verification services company covering complete RTL to GDS flow and FPGA implementation. ANKASYS has a track record of providing SystemVerilog and UVM based verification services covering IEC61508, DO254 and ISO26262 safety related applications. ANKASYS also provides cost-effective training services in ASIC/FPGA design and verification with hands-on lab exercises on PC or directly on FPGA.



Avery Design Systems, Inc.

Booth: 302 | www.avery-design.com

A leader in Verification IP providing robust models, compliance testsuites, and services for PCI Express, USB/xHCI, UFS/UFSHCI, NVMe/f, SATA Express, SATA, UniPro, Soundwire, Sensewire, CSI/DSI, HDMI, DP, eMMC, SDIO, DDR4/LPDDR4, HBM, HMC, ONFI/Toggle, CAN FD, LIN, FlexRay, and ACE/AXI3/AXI4/AHB. A leader in verification tools. SimXACT automatically eliminates X bugs in RTL and gate-level simulation. ResetOPT minimizes reset/retention design overhead.



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Booth: 204 | www.brekersystems.com

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Cadence Design Systems, Inc.

Booth: 103 | www.cadence.com

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CircuitSutra Technologies Pvt Ltd.

Booth: 401 | www.circuitsutra.com

Circuitsutra is an Electronics System Level (ESL) design IP & Services company, headquartered in India, having development centres in Noida & Bangalore, and serves the customers worldwide. It enables customers to adopt advanced methodologies based on C, C++, SystemC, TLM, IP-XACT, UVM-SystemC, SystemC-AMS. Its core competencies include virtual prototype (development, verification, and deployment), Architecture & Performance modelling, co-simulation, co-emulation, HLS, SoC & System verification.



COSEDA Technologies GmbH

Booth: 101 | www.coseda-tech.com

COSEDA Technologies is a leading provider of system-level software solutions for complex electronic hardware and software products. We offer our customers the latest modeling and simulation technologies to cost-effectively manage new concepts for their innovative, complex and safety-critical products.



Doulos

Booth: 202 | www.doulos.com

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ElectraIC provides D&V services especially for Advanced Verification for Safety Critical Digital Hardware Development. ElectraIC can work with you in your DO-254 projects, support you as an independent verification team for your DAL-A/B/C product verifications or help you deploying methods, tools and templates required in a DO-254 certification process like configuration management, requirements traceability, verification procedures and records, etc.



Fraunhofer IIS/EAS

Booth: 505 | www.eas.iis.fraunhofer.de

Major aspects of the work of Fraunhofer Institute for Integrated Circuits IIS with its division Engineering of Adaptive Systems EAS are the design of reliable microchips and complex electronic systems in leading-edge semiconductor technologies as well as the corresponding design methods. Mastering challenges like increasing integration density calls for our new design methods and functional system verification approaches.

GRAPHCORE

GRAPHCORE

Booth: 303 | www.graphcore.ai

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L&T Technology Services

Booth: 403 | www.ltts.com

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The MathWorks GmbH

Booth: 203 | www.mathworks.com

MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development. MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields.



Mentor, A Siemens Business

Booth: 507 | www.mentor.com

Mentor, A Siemens Business, has pioneered technology to close the design and verification gap to improve productivity and quality of results. Catapult High-Level Synthesis for C-level verification and PowerPro for power analysis; Questar for simulation, low-power, VIP, CDC, Formal and support for UVM and Portable Stimulus; Velocir for hardware emulation and system of systems verification, unified with the VisualizerT debug environment.



OneSpin Solutions GmbH

Booth: 502 | www.onespin.com

OneSpin Solutions, a leader in formal verification, is creating the industry's most advanced formal platform, encompassing agile design evaluation, coverage-driven ABV, and automated DV apps. The world's leading electronics companies partner with us to pursue design perfection in areas where reliability really counts: safety-critical verification, SystemC/C++ HLS code analysis, and FPGA equivalence checking. OneSpin: Making Electronics Reliable



Oski Technology, Inc.

Booth: 603 | www.oskitechnology.com

Oski reduces our clients' overall project costs and improve their tapeout confidence with our comprehensive formal verification sign-off services. Oski is changing the course of semiconductor verification by formally signing-off high-risk blocks that are impossible to verify with simulation. Drop by our booth to learn how our pioneering formal verification methodologies can greatly reduce your bug-escape and schedule-slip risks.



PRO DESIGN Electronic GmbH

Booth: 305 | www.prodesign-europe.com

PRO DESIGN is a leading provider of FPGA-based Prototyping systems. PRO DESIGN's product family proPFGA is a very flexible high-performance FPGA system which is mainly used for ASIC Prototyping and pre-silicon software development. The modular concept of the proPFGA system, consisting of different motherboards, FPGA modules, daughter boards and interconnects allows the user to adjust it for almost any type of application.



Real Intent, Inc.

Booth: 304 | www.realintent.com

Real Intent provides intent-driven static signoff tools to accelerate early functional verification of digital designs, leading the industry in precision, performance, and capacity. Its product capabilities for eliminating complex design failure modes include: clock domain crossing sign off from RTL through gate level, including multimode CDC; reset domain crossing sign off; and advanced RTL linting and analysis.

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Booth: 401 | www.synopsys.com

Synopsys is the Silicon to Software partner for innovative companies developing electronic products and software applications. Synopsys' Verification Continuum combines best-in-class technology, including simulation, verification IP, emulation, advanced debug, static and formal verification, prototyping and virtual prototyping, with advanced methodologies enabling users to address rapidly escalating SoC complexity, accelerate time-to-market and bring products to market sooner.



Truechip Solutions Pvt. Ltd.

Booth: 400 | www.truechip.net

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Veriest Veriest Solutions Ltd.

Booth: 504 | www.veriests.com

Veriest is a design house providing ASIC/FPGA engineering services. Our clients are industry leaders and startups developing high-end chip technology. With headquarters in Israel and R&D centers in Serbia and Hungary, our 100+ engineers have made their mission to provide customers with superior solutions that include architecture design, design implementation for digital/mixed-signal designs, system modelling, functional and formal verification and embedded software.

Verifyter

Booth: 102 | www.verifyter.com

Verifyter develops and sells PinDown, an automatic debugger of regression failures. Using machine learning, PinDown quickly identifies the bad code and validates the debug analysis by making the failing test pass again.



Yonga Technology Microelectronic R&D

Booth: 506 | www.yongatek.com

YONGATEK is design and verification company. It provides design services to national and international companies for ASIC/FPGA designs, UVM and RISC-V based SoC verifications projects. It has also vast experience in verifying hardware requirements according to RTCA DO-254 standards. YONGATEK has accomplished important R&D products like to Multiple Object Video Tracker, H264 Video Codec IP, Digital Moving Map and ADAS (Advanced Driver Assistant System).

DVCON EUROPE 2019 EXHIBITORS*





This image shows a full page of blank, lined paper. It features approximately 20 evenly spaced horizontal blue lines across its entire width. The background is a solid off-white color, typical of standard notebook or legal pad paper. There are no margins, text, or other markings present.

NOTES



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