DV methodology to model scalable/reusable component to handle IO delays/noise/crosstalk in Multilane DDR PHY IF

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***Abstract*— The demand for increased data throughput has resulted in aggressive migration to advanced process technology nodes in order to support higher operating frequencies. As a result of the smaller geometries in advanced technology nodes, the effect of cross coupling at interconnects and buses, delay/distortion of signals traveling on high-speed interconnects need to be analyzed to ensure signal integrity. DDR system consists of Memory Controller, PHY and DRAM devices connected externally on the system board. Information transfer between the controller and off-chip DRAM is handled by the PHY layer of a DDR interface. In order to ensure good data-integrity of the system in silicon, the DV infrastructure needs to be enhanced. The effect of silicon artefacts like cross-coupling, noise, delay, distortion etc. need to be modelled in order to thoroughly verify the functionality of DDR-PHY. Delay Network Module (DNM) has been developed to enable robust verification.**

Keywords*— *Delay Network Model (DNM), Design Verification(DV), Universal Verification Component (UVC), System on Chip(SoC), Double Data Rate(DDR), Dual In-line Memory Module(DIMM), Design Under Test (DUT).

I. INTRODUCTION

DNM is integrated between PHY and external DRAM memory model (Figure 1) to mimic silicon, board artefacts. The DNM is completely parameterized and configurable to replicate the behavior of different DRAM devices in order to enable re-use across multiple projects/protocols. DNM consists of Duty Cycle (DC) Modulator, IO Delay Module, and Cross talk (X talk) Module, and Setup/Hold Time (IO Damage) Module.

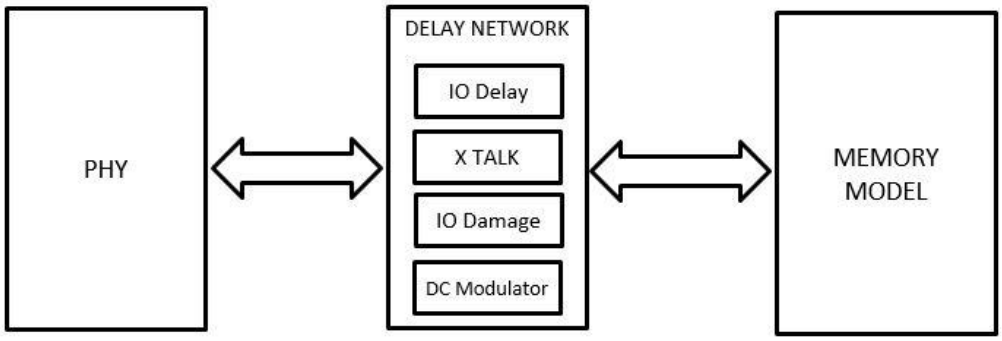

Figure 1: DV architecture with delay network UVC

II. FUNCTIONAL ARCHITECTURE

A. IO Delay Module

The PHY consists of Control Path (Clock & Command Address Bus) and Data Path (DQ and DQ Strobe). The contributing factors for the IO delays are as follows.

a. Placement and routing of DRAM in SoC ➔ Transport Delay.
b. External placement of DRAM ➔ Board Delay.
c. DDR placement on DIMM ➔ Relative delay between DQ/DQS & Clock.

Randomized delay value, based on PHY and system specifications, is generated by DNM for all control and data (bi-directional) signals. An example of delayed_ram_ip_C is depicted in Figure 2. DNM has provision for controlling the parameterization of each signal in any bus independently. Additionally, the delay values can be changed dynamically during simulation to facilitate rigorous stress testing. The delay on the data and data strobe signals can be configured independently for both read and write paths.

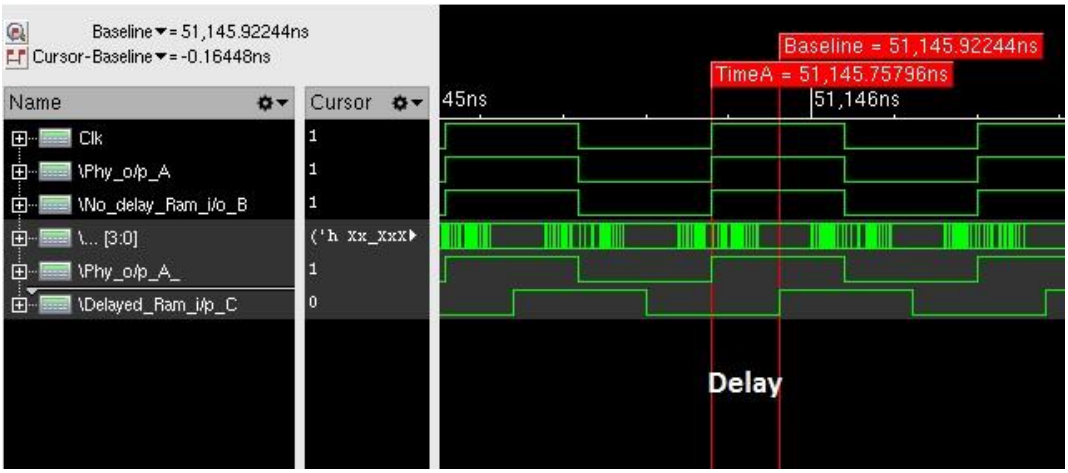

Figure 2 : Delay Insertion

B. Cross Talk Module

The PHY data-bus valid window gets impacted due to cross-talk between different data-bus signals. The cross talk is modelled based on the analysis of the current and neighboring bit transitions. The calculation is based on mathematical expression which will be user-defined and depends on the application where PHY is used and noise sensitivity of the system. The Damaged_Ram_i/p_C signal (Figure 3) reflects the effect of Cross talk module.

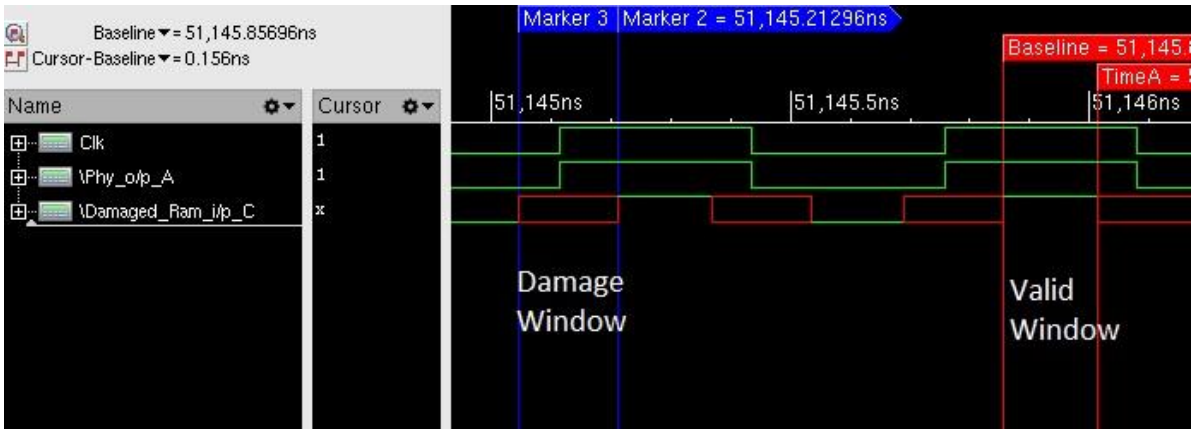

Figure 3 : Damage due to cross talk

C. Setup/Hold Time Module

PHY provides clock along with data and control lines to memory. Apart from cross talk, the valid window reduction can occurs due to Voltage reference (Vref) fluctuation effect etc. Change in valid window width against the permissible limit will result in setup/hold time violation. To replicate this behavior during simulation and to stress test the setup and hold time violation the DNM corrupts the data using MVL(Multi-Value Levels) signaling - 'X' or 'Z' on both the edges of the valid window. The extent of corruption depends on the eye-opening specifications.

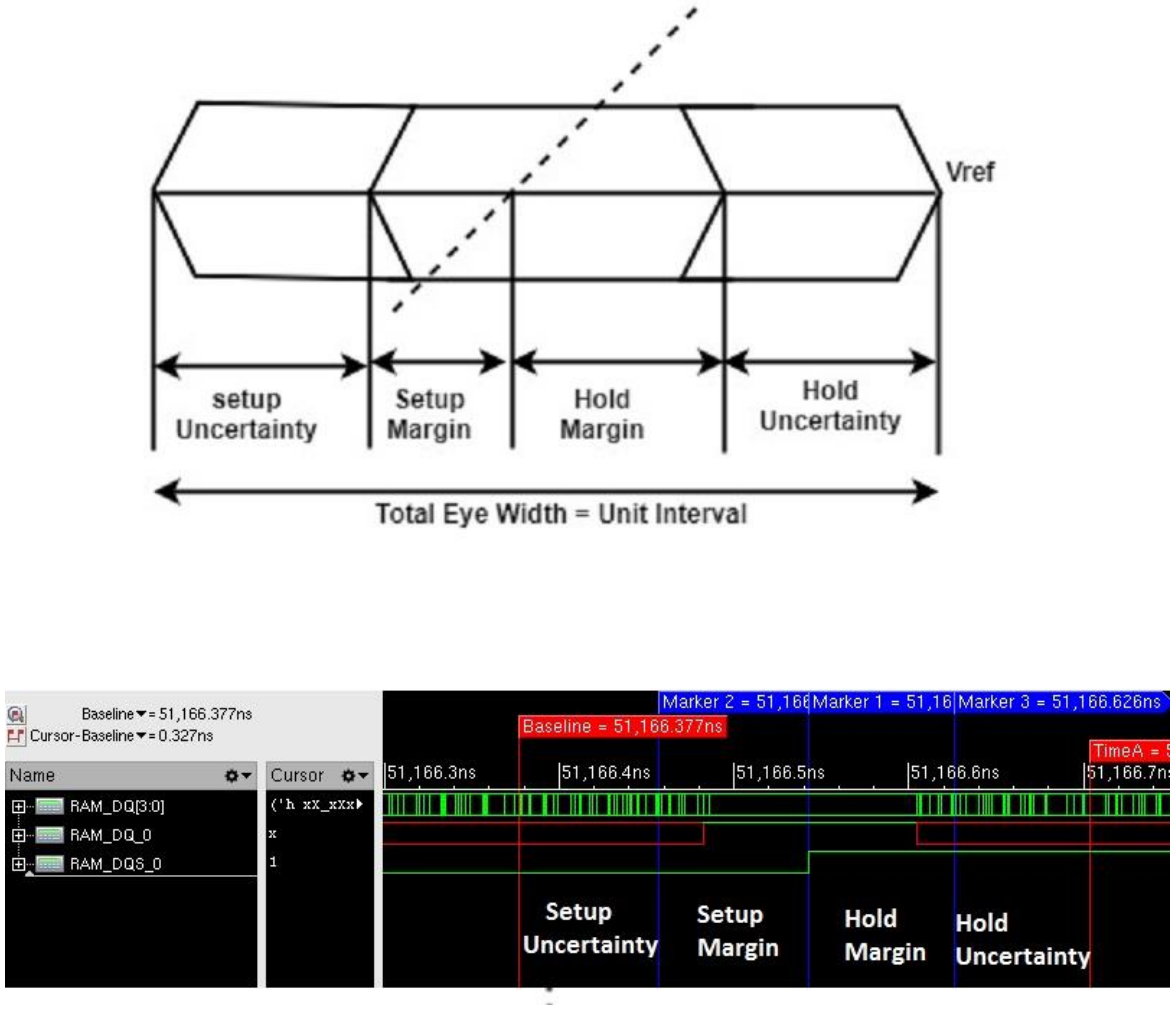

Figure 4 : Setup hold time module

D. Duty Cycle Modulation

In order to stress-test the data sampling algorithm during read/write operations, the duty cycle of data bus and data strobe is randomized. This enables robust and comprehensive verification of the read and write data calibration features with different duty cycle settings. DNM provides control to change the duty cycle on the fly in addition to configurable values support. DNM supports independent controls for read and write paths to facilitate independent and robust testing.

Figure 5 : Duty cycle modulation

III. CONCLUSION

With shrinking time to market timelines, the DV needs to be done with a smarter and modular approach. DNM acts as a plug and play module and plays a crucial role in expediting the DV with real time scenarios. Randomization and parameterization of the delay/damage ranges and other critical parameters results in engineers spending their valuable time on stressing more on Design w.r.t interface timing and debug, rather than reinventing the wheel for different DRAM devices. DNM is interoperable with all the individual bits of the data line. Detailed log messages enhance the ease of debug. Centering timing checkers and functional coverage reinforces the confidence on the role played by DNM and quality of design as well.

DNM had uncovered quite a few critical bugs in the design. For Ex:

- Calculated delay for one of the rank was applied to the other rank by the DUT. The DNM applied randomized unique delays for different ranks and this resulted in uncovering the DUT issue.
- The PHY applied DQ delay code to DM bus even when the DM /DBI bus was disabled for calibration.
- PHY not asserting delay line overflow bit even with maximum delay.
- DUT failing to calibrate the valid centring position when the damage on both edges were randomized according to spec.

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