# Don't Forget the Protocol! A CDC Protocol Methodology to Avoid Bugs in Silicon

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# Introduction

• CDC issues: 2<sup>nd</sup> most common reason for silicon re-spins

#### - Structural CDC Verification

- Use of synchronizer to essentially reduce the probability of metastability
- Good understanding in industry (part of some industry standards like DO-252)
- Widely used in industry

#### - Functional CDC Verification

- Synchronizers has to meet functional requirements (CDC Protocols)
- No large awareness in industry





### If CDC Protocol Verification is Skipped

- Structural CDC checking alone is not enough
- Risks
  - Lose of data
  - Propagation of metastability ( $\rightarrow$  corruption of data)





#### **Risks: Loss of Data**

- Case of a 2DFF Synchronizer Protocol Violation
  - TX Data stable for less than two (NUM\_CYCLES) clock cycles



### **Risks: Propagation of Metastability**

- Case of a Protocol Violation
  - Mux-enable is asserted and
  - TxData is changing in the critical time window of the receive clock RxClk
- Rx Data Tx Data Tx Control Rx Clk Data-Mux (DMUX) Synchronizer **Rx clock** Mux-enable Tx Data

- What happen
  - Metastability could be propagated
  - Corruption of RxData



### **CDC Protocol Verification is a MUST !!**



















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### **Challenges with Existing Methodology**

- Setup design for Formal, Simulation
  - Effort, time for translating CDC design setup to both environments
- Debug effort to review firings in Formal, Simulation
  - Technical expertise of both environments
  - Setup translation errors cause false violations
- Correlating assertions results in CDC vs. Formal vs. Simulation

   Coverage, review of CDCs is cumbersome for complex crossings
- No re-utilization of benefits, efforts of Formal, Simulation
  - Simulation: More intuitive to understand but coverage issues
  - Formal: Offers exhaustive proofs but capacity, constraint issues



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### **Proposed Verification Methodology**

- Perform static CDC analysis
- Generate:

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SYSTEMS INITIATIVE

- Assertions for synchronizer protocols
- Setup for Formal
- Setup for Simulation
- Validate assertions in formal
  - Formal analysis using generated setup
- Validate assertions in simulation
  - Simulate design using generated setup
  - Only formal non-proven assertions



### **Verification Methodology**

- Automated design setup for Formal & Simulation
  - Static analysis setup exported to formal constraints
- Reduced formal firing debug effort
  - Avoid debug of unconstrained formal firings
  - Promote non-proven assertions to simulation
- Formal & simulation results correlated to CDC paths
  - Improved review/debug of CDC paths & assertion/coverage results
  - Avoids manual aggregation/correlation of assertion results
- Leverage formal efforts in simulation
  - Prune formally proven assertions from simulation





## **Correlated Results View**

- Formal, Simulation results correlated to CDC
  - Enables faster review of CDC paths, coverage closure
  - No manual correlation of assertion results required



### **Existing vs. New Methodology** (Formal)



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\* Formal Coverage = ((Failed Assertions + Proven Assertions) / Total Assertions) \* 100 15

### **Existing vs. New Methodology** (Simulation)





# Conclusion

- Dynamic CDC Protocol Verification is critical
  - CDC bugs missed if synchronizer protocols not validated
- Proposed methodology helps achieve faster design closure
  - Seamless to adopt
  - Significant reduction in verification time, effort
  - Reduced chances of error thru automated setup generation
  - Overcomes challenges of Formal, Simulation methods
  - Enables efficient utilization of both methods





## Thank you!

#### Questions?





## **Existing Verification Methodology**

- Perform static CDC analysis
- Generate assertions for protocols
   of synchronizers
- Validate assertions in formal
  - Setup design for formal
  - Perform formal analysis
- Validate assertions in simulation
  - Setup design for simulation
  - Simulate design





# Setup, Debug Challenge (1)

• Example: False two DFF synchronizer protocol firing in Formal

- Data stability check firing due to change in value of 'ctrl\_in' signal



# Setup, Debug Challenge (2)

- False firing due to incomplete setup for Formal
  - Constraint specified on input signal 'ctrl\_in' during static CDC
  - Setup issue: Stable constraint missing from formal setup
  - Debug effort required for false firing caused due to incomplete setup



## **Correlation Challenge**

- Formal, Simulation environments very different from CDC •
- Complex synchronizers have multiple assertions ۲

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- Treated as separate entities in Formal, Simulation, but relate to a single CDC sync
- Correlating results is cumbersome, time consuming
- Errors during result correlation can lead to missed bugs



