This presentation focusses on:

- Multiple approaches: fixed board delays, configurable board delays
- Modeling external board delays using UVM (Universal Verification Methodology) for single and multi-channel environment.
- Demonstration of external board delay modeling using LPDDR (Low Power DRAM) and HBM (High Bandwidth Memory)

### Board Delay Model Encapsulated within Memory System

- **SoC/ System/ Controller**
- **Board Delay Model**
- **Memory Model**

### UVM Architecture with Memory VIP

- **Environment**
- **Agent**
- **Driver**
- **Monitor**
- **Virtual Interface**
- **DRAM Model**
- **Board Delay Interface**
- **DUT**

### Board delay architecture with UVM approach

- **Environment**
- **Agent**
- **Driver**
- **Monitor**
- **Virtual Interface**
- **DRAM Model**
- **Board Delay Interface**
- **DUT**

### Board Delay Interface from Memory Controller Perspective

- **Not Visible from Memory Controller side**
- **Virtual Interface**
- **DRAM Interconnect**
- **Board Delay Interface**
- **Memory Model**

### Board Delay Interface from Memory Model Perspective

- **Not Visible from Memory Model side**
- **Virtual Interface**
- **DRAM Interconnect**
- **Board Delay Interface**
- **Memory Model**

### Interconnect class code

Introduced two additional components in VIP:

- **External Board Delay Interface**: Pin compatible interface with original memory interface
  - Installed inside original memory interface
- **Intermediate Interconnect Class** (DRAM Interconnect):
  - Connects board delay interface to original interface
  - Provides a mechanism to add desired delays on each pin
- **Board Delay Interface from Memory Controller Perspective**
  - Not visible from Memory Model side

### Board Delay Interface from Memory Controller Perspective

- **Not Visible from Memory Controller side**
- **Virtual Interface**
- **DRAM Interconnect**
- **Board Delay Interface**
- **Memory Model**

### Experiments & Results

- **Differential signals skew**: Provided a skew of 0.25UI (Unit Intervals) between differential signals, clk_fibck_c, wbmp_tividx_c and rdpp_tridx_c
- **Board Delay Interface Connecting DRAM Interconnect to Memory Model**
- **Board Delay Interface from Memory Controller Perspective**

### Summary

- **Don’t delay catching bugs**: Using UVM based architecture to model external board delays
- **Amit Paunikar, Saurabh Arya, Vikas Makhija & Shailly Khare**
- **Synopsys India Pvt. Ltd.**

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**Per transaction delays**: Provided different delays during different transactions by reconfiguring these delays in every transaction.

**DQ skew**: We monitored the data sampling on both reading and writing by applying data skew between individual DQ pins.

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**Demonstrated UVM based model to generate random board delays on each pin of a memory-oriented interface.**

- These delays are independent and entirely user configurable.
- These methods could be extended to multi-rank and multi-channel environments also.
- We have examined this model on a parallel memory protocol, but this approach can be extended to other parallel as well as serial protocols as future work.
- The board delay model can be modeled for multiple VIPs such as DDR, LPDDR 2/3/4, HBM, USB, PCIE etc.