DESIGN & VERIFICATION DVCON 2014 CONFERENCE & EXHIBITION

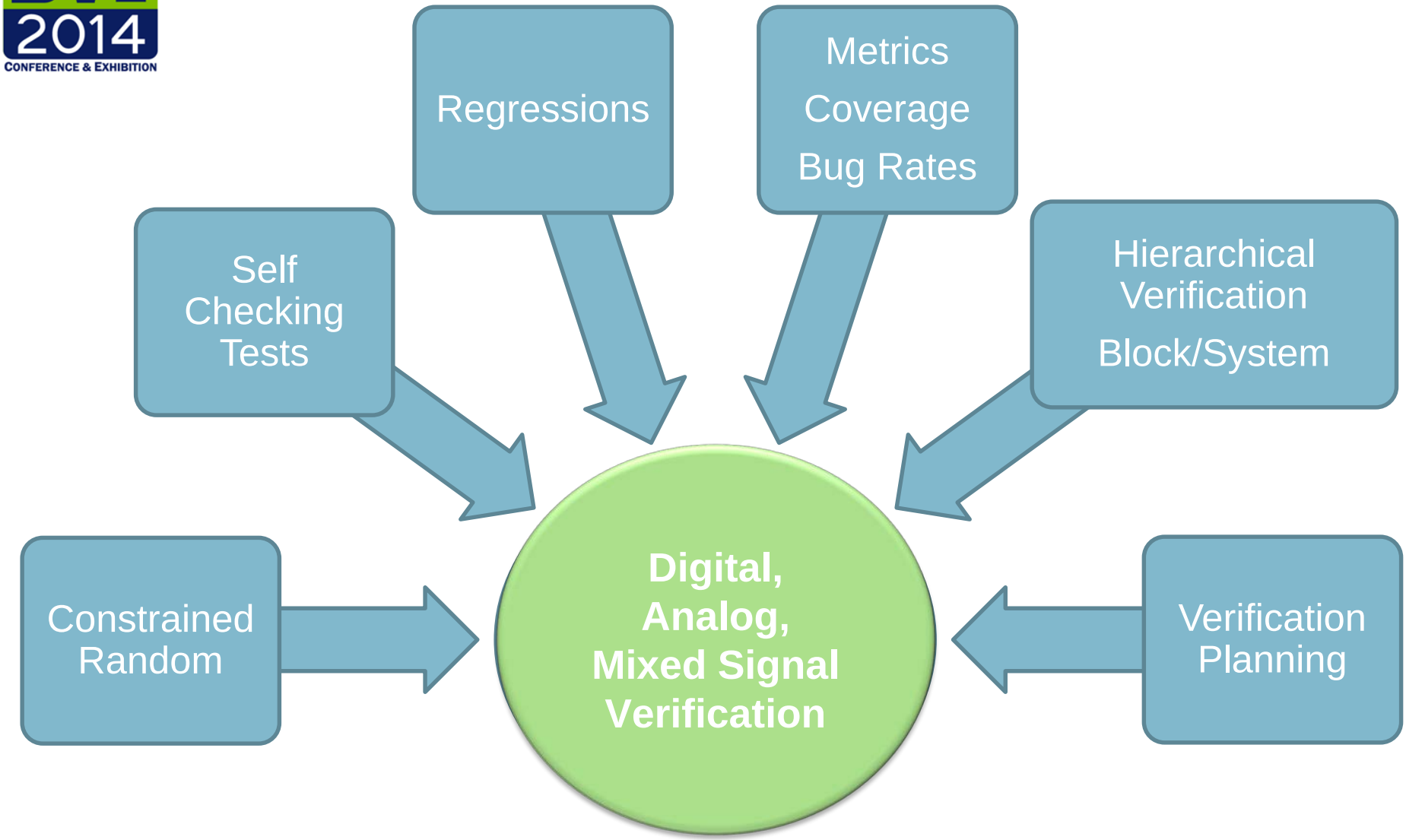
Digitizing Mixed Signal Verification:
Digital Verification Techniques Applied to Mixed Signal and Analog Blocks on the LMA Project

David Brownell and Courtney Schmitt
Analog Devices, Inc.

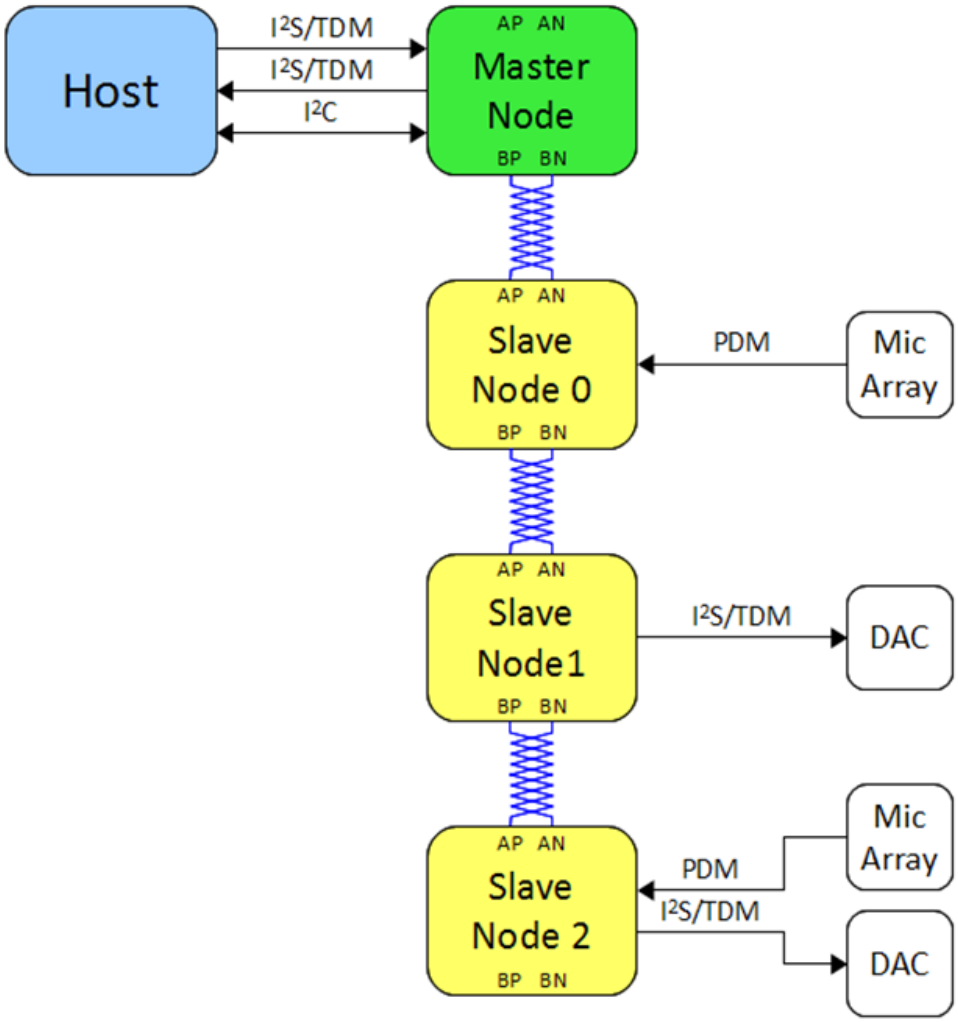
ANALOG DEVICES

Agenda

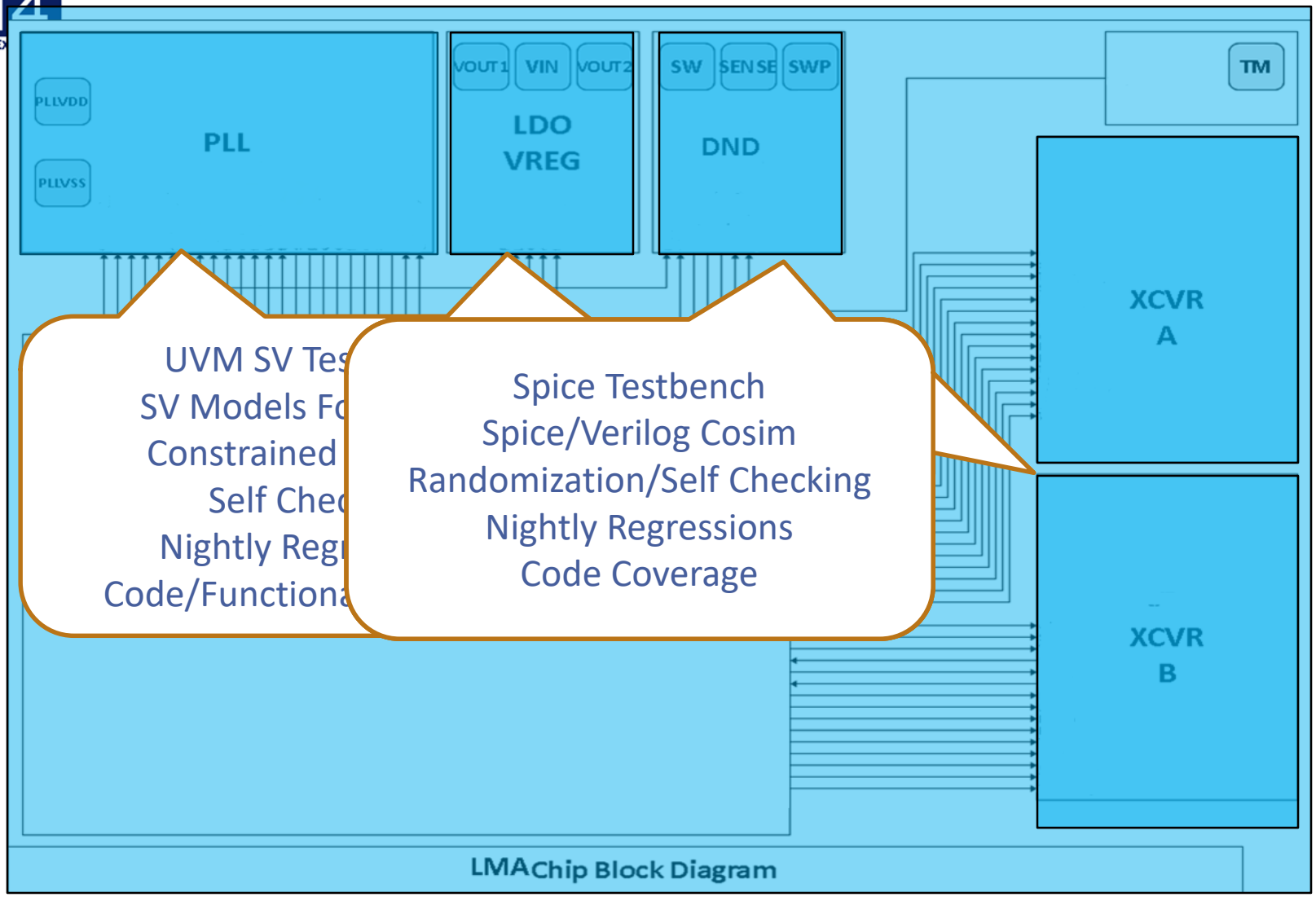
- Intro to LMA Project and MDV
- Specific Digital DV Techniques used on LMA
- System Level Cosim
- Results & Lessons Learned


Regressions
Metrics
Coverage
Bug Rates
Self
Checking
Tests
Hierarchical
Verification
Block/System
Constrained
Random
Digital,
Analog,
Mixed Signal
Verification
Verification
Planning

LMA System Overview



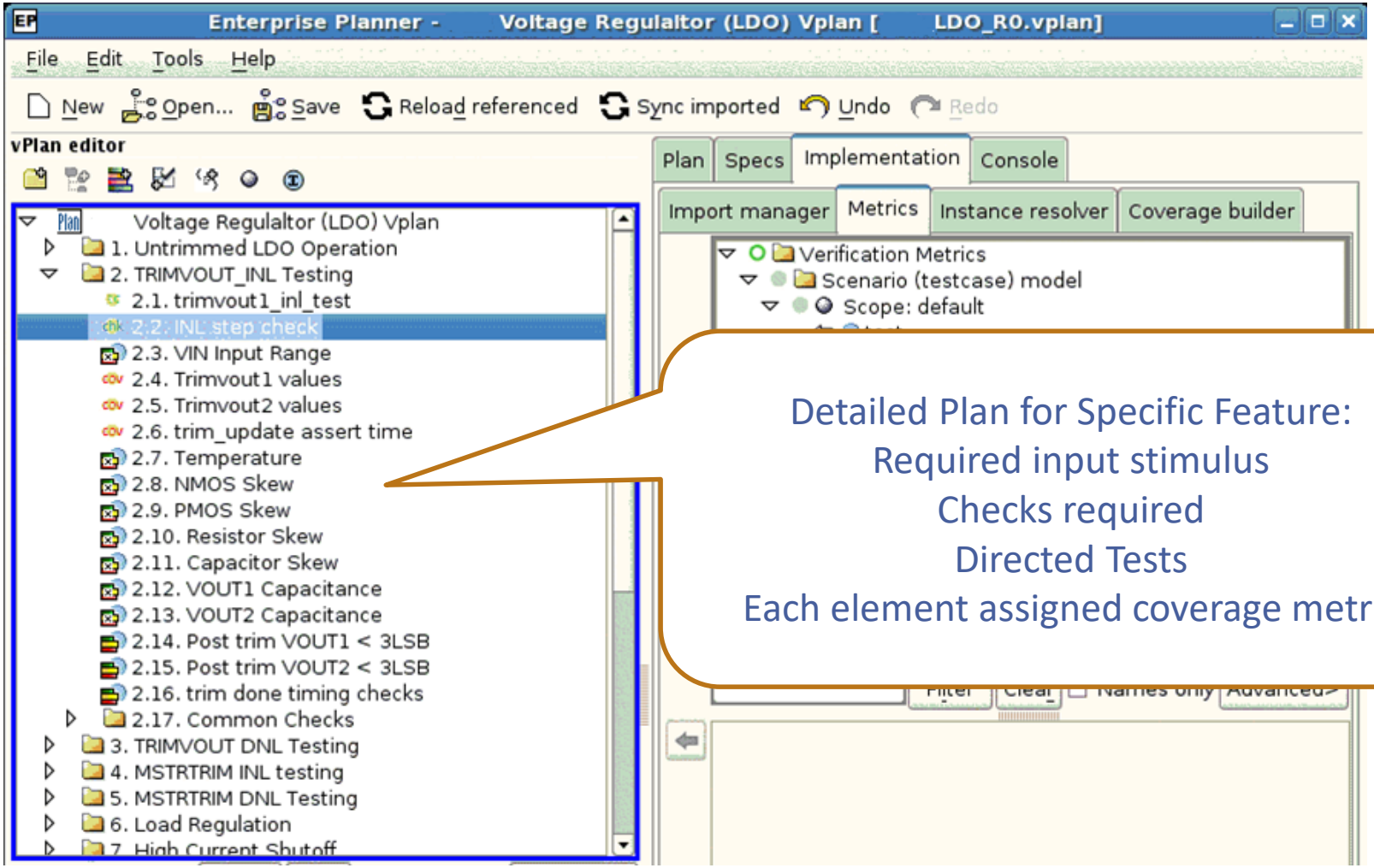
Hierarchical Verification



LDO

- Executable Verification Plan
- SPICE and Self Checking Tests
- SPICE & Functional Coverage

LDO Verification Plan



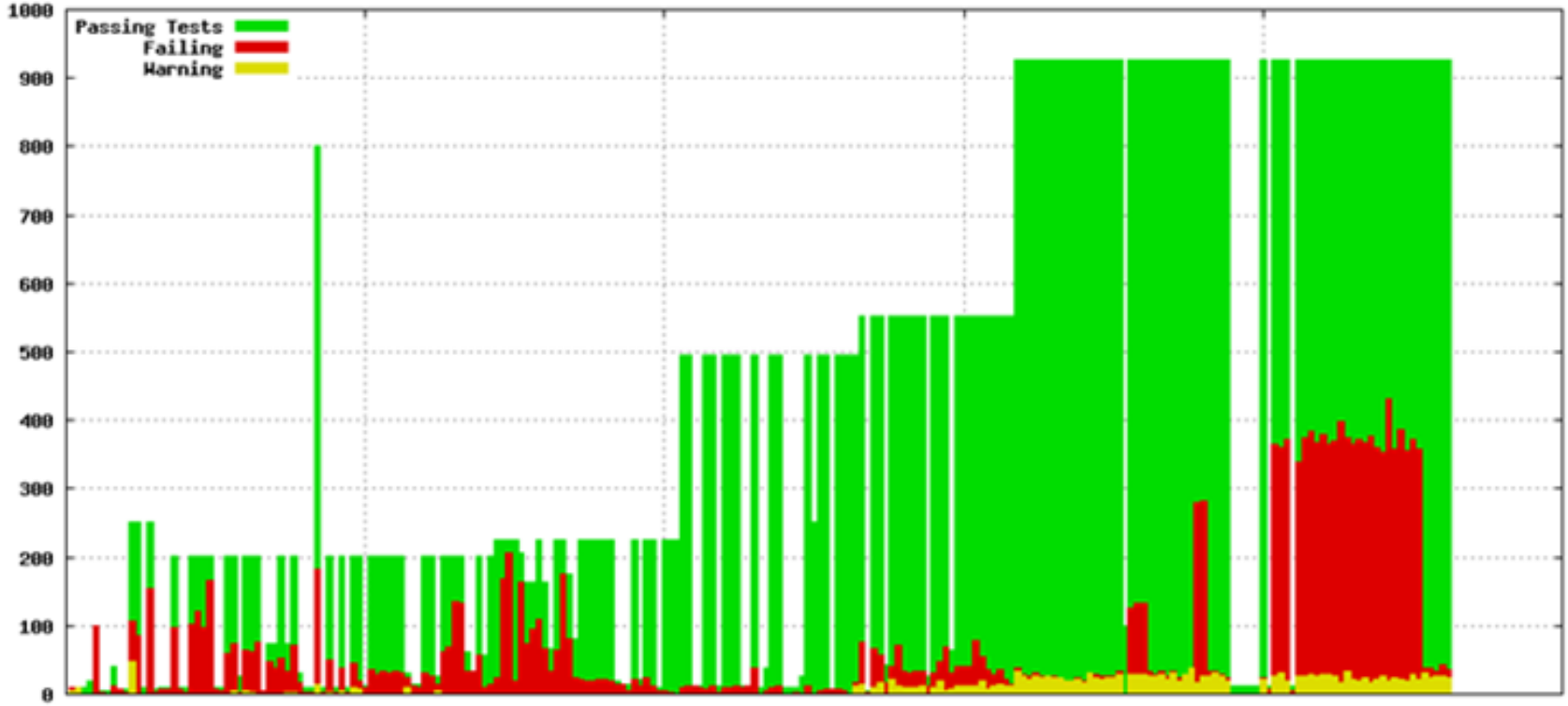
Spice & Self Checking Tests

- Most significant change in DV Methodology for LMA
- Internal Spice Simulator and control language
- Converted former visual checks into checks run for every test

```
//ponrstb assertion checks
ponrstb_assertion_time = find(voltage(ponrstb) > 1.0);

vout1_at_ponrstb = value(vout1, ponrstb_assertion_time);
if (vout1_at_ponrstb < 1.62) then print “ERROR :: Vout1 < 1.62V when ponrstb asserts”
```

- Harder to code than digital checks but worth the effort
- After identifying real issues designers quickly become comfortable with automated regression methodology

vreg_tb Regression Summary



Date	Start_Time	User	Simulator	RP	Simulated Time	Time Elapsed	Result	Coverage
04_06_13	23_59_07	brownell	nc	N	0.000000s	7h,13m,38s	TT= 926, PT= 890, FT= 13, WT= 23	Not Collected
04_05_13	23_59_07	brownell	nc	N	0.000000s	13h,3m,5s	TT= 926, PT= 883, FT= 16, WT= 27	Not Collected
04_04_13	23_59_08	brownell	nc	N	0.000000s	8h,25m,33s	TT= 926, PT= 893, FT= 8, WT= 25	Not Collected
04_03_13	23_59_07	brownell	nc	N	0.000000s	14h,5m,33s	TT= 926, PT= 889, FT= 14, WT= 23	Not Collected

Spice & Functional Coverage

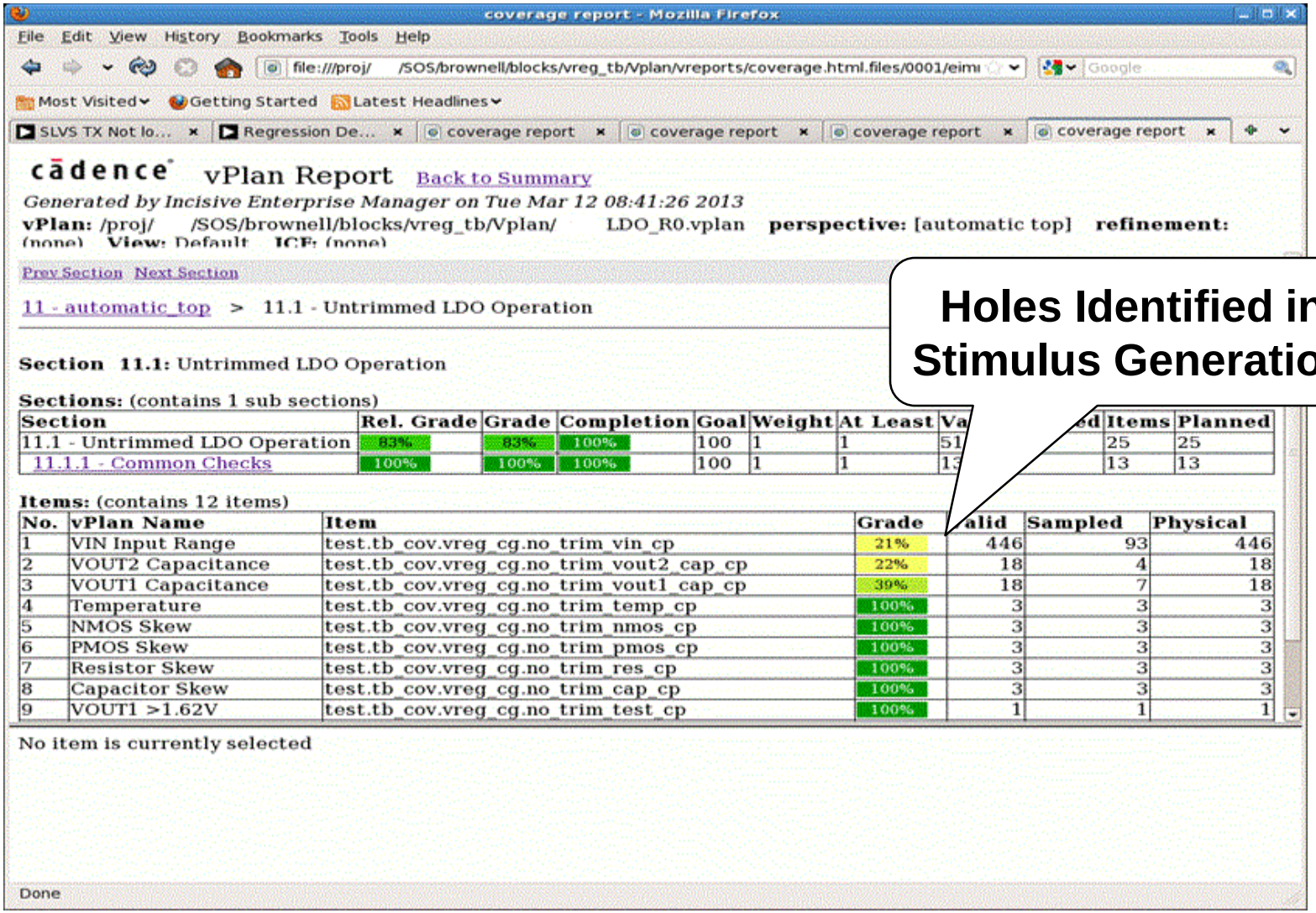
- use print commands to log metrics in spice run logs
- SystemVerilog Program parses log
  - Collect Functional Coverage Metrics
  - Input Stimulus, Checkers Called, States Observed

```
typedef enum {NO_SKEW, F, T, S }
                    skew_t;

covergroup cov_cg;
skew_cp : coverpoint skew {
   ignore_bins ign_bins = {NO_SKEW};
}
```

```
//Check for SKEW
if (str_match(line, "SKEW")) begin
  if (line[8] == "F") skew = FAST;
  else if (line[8] == "S") skew = SLOW;
  else if (line[8] == "N") skew = TYP;
end

cov_cg.sample();
```

- Full code available in paper

Annotated Vplan: Summary View Live Snapshot into Verification Status



PLL

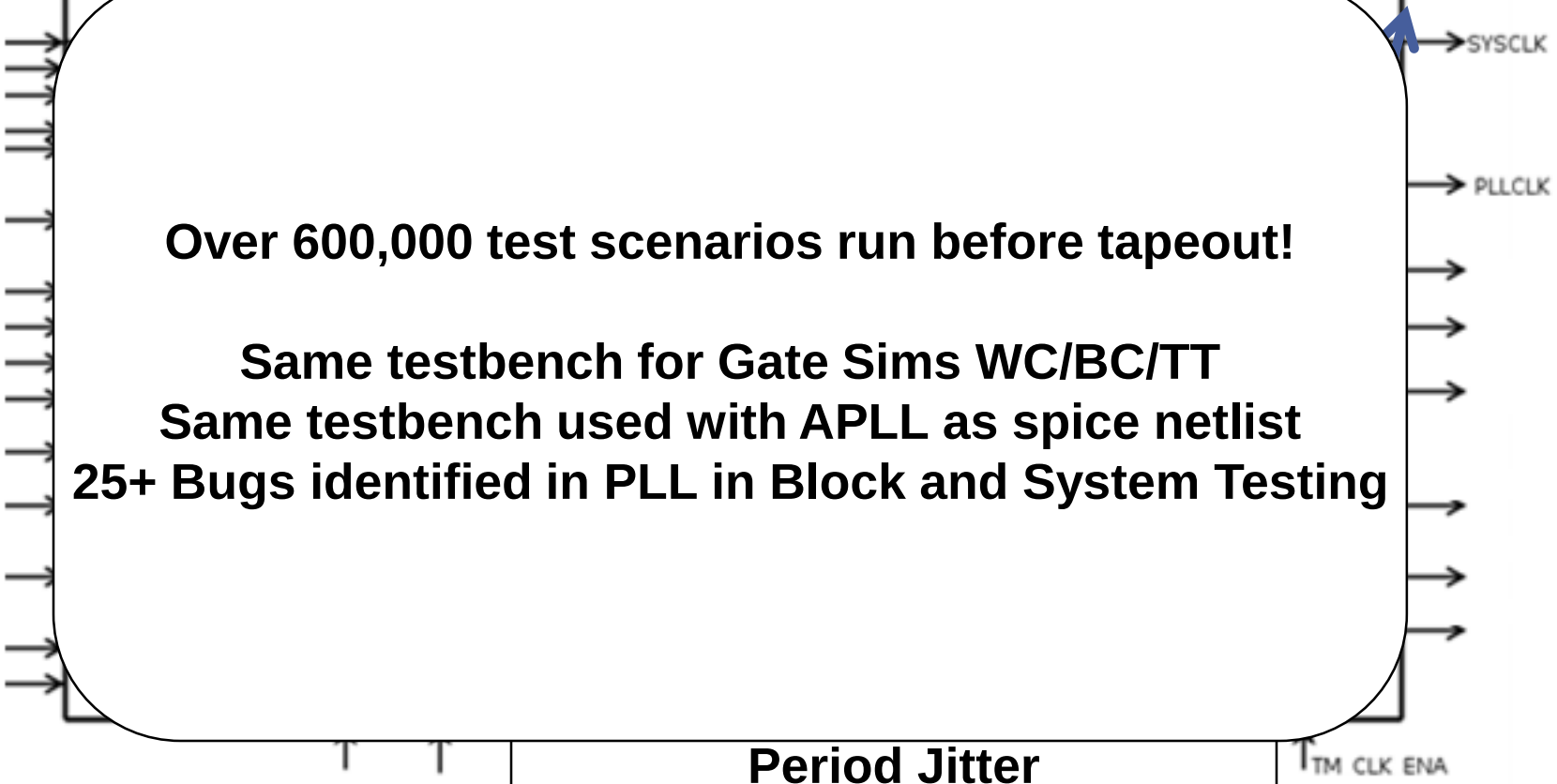
- UVM Testbench
- System Verilog RNM models

PLL BLOCK LEVEL VERIFICATION

ndomization:

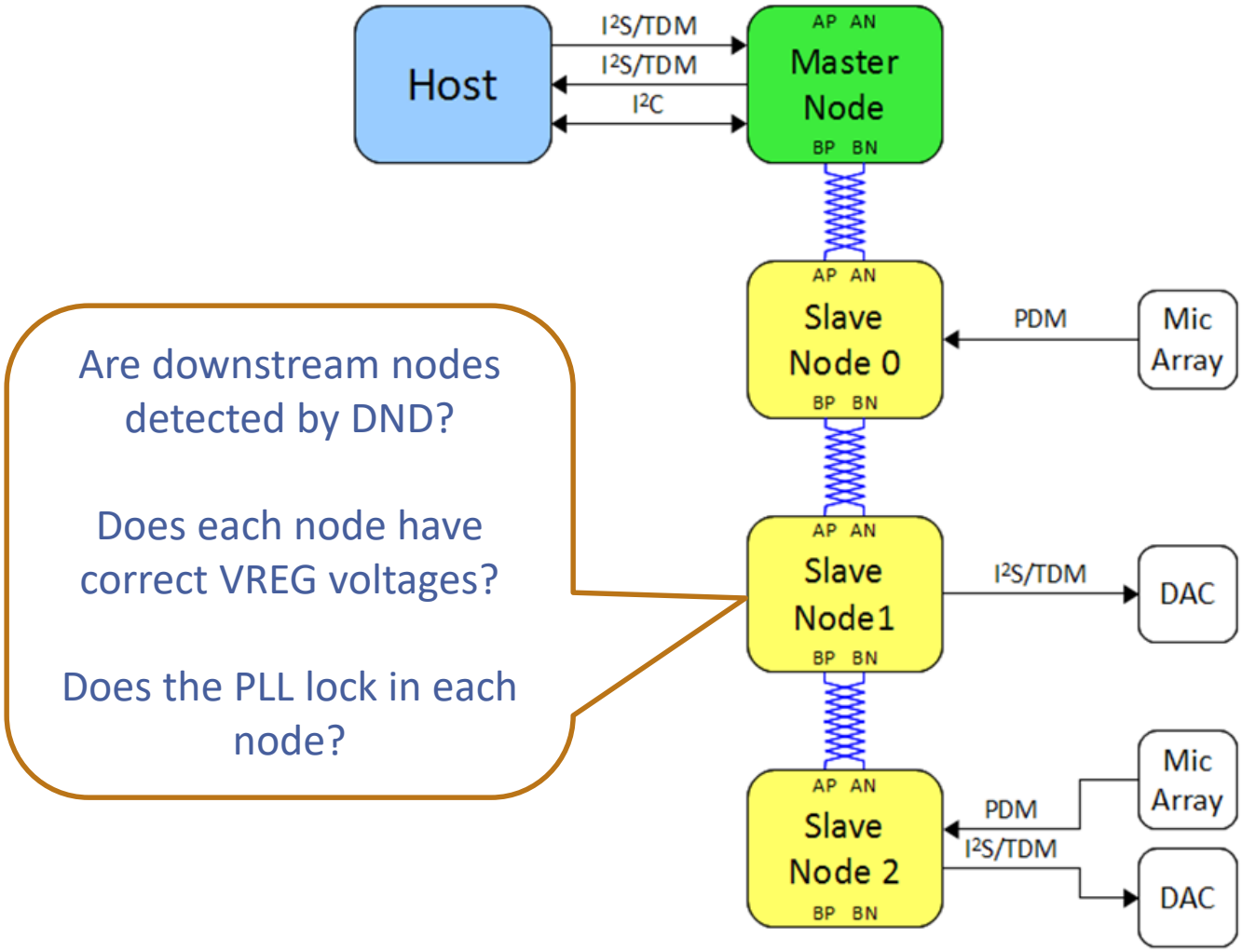
Over 600,000 test scenarios run before tapeout!

Same testbench for Gate Sims WC/BC/TT
Same testbench used with APLL as spice netlist
25+ Bugs identified in PLL in Block and System Testing

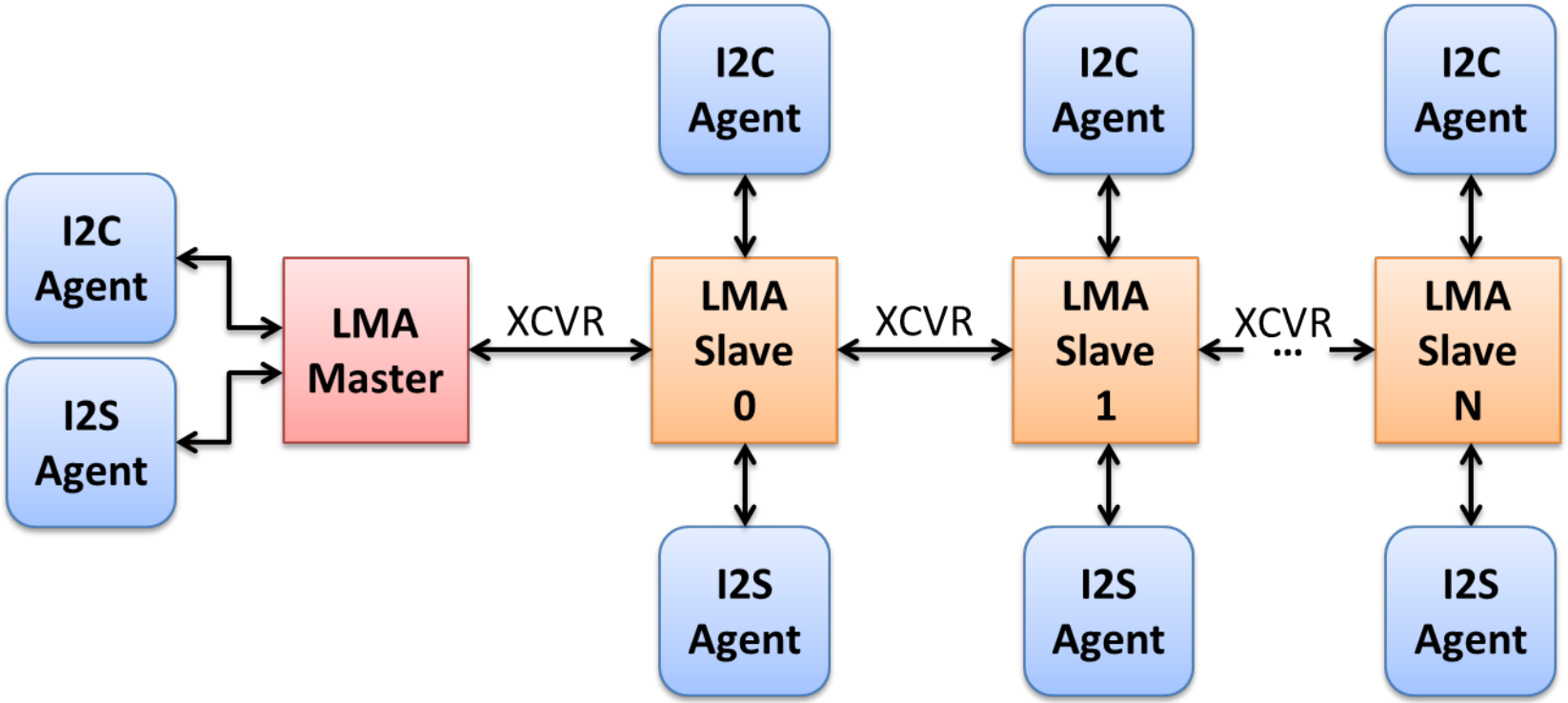


Period Jitter
TIE Jitter

System Level Verification



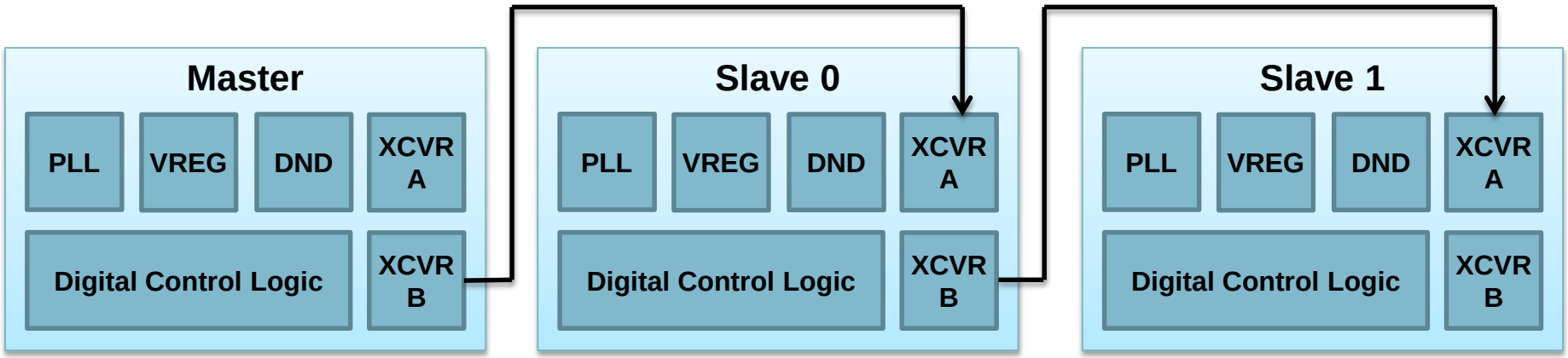
System Level UVM Testbench



System Level Cosim

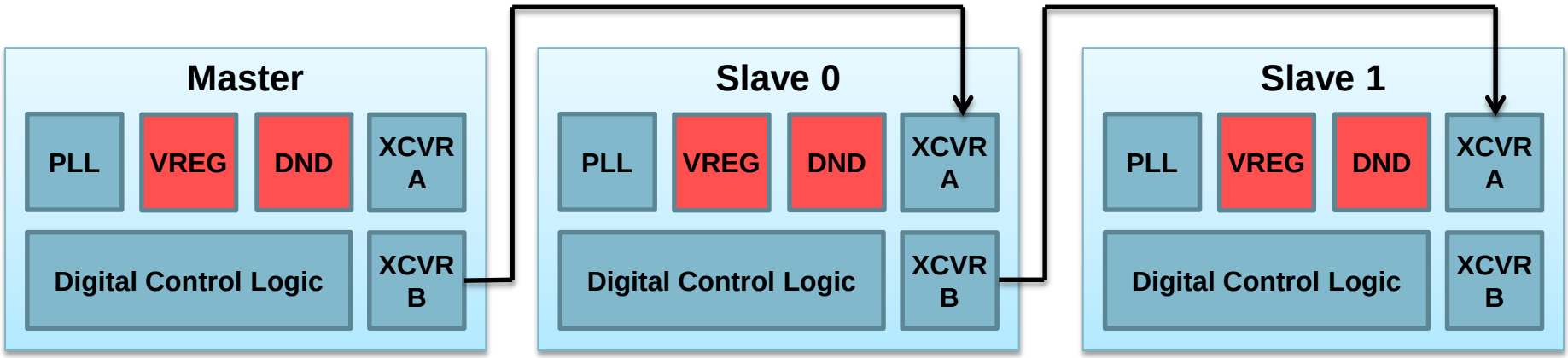
- Cadence Spectre AMSD
  - Control which blocks use SV models vs. Spice netlists
  - Fast spice simulation to balance speed and accuracy tradeoff

- 3 Main Goals:
  - Replicate issues seen in early rev of silicon
  - Provide a platform to debug and test out design fixes
  - Further stress AMS blocks to expose any other potential issues



Goal 1: Replicate Silicon Issues

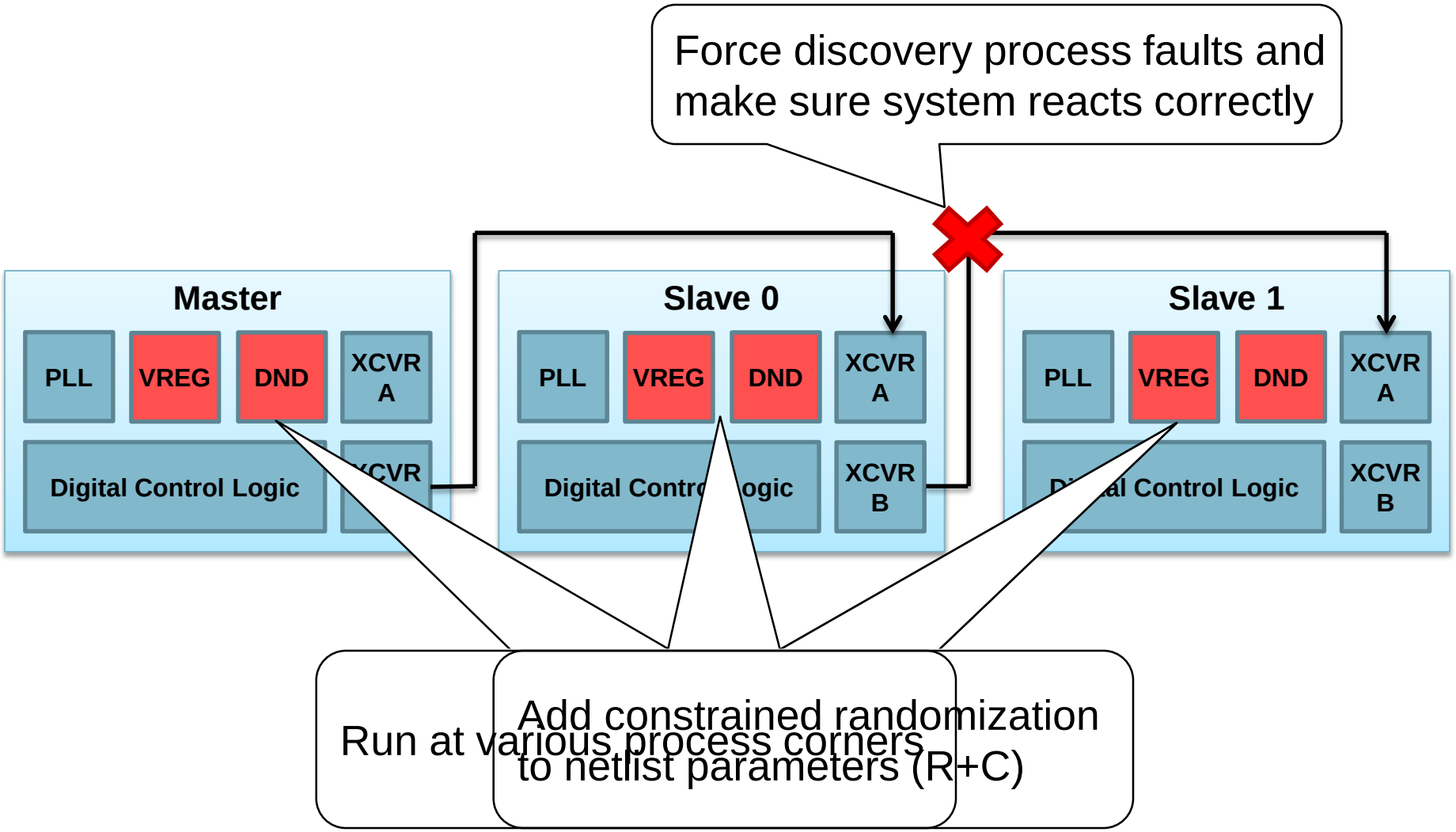
- Discovery process bugs
  - Nodes were not detected and powered up correctly without software workarounds
- Cosim with spice netlists for VREG and DND
  - Able to replicate silicon bug, which was related to interactions between nodes
  - Would not have been caught with block-level simulations



Goal 2: Debug and Fix Failure

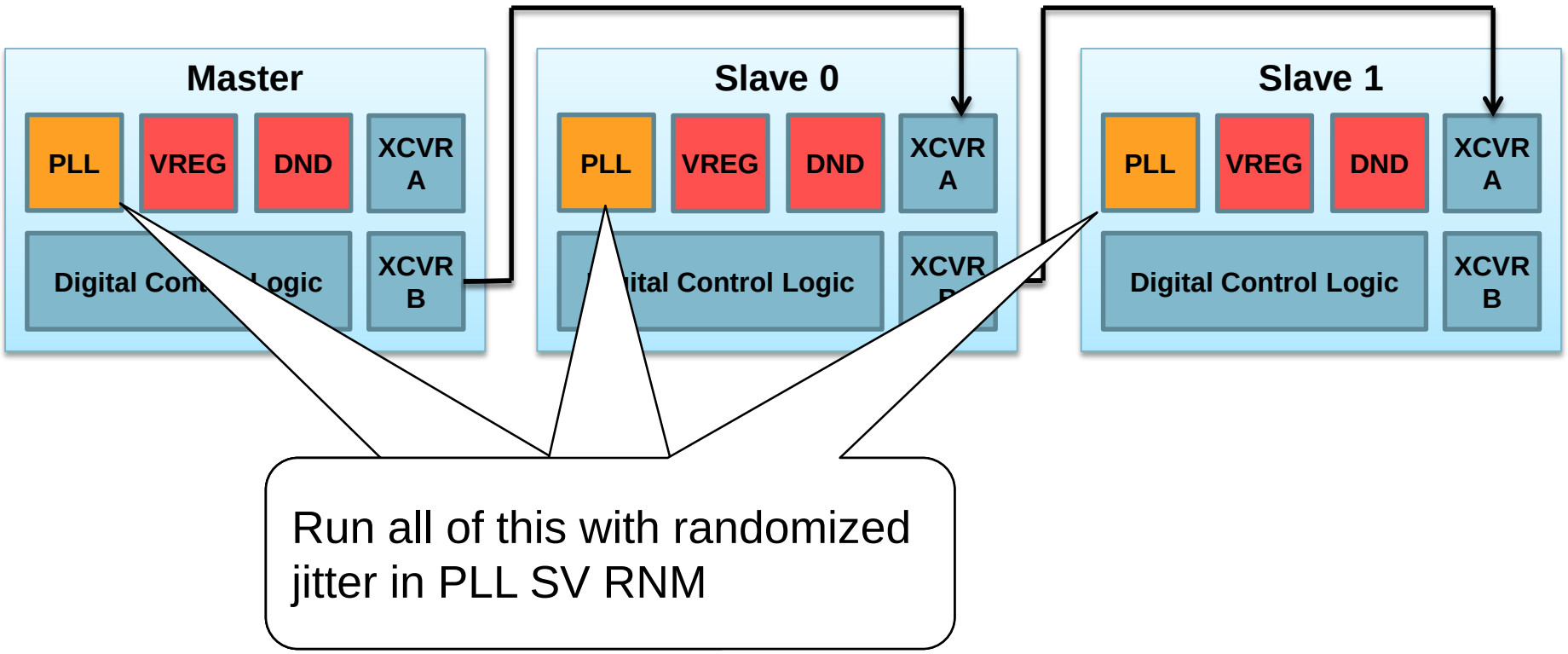
- Cosim was used to debug the failing DND behavior
  - Cosim provided accurate voltages and currents in waveforms
  - Potential design fixes could be checked with a fast turnaround time using regressions
- Cosim regressions provided high confidence in revised design
  - Various tests used to optimize fixes and component values
  - Ability to run large number of LMA nodes ensured robust solution

Goal 3: Stress AMS Blocks



Goal 3: Stress AMS Blocks

Fully verify AMS discovery process



LMA DV Results

Testbench	Bugs Found	Simulation Count
PLL	16	2463580
VREG	18	249477
DND	11	810281
System	238	329702

Sim and Model Performance

Simulation Type	TB Cfg	Runtime
Spice Only	1-9	Not Possible
AMSD Cosim (Spice for DND, PLL, VREG)	2 Node	6 Days
	9 Node	Not Possible
AMSD Cosim (Verilog PLL, Spice VREG & DND)	2 Node	13 Minutes
	9 Node	1.25 Hours
Verilog Sim (SV RNM for PLL, VREG & DND)	2 Node	9 Minutes
	9 Node	1.5 Hours
All Verilog Models	2 Node	30 seconds
	9 Node	2.5 Minutes

Lessons & Future Work

- **No reason for analog/mixed signal verification not to be metric driven**
  - **Capabilities, tools and expertise already exist**
  - **Adds a lot of value and finds bugs!**
  - **Verification planning and automated regressions provide the biggest impact**
- **Up front verification planning worth the effort!**
  - **Final cosim identified in initial planning found system level bug**
- **Fast spice is too slow for all required system simulations**
  - **Can we do a better job with SV Real Number Modeling?**
- **Mistake not to develop AMS models up front and regress them**
  - **Late issue with model caught by netlist inspection**
  - **No magic for developing and testing models**
  - **Capabilities exist just need to do the work**

Thank You!

- **LMA Design & DV Team**
  - **Lew Lahr, Stuart Patterson, A Gutmann, Will Hooper, Ara Arakelian, Bill Thomas, Mike Young, Gordon Cheung, Piotr Olejarz, Ashar Saleem, Todd Honan, Jainik Kathiara**
- **CAD Support**
  - **Syam Veluri and Mani Mariappan**
- **Cadence Support**
  - **Praveen Sridhar Pillai**
- **Synopsys Support**
  - **Paul Collins**