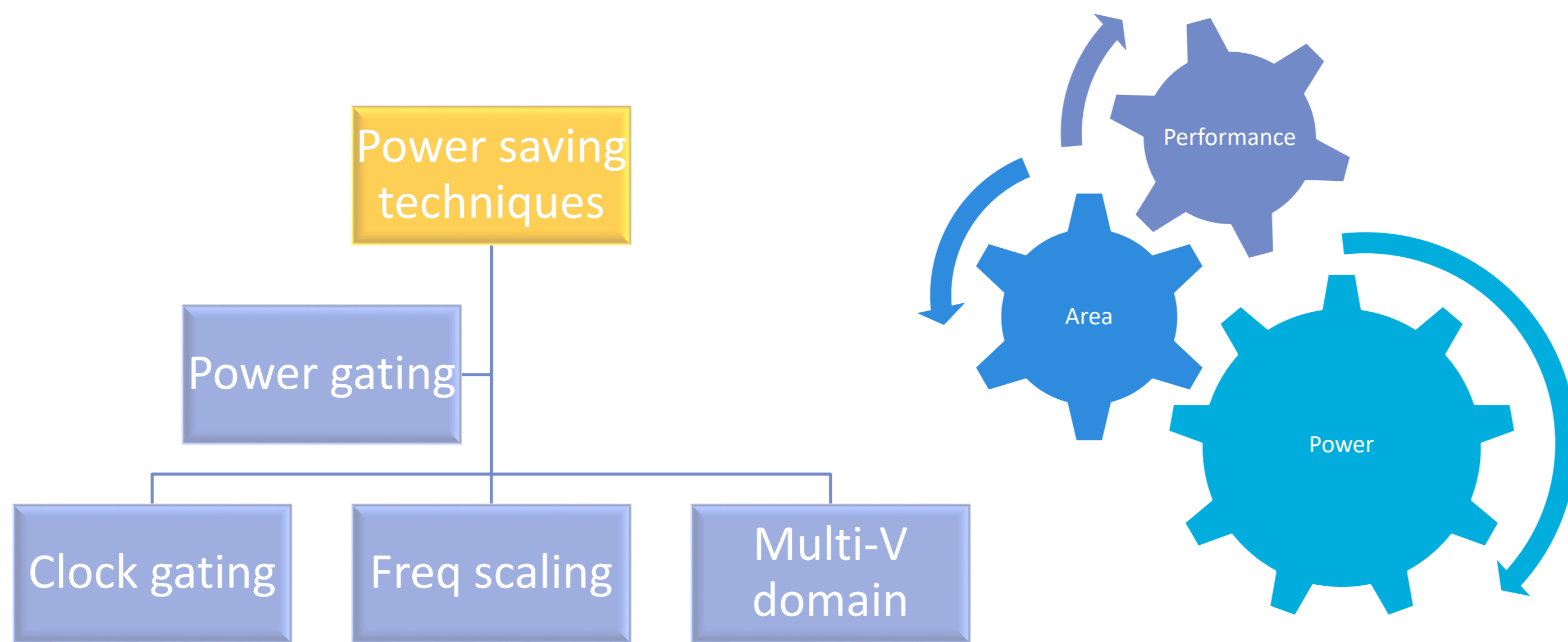


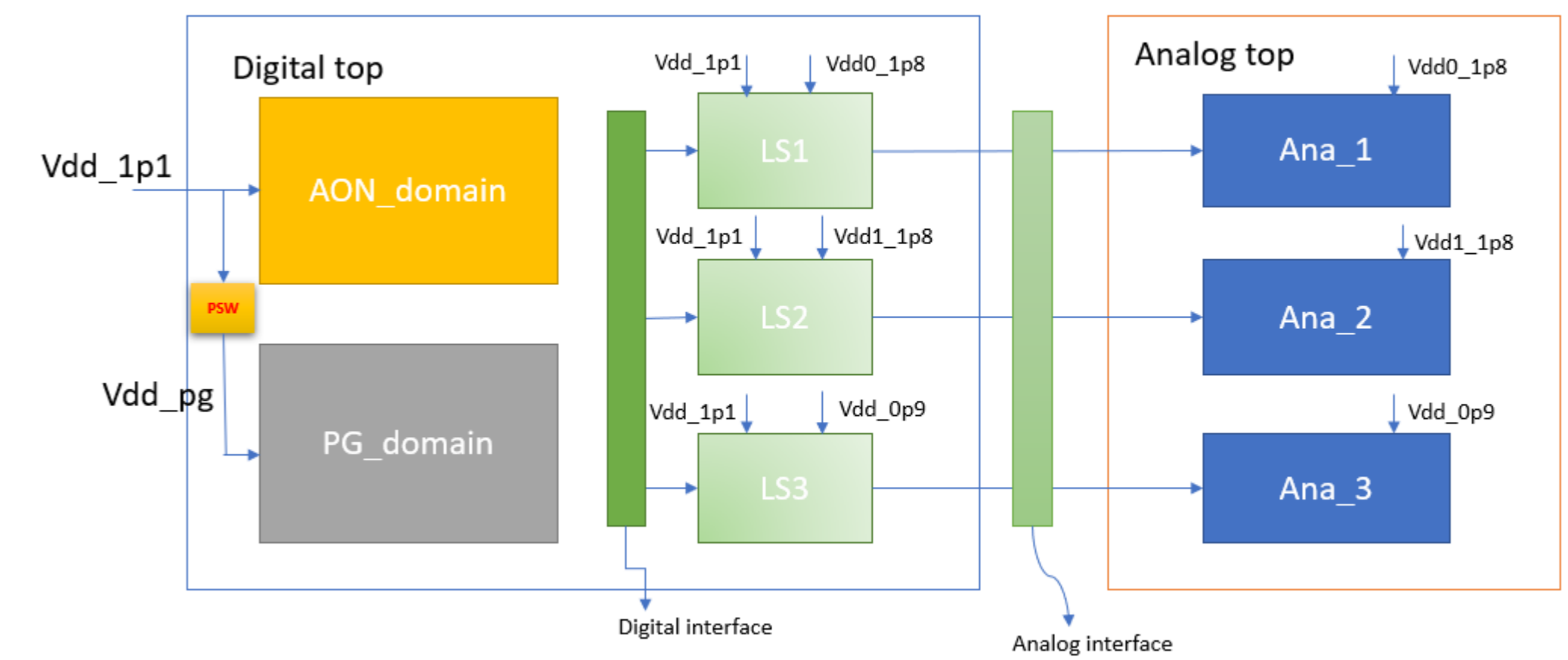
Problem Statement/Introduction

- Portable systems crave for low-power and ultra-low power solutions.
- With increase in complexity of low power design techniques, How do we verify the power intent of such systems?
- How do we mimic exact silicon behavior in design phase?



Proposed Methodology/Design details

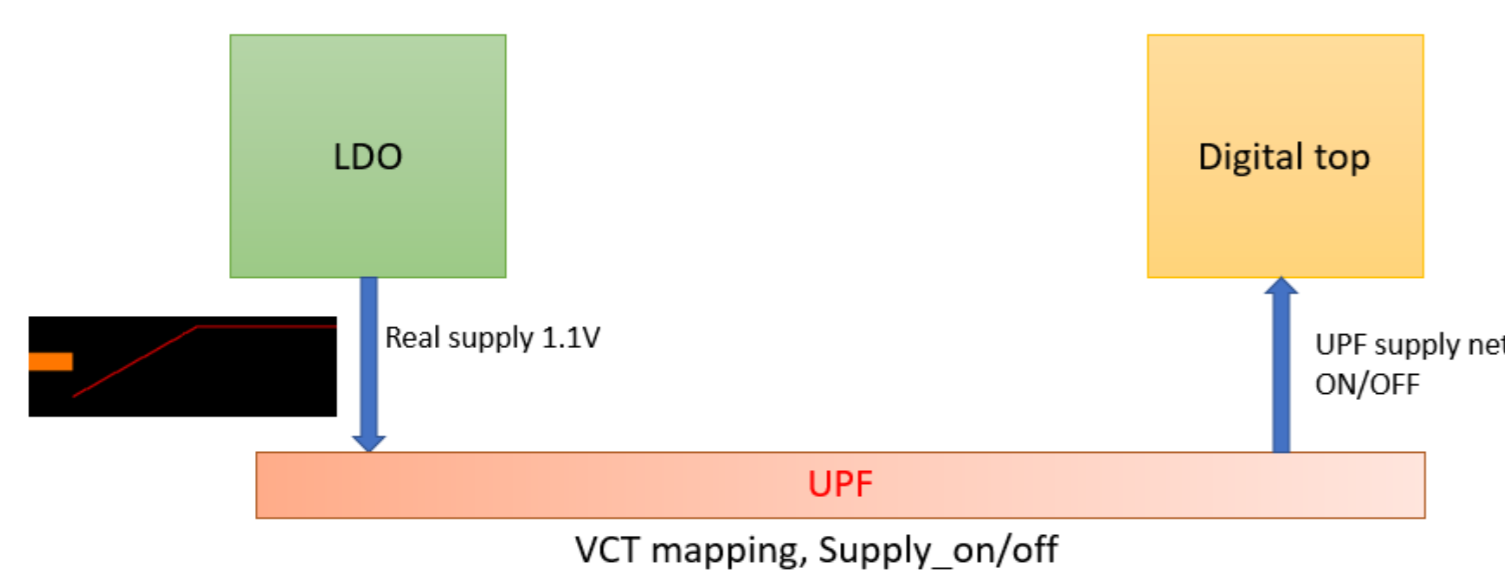
- IEEE 1801 aka UPF standard acts like a boon to verify the power intent in very early phase of design.
- DMS low power verification has three major components:
 - Analog SV-RNM models - replicates analog schematic behavior.
 - Digital design
 - UPF - contains power intent definition



Implementation Details/Setup

- Supply interaction between analog and digital.
 - VCT supply mapping in UPF
 - Usage of \$supply_on/off
- Signals interaction between analog and digital.
 - Drives X 's on the digital interface until supply ramps up.
 - Isolation cells clamps the signals to known values.

```
#####
# Create HDL2UPF VCT
#####
create_hdl2upf_vct VCTWR2UPF_VDD \
    -hdl_type {svc ds_rnm} \
    -table {(>= 1.1 FULL_ON) \
            {>= 0.6 PARTIAL_ON} \
            {<0.6 OFF}}
void' ($supply_off(VDDsupplyNet, 0.0));
void' ($supply_on(VDDsupplyNet, 1.1));
```

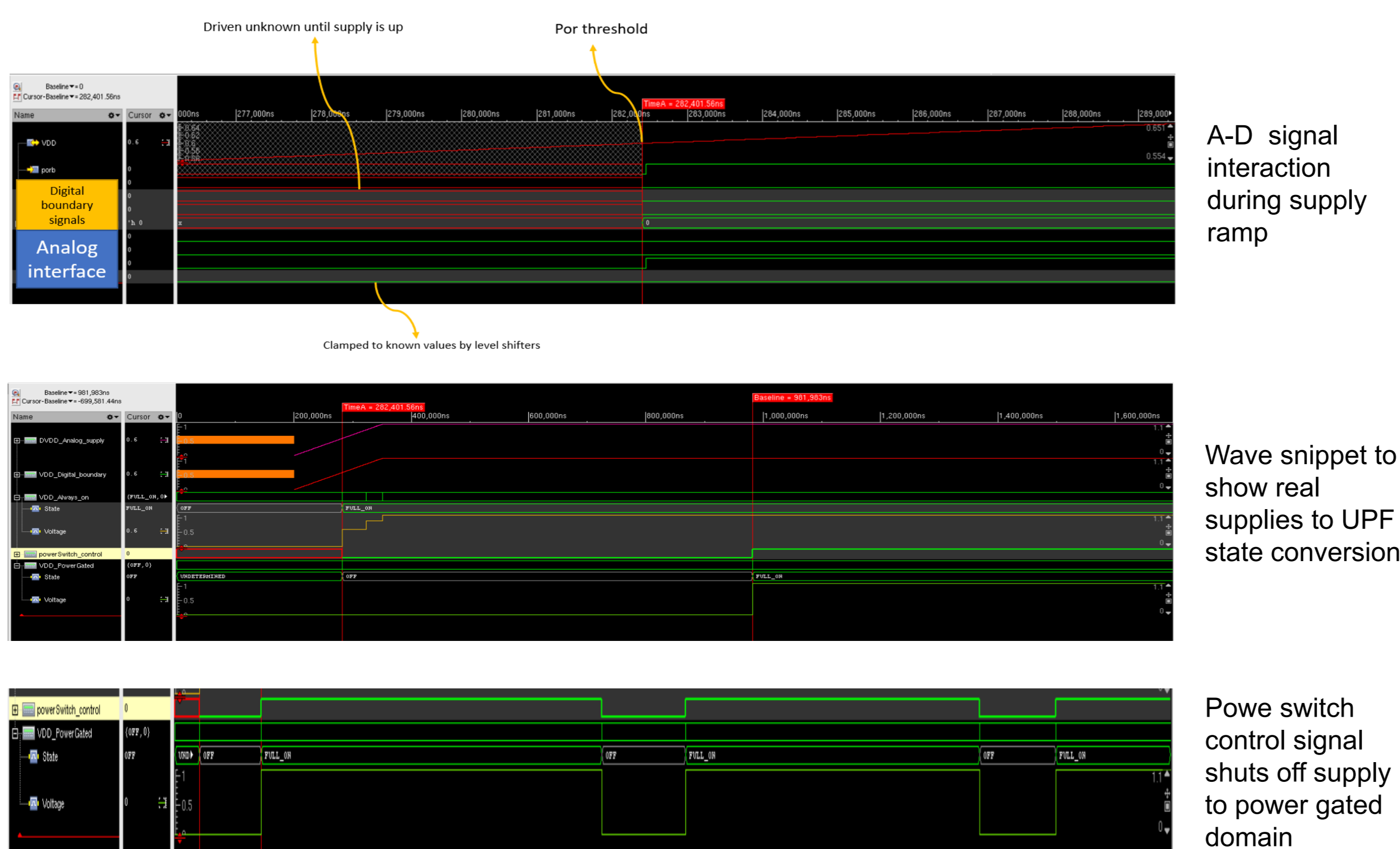


Implementation Details/checkers

- Main Checkers:
- Supply state check


```
supplyState = UPF::get_supply_state(UPF::get_supply_value(supplyNet));
```
 - Isolation check
 - Assertions to verify Isolation clamp values against expected.
 - Level Shifter
 - Signal domain checking: To ensure signals are at correct voltage levels.
 - Supply connectivity checks: Checks proper voltage domain separation
 - Memory I/O timing : Checkers placed at memory interface.
 - Power sequencing checks: Checks power up/down sequence

Results Table



Conclusion

Advantages of using UPF in DMS:

- Finds bugs in power architecture early in the design cycle.
 - We found bug in MBIST inserted RTL where one of the TDR in power gated domain was driving always-on memory interface signal.
- DMS helps in stabilizing UPF before physical design flow is completely setup, That saves time at backend.
- Helps visualizing silicon behavior and power dependencies in RTL phase.

REFERENCES

- [IEEE 1801 standard LRM](#)