Digital mixed-signal low power verification with Unified power format(UPF)

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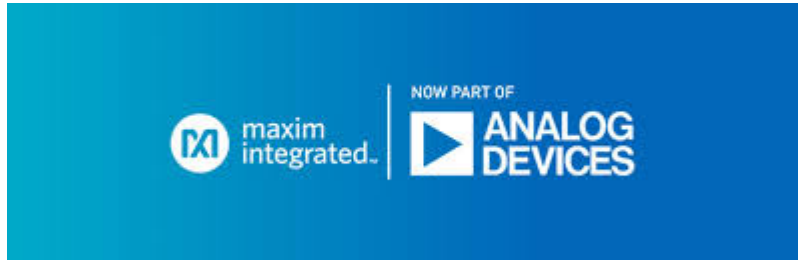

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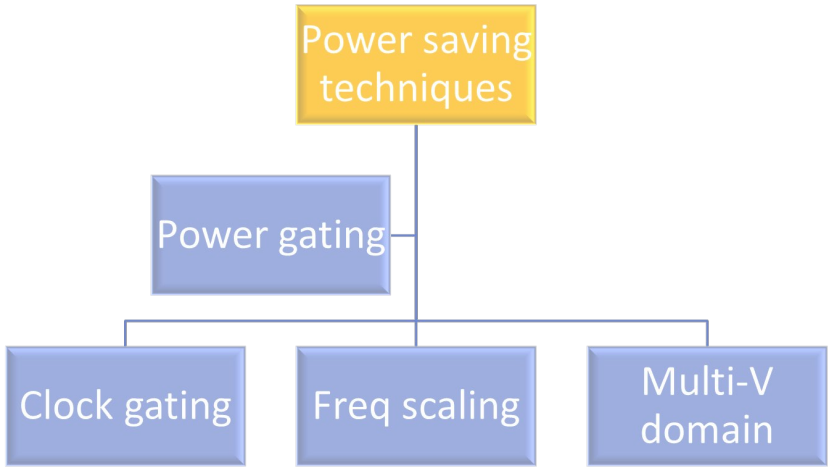
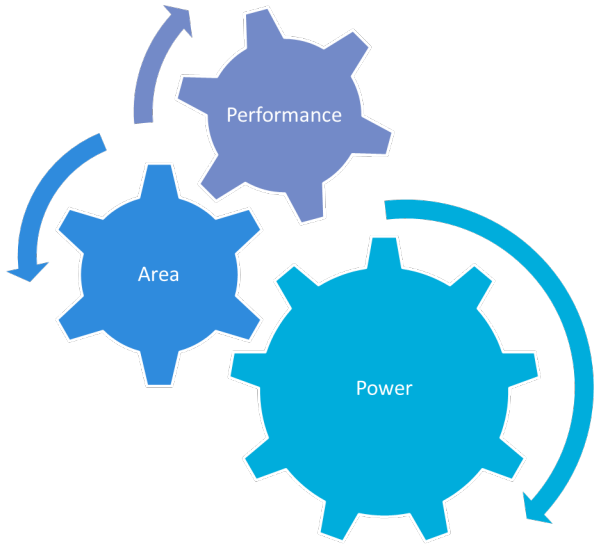
Problem statement

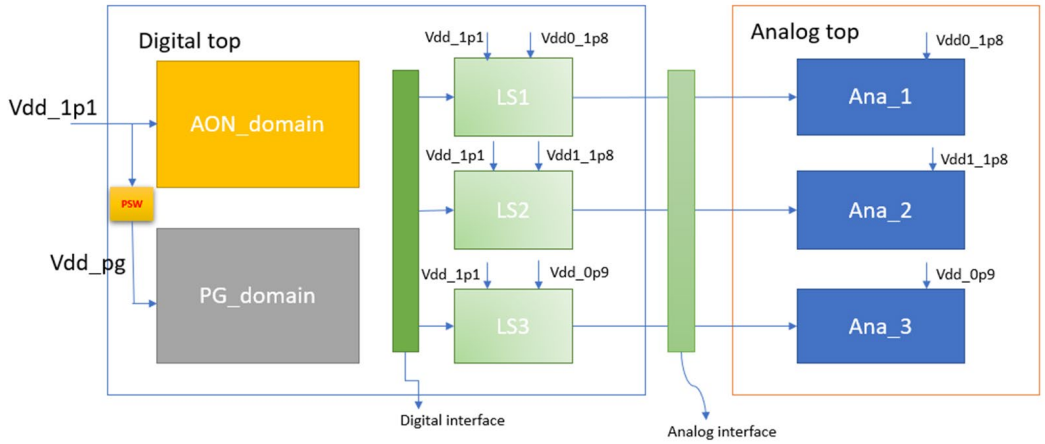
- Portable systems crave for low-power and ultra-low power solutions.
- With increase in complexity of low power design techniques, How do we verify the power intent of such systems?
- How do we mimic exact silicon behavior in design phase?





Proposed Methodology

- IEEE 1801 aka UPF standard acts as a boon to verify the power intent of any complex systems, in very early design phase.
- DMS low power verification has three major components:
  - Analog SV-RNM models – replicates analog schematic behavior.
  - Digital design
  - UPF – contains power intent definition

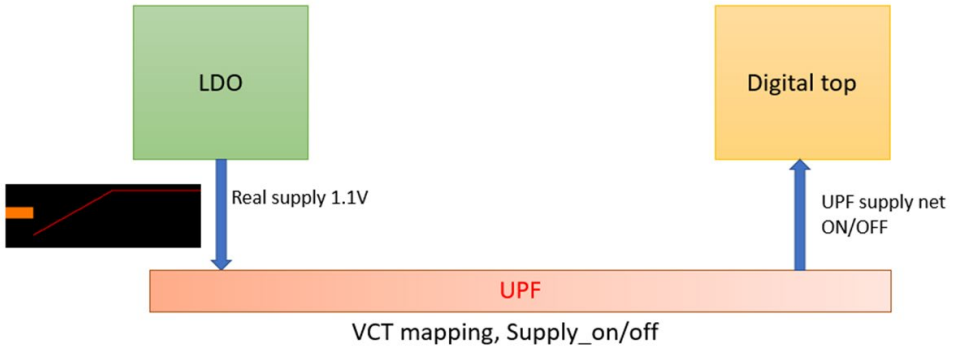


Setup

- Supply interaction between analog and digital.
  - VCT supply mapping in UPF
  - Usage of $supply_on/off
- Signals interaction between analog and digital.
  - Drives X ’s on the digital interface until supply ramps up
  - Isolation cells clamps the signals to known values.

```
##############################################################################
# Create HDL2UPF VCT                                                         #
##############################################################################
create_hdl2upf_vct VCTWR2UPF_VDD \
                -hdl_type {svc ds_rnm} \
                -table {{>= 1.1 FULL_ON} \
                        {>= 0.6 PARTIAL_ON} \
                        {<0.6 OFF}}
```

```
void'($supply_off(VDDsupplyNet, 0.0));
void'($supply_on(VDDsupplyNet, 1.1));
```



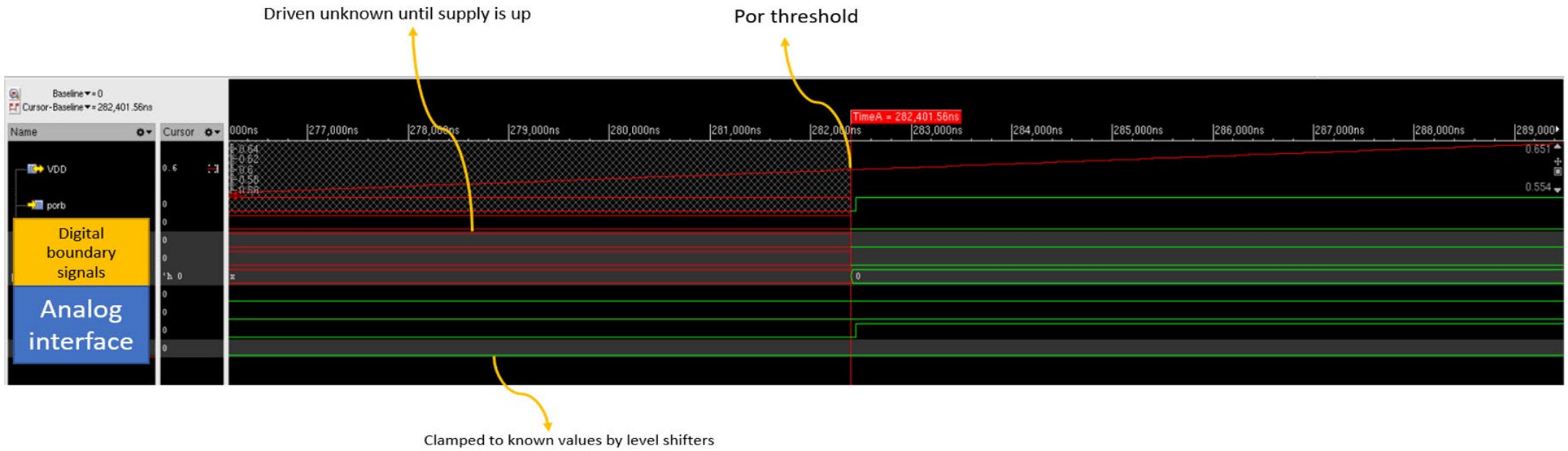
Checkers

- Supply state check

```
supplyState = UPF::get_supply_state(UPF::get_supply_value(supplyNet));
```

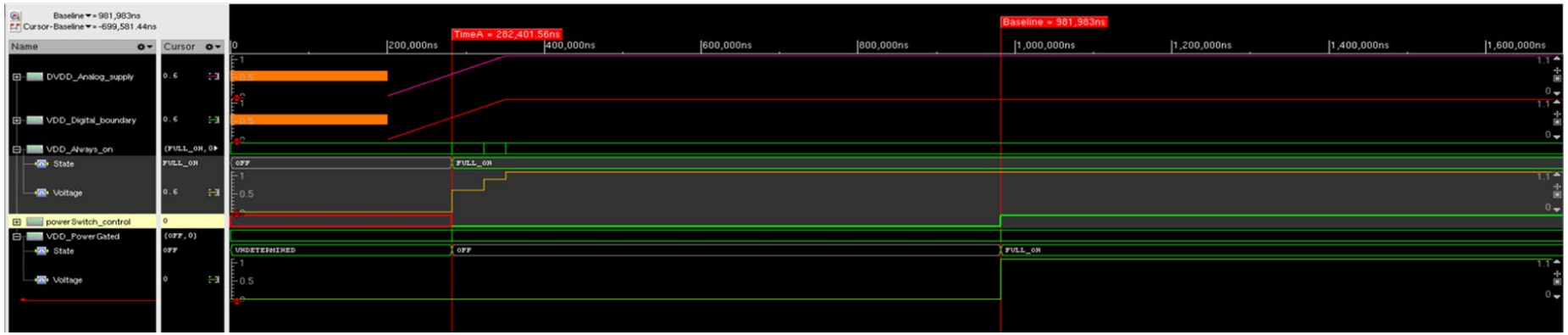
- Isolation check
  - Assertions to verify Isolation clamp values against expected.
- Level Shifter
  - Signal domain checking: To ensure signals are at correct voltage levels.
  - Supply connectivity checks: Checks proper voltage domain separation
- Memory I/O timing : Checkers placed at memory interface.
- Power sequencing checks: Checks power up/down sequence

Results

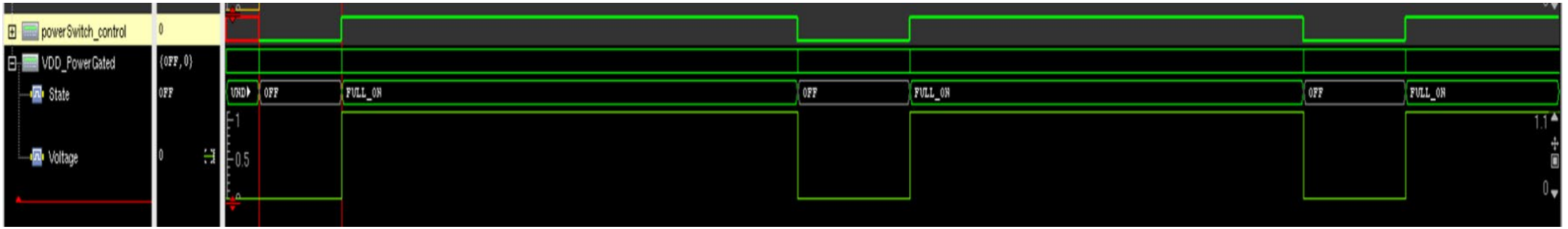


A-D signal interaction during supply ramp

Results



Wave snippet to show real supplies to UPF state conversion



Power switch control signal shuts off supply to power gated domain

Conclusion

- Advantages of using UPF in DMS:
  - Finds bugs in power architecture early in the design cycle.
    - We found bug in MBIST inserted RTL where one of the TDR in power gated domain was driving always-on memory interface signal.
  - DMS helps in stabilizing UPF before physical design flow is completely setup, That saves time at backend.
  - Helps visualizing silicon behavior and power dependencies in RTL phase.

Questions?