Did Power Management Break My CDC Logic?
An Integrated Approach to Power Domain and Clock Domain Crossing Verification

Ashish Amonkar[1] Kurt Takara[2] Avinash Agrawal[3]

[1]Ashish Amonkar, Principal Design EngineerCypress Semiconductor, ashish.amonkar@cypress.com
[2]Kurt Takara, Mentor, a Siemens Business, kurt_takara@mentor.com
[3]Avinash Agrawal, Mentor, a Siemens Business, avinash_agrawal@mentor.com

***Abstract*- Although dynamic power usage has been a concern for decades, leakage power is a big concern for today's SoC designs below 65nm. Reducing power consumption is essential to both mobile and data center applications, where lower power contributes to either longer battery life in IoT and handheld products while minimally impacting performance. The solution has been to partition designs into multiple power domains which allows selectively reducing voltage levels or powering off partitions. Traditional low power verification only validates the functional correctness of power control logic, but it does not validate the impact of power logic on multi-clock logic.**

I. Introduction

Although dynamic power usage has been a concern for decades, leakage power is a big concern for today's SoC designs below 65nm. Reducing power consumption is essential to both mobile and data center applications, where lower power contributes to either longer battery life in IoT and handheld products while minimally impacting performance. The solution has been to partition designs into multiple power domains which allows selectively reducing voltage levels or powering off partitions. Traditional low power verification only validates the functional correctness of power control logic, but it does not validate the impact of power logic on multi-clock logic.

Today, designers understand clock domain crossing (CDC) design and verification [1], but leading-edge design teams must incorporate low power techniques as part of their CDC analysis to detect CDC issues which are introduced as a result of the low power design approaches. Low power CDC analysis techniques [2] successfully identify CDC problems resulting from incorrect power control logic insertion. In this paper, we will discuss the effects of advanced low power design on CDC design and verification. Specifically, we will describe the CDC issues caused by the addition of power control logic including isolation cells, retention cells, and level shifters.

We will describe the resolution of these CDC issues by employing power-aware CDC analysis techniques:

- Low power-based clock and reset analysis
- Identification of low-power CDC paths and synchronization structures
- Identification and debug of low-power CDC violations

Finally, we will illustrate these issues and solutions with real life Unified Power Format (UPF) [3] examples and de-signs.

II. Background

Design teams are aware of ways that low power design can adversely affect design logic. One of the biggest challenges is that conventional RTL has no notion of power domains and the information on the power supply network, power domains, and other low power logic in contained in the Unified Power Format (UPF) file. Traditional RTL verification does not address the low power logic, so often, low power issues may only be caught very late during gate-level verification after the low power logic has been added to the design.

Additionally, design teams were not previously concerned about CDC paths to and from retention cells, because they believed that the save and restore protocol protected the retention logic from adverse effects due to metastability. Now, design teams are also concerned about CDC paths involving both isolation and retention cells. Designers are using synchronizers with retention registers to synchronize paths that traverse voltage domains.

This paper explains the new low power CDC issues and the CDC verification techniques developed to verify low power designs.

III. UPF AND LOW POWER DESIGN

The latest UPF standards introduce successive refinement for low power design and verification. Successive refinement supports the System-on-Chip (SoC) design and verification flow by allowing the UPF file to be refined and updated as it travels from IP design to SoC design to SoC place and route. The UPF will also be refined as it is updated to support both front-end tools such as verification tools as well as back-end tools such as physical implementation tools.

The power distribution network is a physical implementation feature that is added to the design late in the project cycle. In UPF, a power network grouping option, the power supply set, allows design teams to specify power groups without the definition of the power ports, nets, and switches and their connection to the power domains. The power supply set allows designers to define and test the power distribution network earlier in the project cycle before the power distribution network has been implemented (See Fig. 1).

```
# Specify Supply Set
create_supply_set PRIMARY1
create_supply_set  PRIMARY2

# Declare primary power and ground nets for the power domains
associate_supply_set PRIMARY1 -handle PD1.primary
associate_supply_set PRIMARY2 -handle PD2.primary
```

Figure 1. UPF for Power Distribution Network.

The UPF power distribution network is an example of the successive refinement methodology where the power network can be incrementally built over the duration of the project cycle by the different teams on design projects. The block and system designers can begin to verify the power management logic before the power distribution network has been implemented, then the final power management logic verification will occur later in the design flow when the physical designers add the power distribution network.

Power elements are not directly instantiated in the design, but the power element instantiation is defined in the UPF.

```
# Level shifter specification
set_level_shifter srss_tind_vccdpslp2vddd_clamp1_isoscanclamp_ls  -domain VDDD_PD  -location self  -rule
low_to_high  -threshold 0  -input_supply_set VCCDPSLP_VSSD_SET  -output_supply_set VDDD_VSSD_SET  -
applies_to both \
-elements { \
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_secure_wr_n[3]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_secure_wr_n[2]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_secure_wr_n[1]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_secure_wr_n[0]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_fw_wr_n[3]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_fw_wr_n[2]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_fw_wr_n[1]
u_srss_tind_top/u_srss_tind_vddd/tst_xres_secure_fw_wr_n[0]
u_srss_tind_top/u_srss_tind_vddd/test_conn_exthost_disable
u_srss_tind_top/u_srss_tind_vddd/test_conn_debug_disable
u_srss_tind_top/u_srss_tind_vddd/test_conn_test_disable
}
```

Figure 2. UPF for Level Shifter.

```
# Level shifter specification
set_isolation mxs28srss_vccact2vccdpslp_clamp0_actiso_iso  -domain VCCDPSLP_PD  -location self  -
isolation_supply_set VCCDPSLP_VSSD_SET  -isolation_signal u_srss_tdep_vccdpslp/act_isolate_scantrans  -
isolation_sense high   -clamp_value 0  -applies_to both \
-elements { \
u_srss_tdep_vccdpslp/core_reg_read_en
u_srss_tdep_vccdpslp/pll_config12_pwr1_enable_all[0]
u_srss_tdep_vccdpslp/pll_config12_pwr1_enable_all[1] …
```

Figure 3. UPF for Level Shifter.

```
# Retention specification
set_retention mxs28srss_vccact_ret  -retention_supply_set VCCRET_VSSD_SET -retention_condition {
u_srss_tdep_vccact/act_retain_vccret } -domain VCCACT_PD \
-elements { \
u_srss_tdep_vccact/gen_pll[0].gen_ana_pll1_lp_present.u_srss_pll_lp/u_srss_pll_lp_regs/config_bypass_sel
u_srss_tdep_vccact/gen_pll[0].gen_ana_pll1_lp_present.u_srss_pll_lp/u_srss_pll_lp_regs/config_pll_enable
```

Figure 4. UPF for Retention.

IV. Application

For traditional designs, static structural analysis is used to identify both correct and incorrect CDC synchronization structures. For low power designs, both isolation and retention cells must be reviewed to ensure that incorrect CDC paths are correct as these cells should not disrupt correct CDC structures and should not introduce new CDC paths.

Advanced low power designs are taking advantage of common CDC verification techniques to ensure that data transfer between power domains are not corrupted by metastability. These CDC verification techniques include the identification of low power CDC paths and synchronization structures as well as support for both isolation and retention cells. Static structural analysis is a typical technique used to verify CDC paths, but for low power designs, both isolation and retention cells must be reviewed to ensure that incorrect CDC paths are identified and corrected.

With the power aware CDC analysis, designers are able to identify CDC paths affected by low power structures. Designers must ensure that isolation signals are correctly synchronized on CDC paths and Figure 5 shows both data and isolation enable sources in the same clock domain as the destination register. In addition, CDC analysis should detect scenarios where isolation signals are not properly synchronized. In Figure 6, there is no CDC crossing on the B1-B2 path that is represented in the RTL, but the B3-B2 CDC crossing is introduced with the UPF. When the isolation enable is in the clk2 domain is asserted or deasserted, this may generate an asynchronous event that would cause metastability on the B2 register in the clk1 domain. Also, designers also utilize the power aware CDC verification to validate correct retention cell usage.

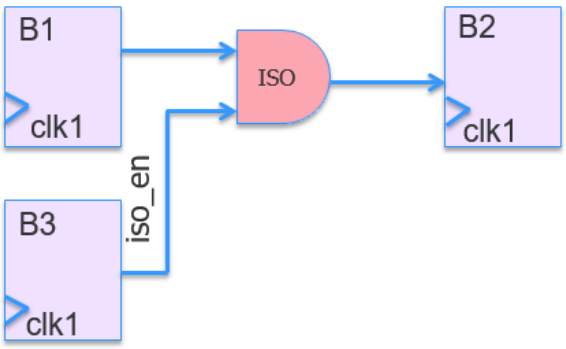

Figure 5. Isolation enable on correct clock domain.

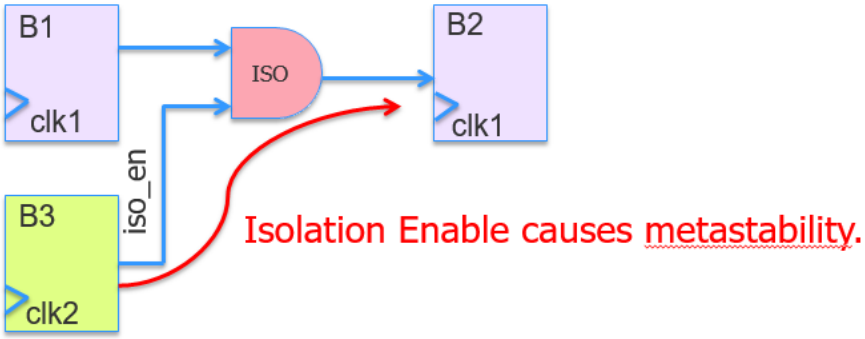

Figure 6. Isolation enable on incorrect clock domain.

Power aware CDC analysis detects cases where low power logic introduces combinational logic in the fan-in of a synchronizer. In Figure 7, a 2DFF synchronizer structure is correctly implemented in RTL from B1 to the B2 synchronizizer, but the isolation cell is described by the UPF and the isolation logic creates a combinational logic violation. Combinational logic fanin into synchronization structures will reduce the reliability of the synchronizer. Similar to CDC combinational logic violations, designers should ensure that design logic must first be registered before driving a CDC synchronizer.

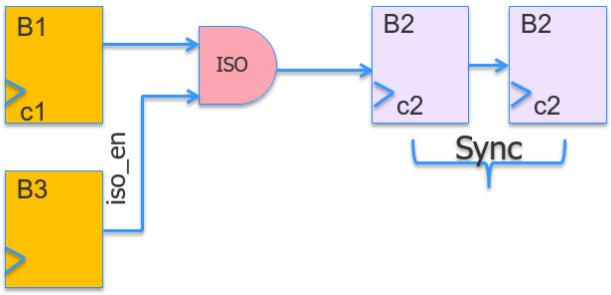

Figure 7. Isolation logic introduces combinational logic violation.

For reporting CDC results, the CDC paths related to low power logic are reported under separate schemes (Figure 8). The low power specific schemes allow engineers to distinguish between non-power related CDC paths and CDC paths affected by low power logic. Since our team was focused on low power-related issues, the separate schemes allowed the team to easily identify, review and debug low power CDC issues.

pa_combo_logic
    UPF adds combinational logic to a crossing.
pa_iso_en_no_sync
    UPF isolation cell enable signal does not have a proper synchronizer.
pa_retention_restore
    UPF retention register restore port does not have a proper synchronizer.

Figure 8. Power aware CDC scheme examples.

IV. Low Power CDC Flow

The low power CDC verification flow is an incremental change to the traditional RTL CDC verification flow (Figure 9). In the traditional flow, the low power elements are added to the design during the implementation phase of the project, so the low power CDC analysis will happen late in the design project. For Power Aware CDC verification, the power annotation adds the low power elements specified in the UPF to the RTL design.

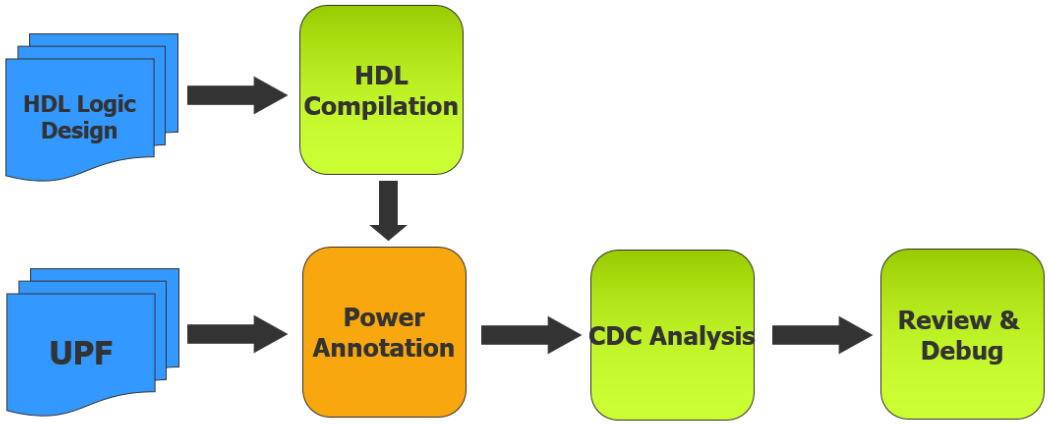

Figure 9. Power Aware CDC Verification Flow.

Cypress Low Power CDC Analysis:

- Step 0: Generate parameterized UPF
- Step 1: Compile the RTL design
- Step 2: Run CDC analysis with UPF (Figure 10)
- Step 3: Generating Power Aware CDC report (Figure 11)

For the Cypress Low Power CDC Analysis, the Power Aware CDC analysis is run at the subsystem level. The subsystem contains parameters that control the power switch configurations, so multiple configurations must be separately tested for low-power CDC integrity. During Step 0, a script generates configuration-specific UPF that

correlates to the RTL with the same parameter configuration. For Step 2, the Power Aware CDC analysis is run on each RTL and UPF configuration set.

```
qverify -c -do " \
          onerror {exit 1}; \
          cdc run -d top -pa_upf my.upf; \
          exit 0"
```

Figure 10. Specify UPF for CDC analysis.

```
qverify -c -do " \
          onerror {exit 1}; \
          cdc run -d top -pa_upf my.upf; \
          cdc generate crossings crossings.rpt; \
          cdc generate pa pa_design_detail.rpt -design;  \
          exit 0"
```

Figure 11. Generate Power Aware CDC report.

V. RESULTS

In our designs, we utilized low power CDC verification techniques to ensure that data transfer between power domains are not corrupted by metastability. The static techniques include the identification of low power CDC paths and synchronization structures as well as support for both isolation and retention cells in our RTL designs. For the subsystem, the Power Aware CDC analysis instantiated 286 isolation cells from the UPF file.

TABLE I
POWER AWARE CDC RESULTS

	Power Domains	Primary Clocks	Isolation Cells	Retention Registers
Subsytem	5	10	286	0

TABLE II
POWER DOMAIN RESULTS

Power Domain	Registers	Latches	Isolations	Level-Shifters	Retentions
PD1	8187	569	1	0	0
PD2	5613	122	83	0	0
PD3	1029	25	201	204	0
PD4	0	0	1	1	0
PD5	0	1	0	0	0

Power Aware CDC analysis detected the CDC paths for isolation cells under the pa_iso_en_no_sync scheme (Figure 12). For these isolation cases, a low power protocol is implemented where the Rx clock is disabled when the isolation clamp is asserted and deasserted to avoid generating metastability at the Rx register. In order to check that the Rx register is safe from metastability, designers generate constraints that check the destination registers on isolation paths are connected to the correct clock. Any remaining violation paths indicate incorrect isolation

implementation that will be subject to metastability and designers must connect the Rx register to the correct destination clock. This low power isolation verification method allowed the design team to detect and correct incorrect isolation logic implementation. The CDC summary is shown below for the PA CDC checks.

CDC Violations

Isolation enable signal does not have proper synchronizer.	(43378)
Power-aware combinational logic before synchronizer.	(14)
Power-aware fanin logic from multiple clock domain	(10)

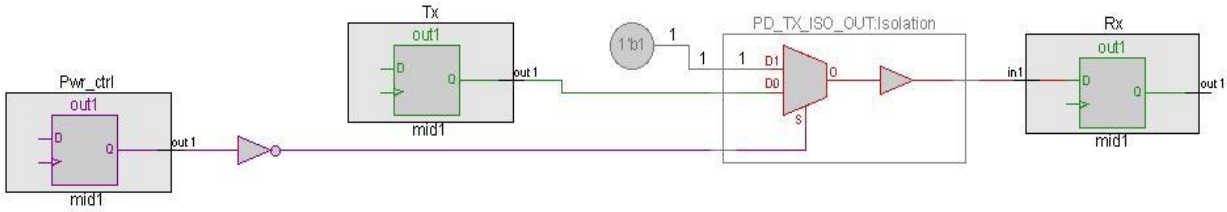

Figure 12. Low power isolation path detected as pa_iso_en_no_sync scheme.

```
cdc report item –status verified –scheme pa_iso_en_no_sync –tx_clock safe_Rx_clock
```

Figure 13. Constraint to detect safe isolation paths.

VI. CONCLUSION

Power management continues to be a critical need for IoT and mobile designs. With the advances in low power design, the low power design and verification methodologies and techniques continue to evolve. The successive refinement features in IEEE 1801 allow designers to begin the design and verification of power distribution networks earlier in the design flow and continue to refine the power networks throughout the design cycle. It is critical that designers start the CDC verification for the power distribution networks at the RTL level. Power Aware CDC analysis enables our design team to start CDC analysis before the low power logic is added to the design during implementation and avoids detection of CDC errors late in the design flow at the gate-level.

REFERENCES

[1] C.E.Cummings, “Clock Domain Crossing (CDC) Design and Verification Techniques using System Verilog,” SNUG 2008.
[2] A. Chen, et. al., “Power Aware Clock Domain Crossing Verification”, DAC 2014.
[3] IEEE 1801 : Design and Verification of Low Power Integrated Circuits
[4] A. Chakraborty, et. al., “Power-Aware CDC Verification for Faster SoC Verification”, DVCon India 2014.
[5] P. Yeung, “Multi-Domain Verification: When Clock, Power and Reset Domains Collide”, DVCon, March 2015.