Deploying HLS in a DO-254/ED-80 Workflow

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INTRODUCTION

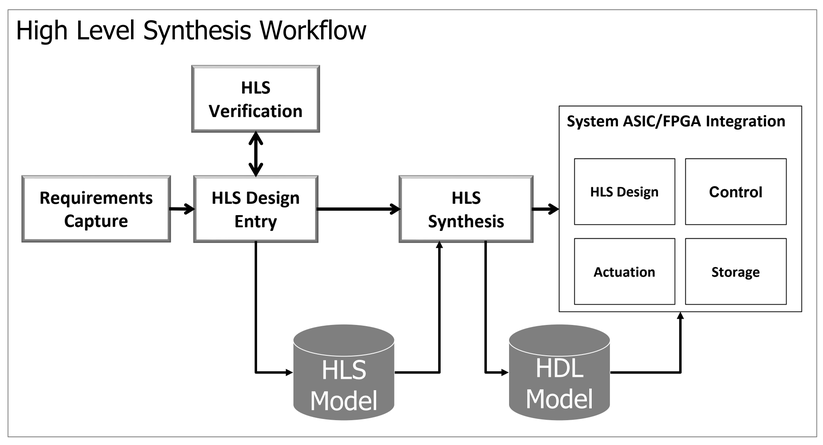
- HLS (High-Level Synthesis) is a commonly used methodology to quickly develop, test and deploy new algorithms in ICs. This is typically utilizes a more software oriented language for a higher level of abstraction (ex. SystemC or C++)
- Due to the increased complexity of aircraft systems, avionics companies continually seek ways deliver more robust functionality in their ICs in a cost effective manner
- Leveraging HLS is one of the ways to increase functional capabilities of IC designs without significantly increasing cost.
- However, some avionics companies find it a challenge to utilize HLS as part of a DO-254 workflow and need assistance regarding how to incorporate HLS and generate the required evidence necessary that demonstrates compliance to the DO-254 objectives.
- Given the advancement in verification technology, this paper provides an approach to use HLS as part of an overall workflow that complies with the overall DO-254 objectives as well as provides the evidence necessary for acceptance by the certification authorities.

DO-254 Objectives

- Planning – Usage of HLS must be disclosed in the Plan for Hardware Aspects of Certification (PHAC). It should identify the HLS workflow, artifacts that will be created, processes utilized in the flow, and DO-254 objectives that will be achieved.
- Requirements – For HLS requirements capture, an approach very similar to traditional HDL can be used. This also means that artifacts generated will also be similar to the artifacts from an HDL flow.
- Conceptual Design – Provides the architecture and design description regarding how the hardware intends to meet the requirements. Not only can formats common to an HDL flow be used, but the HLS source code itself (SystemC/C++) can be used if documented and commented properly
- Detailed Design – For HLS, the source code can be considered as the detailed design data. Standards, traceability and reviews must be performed as part of the detailed design phase.
- Implementation – The synthesis of the HLS source code into HDL is the implementation for this flow
- Configuration Management – Configuration management of the artifacts generated from the HLS flow should be performed in accordance with the DO-254 objectives.
- Verification – Verification at the HLS level allows you to verify the design sooner and quickly identify deficiencies in the design.

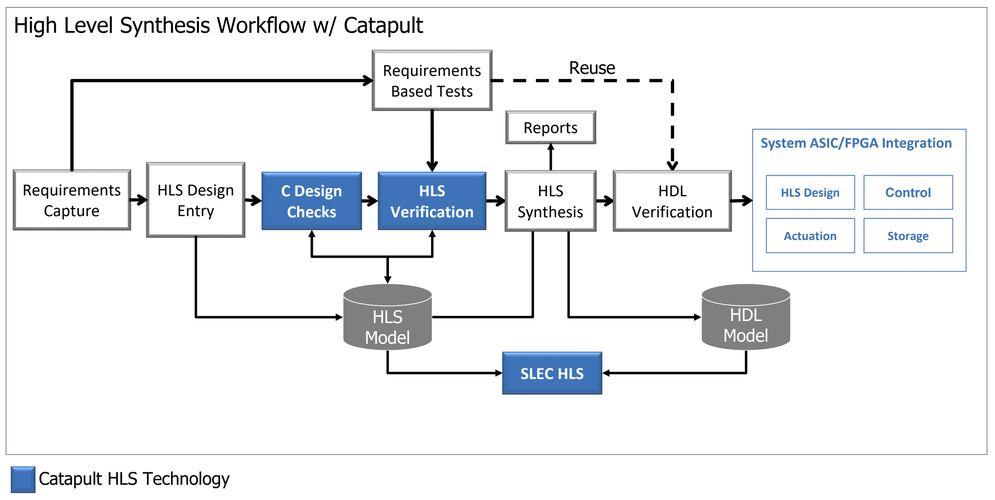
HLS Overview

- Below is a generic HLS workflow which shows it to be requirements driven as required by DO-254
- While some form of verification is performed in the HLS, there is not sufficient assurance regarding the output of the HLS synthesis



Catapult HLS in DO-254

- The enhanced Catapult HLS flow provides additional design assurance
- Design checks are performed on the HLS source code
- Simulation is performed on the HLS source code and the HDL output after HLS synthesis
- SLEC (Sequential Logic Equivalence Checking) HLS is used to formally prove functional equivalence between the HLS source code and the synthesized HDL output



CONCLUSIONS

- It is possible to utilize HLS as part of DO-254 compliant workflow
- HLS working in concert with other tools to can easily create the necessary evidence to meet objectives specified by DO-254
- Catapult HLS is a flow which readily works with additional verification tools that can provide the evidence needed for a DO-254 compliant workflow

REFERENCES

RTCA DO-254 / EUROCAE ED-80, Design Assurance Guidance for Airborne Electronic Hardware

FAA CAST-33: Compliance to RTCA DO-254/ EUROCAE ED-80, "Design Assurance Guidance for Airborne Electronic Hardware", for COTS Intellectual Property Used in Programmable Logic Devices and Application Specific Integrated Circuits

RTCA DO-331, Model-Based Development and Verification

AMC 20-152A Development Assurance for Airborne Electronic Hardware (AEH)