Data path verification on cross-domain with formal scoreboard

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Challenges of verification for data path

- The data path verification is a complex task for formal method.
- Block could work in a complete Async mode, where there is no proper relation between write clock and read clock domain. The formal tool normally can not verify such case.
- Block might be configurable by parameters of the Data-Width/ Buffer Depth/ etc.

Solution overview

- Data packets must be transferred through the DUV without corruption.
  - No dropped data packets
  - No duplicated data packets
  - No out-of-order data packets
  - No corrupted data packets

Sanity checks
- Reset connect correct
- Reset is activated
- Reset toggle once
- Packets go through the DUV
  - At least two packets are pushed
  - At least two packets are popped

Formal Scoreboard checks

- Scoreboard checks
  - Data packets must be transferred through the DUV without corruption.
  - No dropped data packets
  - No duplicated data packets
  - No out-of-order data packets
  - No corrupted data packets

Scoreboard

- Sanity checks
  - Reset connect correct
  - Reset is activated
  - Reset toggle once
  - Packets go through the DUV
    - At least two packets are pushed
    - At least two packets are popped

Async-reg/Clock modeling

- Async CDC model:
- Clock frequency Jitter
  - Such frequency jitter generates the 3 different combination of the 2 clocks.

Conclusion

- This method is not only to verify the FIFO. It can be applied in any type of data path verification.
- This method is very adaptable.
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  - The components (checkers/models) can be added or removed.