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Connecting UVM with Mixed-Signal Design

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Agenda

- Introduction
- Environment
- Verilog-AMS adapters
- PROS and CONS
- Q&A

Introduction

- Modeling approaches
  - Very high level of abstraction
  - Real Number Models (WREAL)
  - AMS
- Why UVM?
  - Constraint random verification
  - Re-usability
  - Number of tests
  - Better coverage
  - Better detection of hard-to-find bugs

UVM disadvantages

- Takes more time to build up environment

Very high level of abstraction

- VHDL models
- Very simple
- Only basic functionality is modeled
- Discrete output
- Small values used for errors
- Very fast simulations

```
//LDO output voltage modeled in VHDL
VOUT <= 0.0 when EN = "0" else
        5.0 when EN = "1" else
        0.01;
```

Real Number Models (WREAL)

- WREAL ports used
- Discrete output
- Analogish behavior
- More complex
- Only digital simulator engine is used
- Not possible to model voltage and current on the same port
- Fast simulations

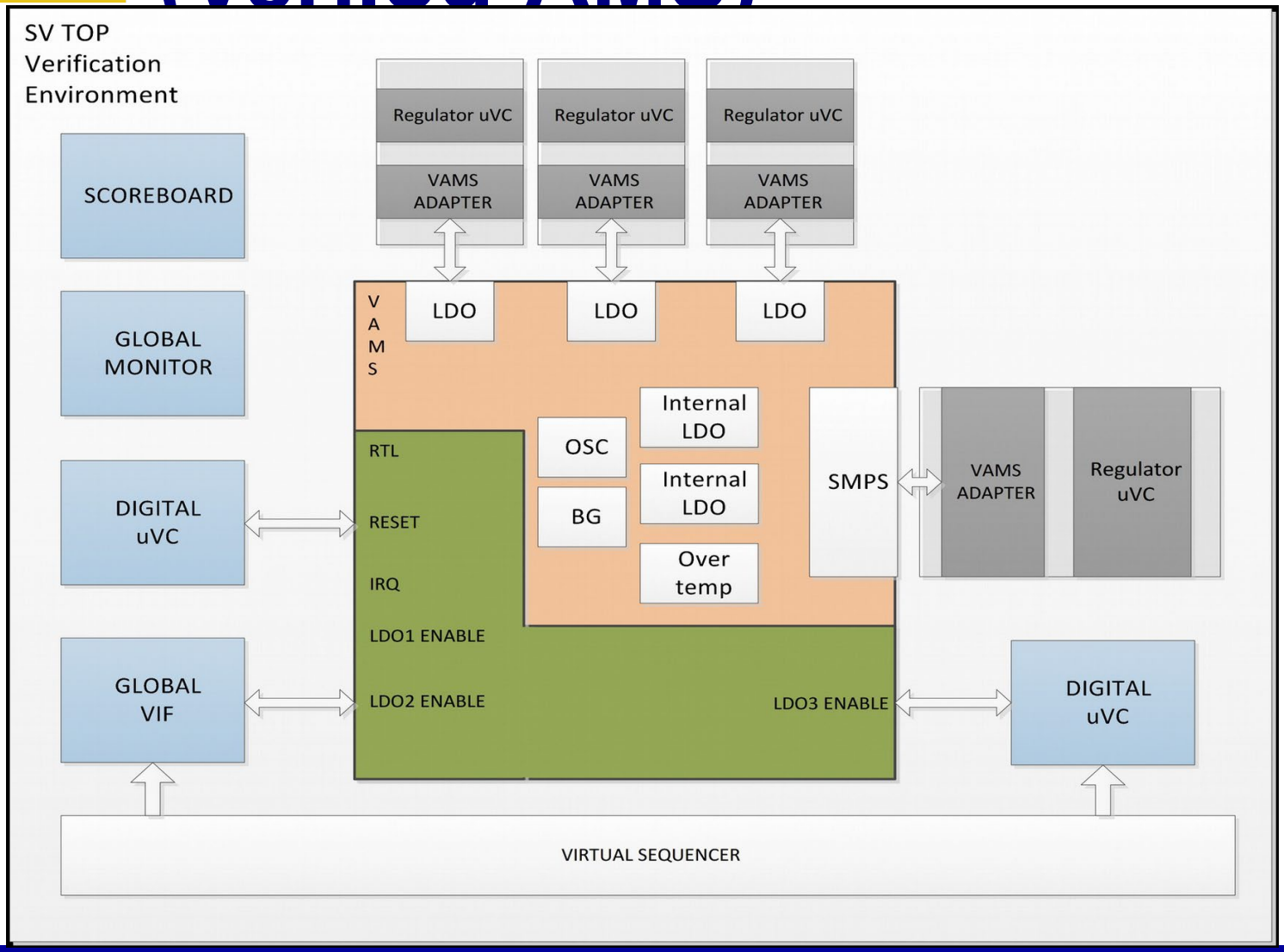
Verilog-AMS

- Electrical ports used
- Continious signals
- Exact analog behavior
- The most complex
- Digital and analog simulators are used
- Voltage and current on the same port
- Slow simulations

Environment

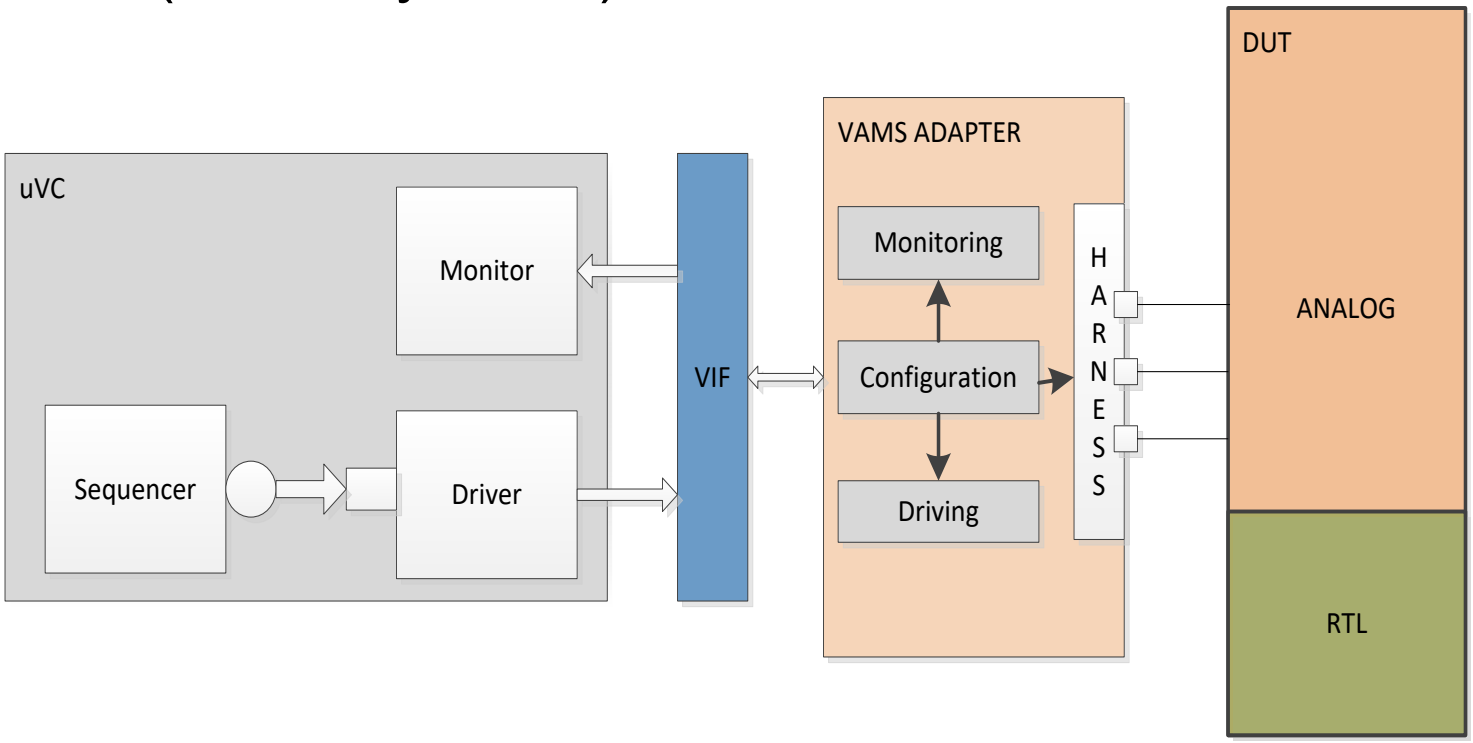
- VHDL models
  - UVM and DUT are directly connected
  - Very hard to switch to schematic
  - Checkers are mostly not reusable
- WREAL models
  - UVM and DUT are directly connected
  - Easier to switch to schematic
    - Many issues with converters (current and bidirectional ports)
  - Checkers are mostly reusable
- Verilog-AMS models
  - UVM and DUT cannot be directly connected
  - Very easy to switch to schematic

Environment example (Verilog-AMS)



Verilog-AMS adapters

- Custom connect module to connect UVM and DUT
- Main elements
  - Configuration (static, dynamic)
  - Drivers
  - Monitors
  - Harness



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Verilog-AMS adapters - configuration

- Static configuration
  - Used only at start of simulation
  - Configure initial configuration of all drivers, monitors...
- Dynamic configuration
  - Change adapter parameters during the simulation
    - Resistor values
    - Monitor thresholds

Verilog-AMS adapters – dynamic configuration

- Example
  - Over-voltage threshold update from UVM

```
module example_adapter(dyncfg_ov_th1, ... )
input [3:0] dyncfg_ov_th1;
...
//Over-voltage threshold dynamic configuration
real OV_THR;
always @(dyncfg_ov_th1) begin
  case (dyncfg_ov_th1)
    4'b0000: OV_THR = 4.0;
    4'b0001: OV_THR = 4.1;
    ...
    4'b1111: OV_THR = 6.0;
    default: OV_THR = 4.0;
  endcase
end
...
endmodule
```

Verilog-AMS adapters - driver

- Usually simple voltage or current source
- Parameters
  - Voltage/current value
  - Rise and fall times
  - Delay time
  - Output impedance
- Can be used to trigger faults on pins

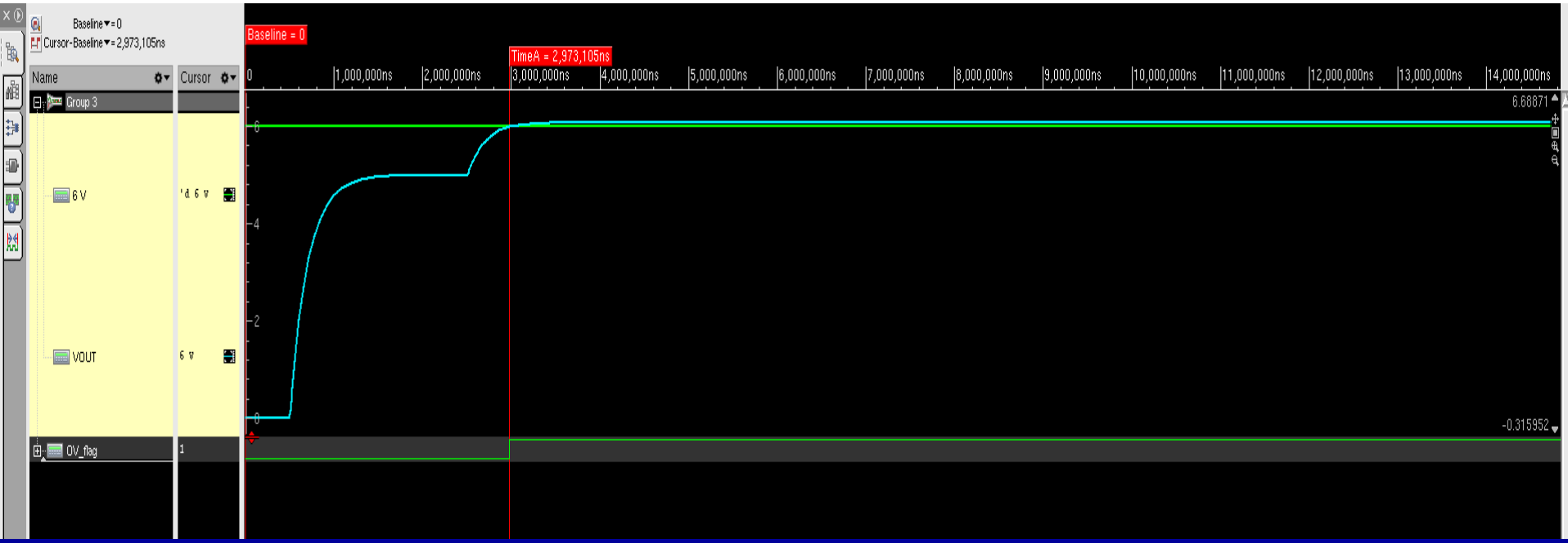
Verilog-AMS adapters - driver

- Example of the driver

```
module example_adapter(VIN, GND, ...)
output VIN;
input GND;
electrical VIN;
electrical GND;
...
//Use wreal if you need to connect through ports
real v_set; //In testbench connect v_set to vif.
real t_trans; //In testbench connect t_trans to vif
...
analog begin
  V(VIN, GND) <+ transition(v_set, 0.0, t_trans);
   ...
end
endmodule
```

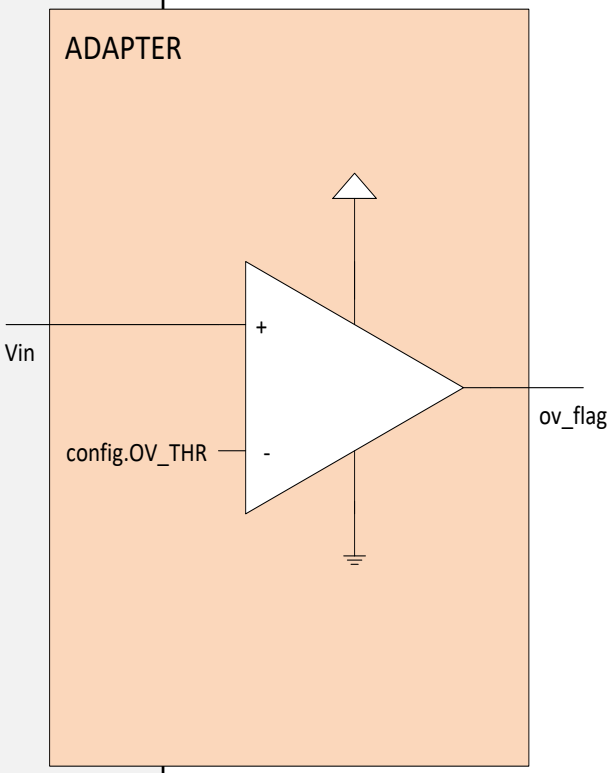
Verilog-AMS adapters - monitor

- Usually simple comparator with configurable threshold
- Return digital flag to UVM environment
  - Simplifies checkers



Verilog-AMS adapters - monitor

```
module example_adapter(OUT, GND, ov_flag_o, ... )
input VOUT; //DUT output voltage
input GND; //Ground
output ov_flag_o; //Over-voltage flag output
electrical VOUT;
electrical GND;
...
//Over-voltage monitor
reg ov_flag_s;
always @(above(V(OUT, GND) - OV_THR)) begin
  ov_flag_s = 1;
end
always @(above(OV_THR - V(OUT, GND))) begin
  ov_flag_s = 0;
end
assign ov_flag_o = ov_flag_s;
...
endmodule
```



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Verilog-AMS adapters - harness

- Contains all external components needed for a module to work correctly
  - Resistors
  - Capacitors
  - Inductors
  - Transistors
  - ...
- Topology is not changeable on the fly
  - Need to provide a way for error injection

Verilog-AMS adapters – freeze frame

- Used to store important values when error occur
  - Values are collected by UVM to be able to do checks/measurements/message reports
- Not needed for basic adapter functionality

```
module example_adapter( ... )
...
//Freeze frame block
real freeze_OUT;
always @(posedge ov_flag_s) begin
freeze_OUT = V(OUT, GND);
end
...
endmodule
```

PROS

- Simple uVCs
  - No need to deal with real values as checking is done by adapters
- Adapters are usually very simple
- No need to change anything when running Mixed-Mode simulations
- Able to find bugs in analog modules, not just in RTL
- More time for verification engineer to write exhaustive tests

CONS

- More work for analog designer
- Hard to differentiate two completely different periodic signals
  - We can measure amplitude and frequency, but we can not for sure know if that signal is sine or saw wave
  - This is the space for biggest improvements of the methodology

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Questions & Answers

Thank you for your attention!