

Challenges, Complexities and Advanced Verification Techniques in Stress Testing of Elastic Buffer in High Speed SERDES IPs

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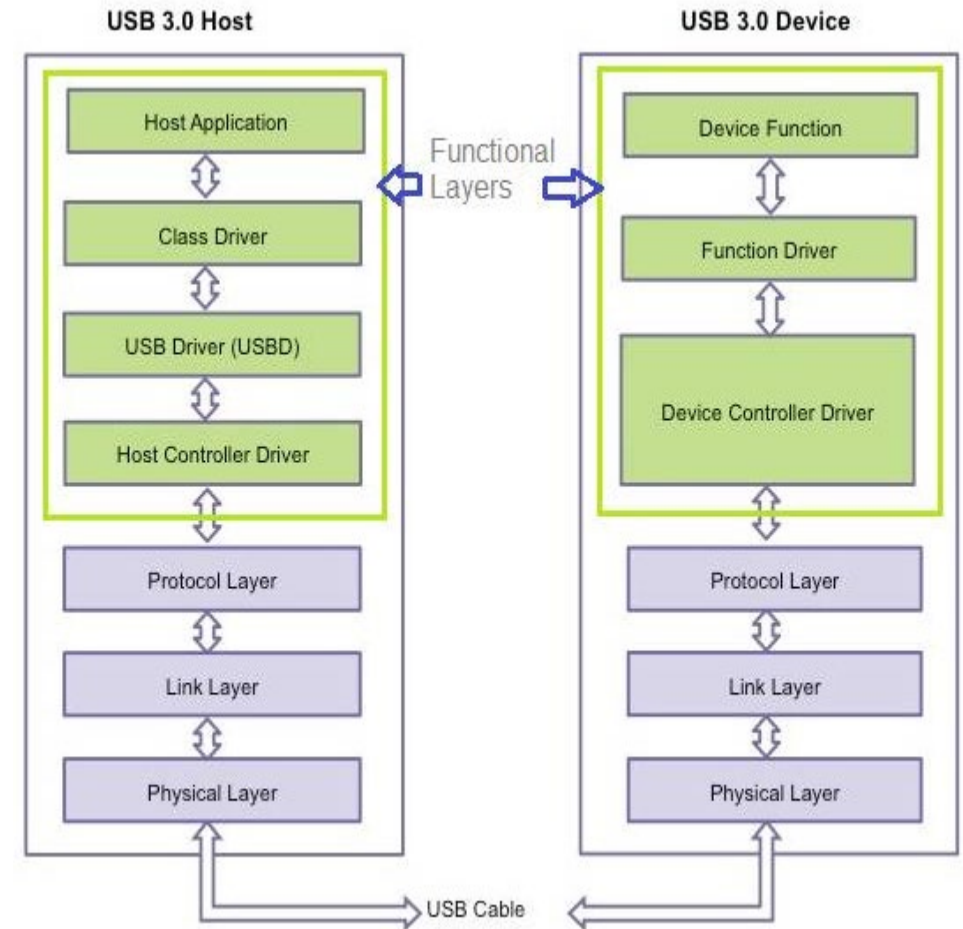


Agenda

- Introduction to PHY
- Elastic Buffer Functionality & SKP Handling
- Challenges in Testing Elastic Buffer
- Verification Approach
- Typical Scenarios
- Debugging Techniques
- Coverage space
- Results

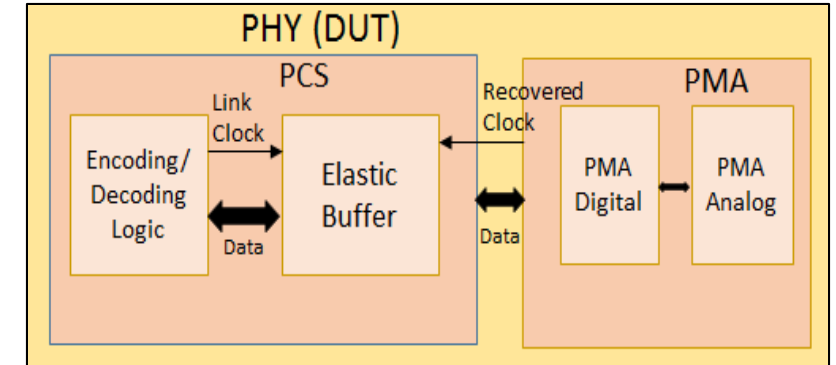
Introduction

- MOST High Speed Serial Interface protocols typically constitute:
 - Functional layers
 - Transport/Protocol Layer
 - Link Layer
 - Physical Layer
- Physical layer(PHY) deals with:
 - Physical connectivity, Electrical Characteristics
 - Supporting Link Layer with some protocol related features



PHY Introduction

- Physical layer(PHY) has 2 parts:
 - Physical Media Attachment (PMA)
 - Physical Coding Sub-layer (PCS)



- PMA majorly responsible for: Serialization/Deserialization(SERDES) and Clock & Data Recovery(CDR)
- PCS majorly responsible for Scrambling(Optional), Encoding/Decoding and maintaining Clock Tolerance Compensation(CTC)

Clock Frequency Variations

- Transmitters and Receivers usually have individual clock sources separated by Channel
 - SSC, Jitter, PPM Offset are common factors for frequency deviation
- For eg: Worst case frequency difference for USB among the transmitter and receiver clocks can be as high as 5600 ppm.
- Jitter will also deviate the bit clock period slightly from the actual UI width

Protocol	SSC Modulation rate	Maximum SSC Deviation	PPM offset	Worst case frequency difference
USB	30 to 33 KHz	-4000ppm to -5000ppm	-300ppm to +300ppm	+300 to -5300ppm
PCIe(Separate Ref CLKs)	30 to 33 KHz	-4000ppm to -5000ppm	-300ppm to +300ppm	+300 to -5300ppm
SATA	30 to 33 KHz	-4000ppm to -5000ppm	-350ppm to +350ppm	+350 to -5350ppm

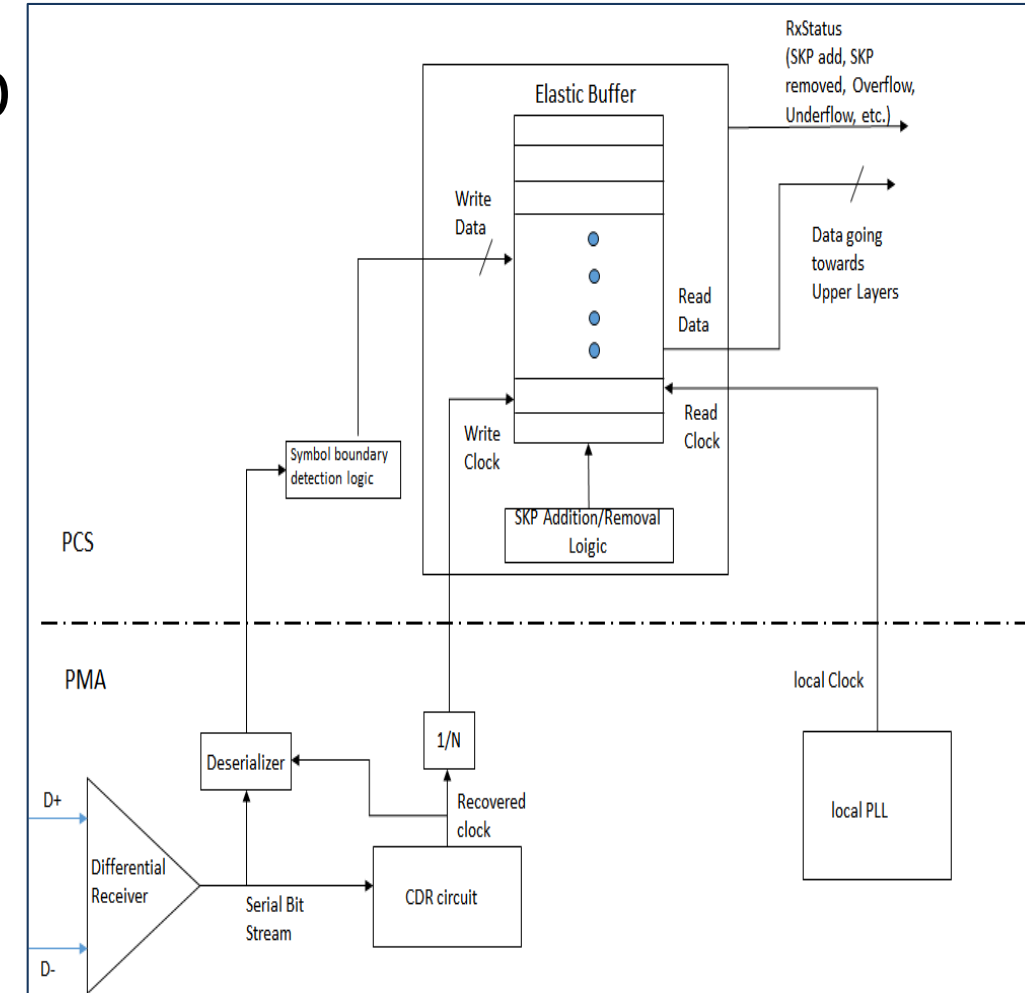
Special Symbol –SKP(USB)

- USB uses special symbols called SKPs to handle CTC in EB.
- Symbol: Collection of 8bits (before encoding)
- SKP Symbol: Used to balance out the Clock Frequency difference on both sides of the link; depending on protocol.
- Inserted by TX into the Data Stream at suitable places.
- Ignored by Link Layer.
- SKP ordered set: Collection of multiple SKP symbols.

Protocol	SKP Symbol value	SKP Ordered Set
USB Gen1	3C	2 SKP Symbols
USB Gen2	CC	12 SKP + SKP_END+ 3 LFSR Symbols
PCIe Gen1 to 2	1C	COMMA+ 3 SKP
PCIe Gen3 and above	AA	12 SKP + SKP_END+ 3 LFSR Symbols

Elastic Buffer Functionality

- Elastic Buffer (EB) is an asynchronous FIFO
- Acts as a bridge between the 2 separate clock domains – the Recovered Rx Clock and the Local PLL clock.
- SKP Handling Logic : addition and removal
- Optionally maintains Read and Write Pointers.



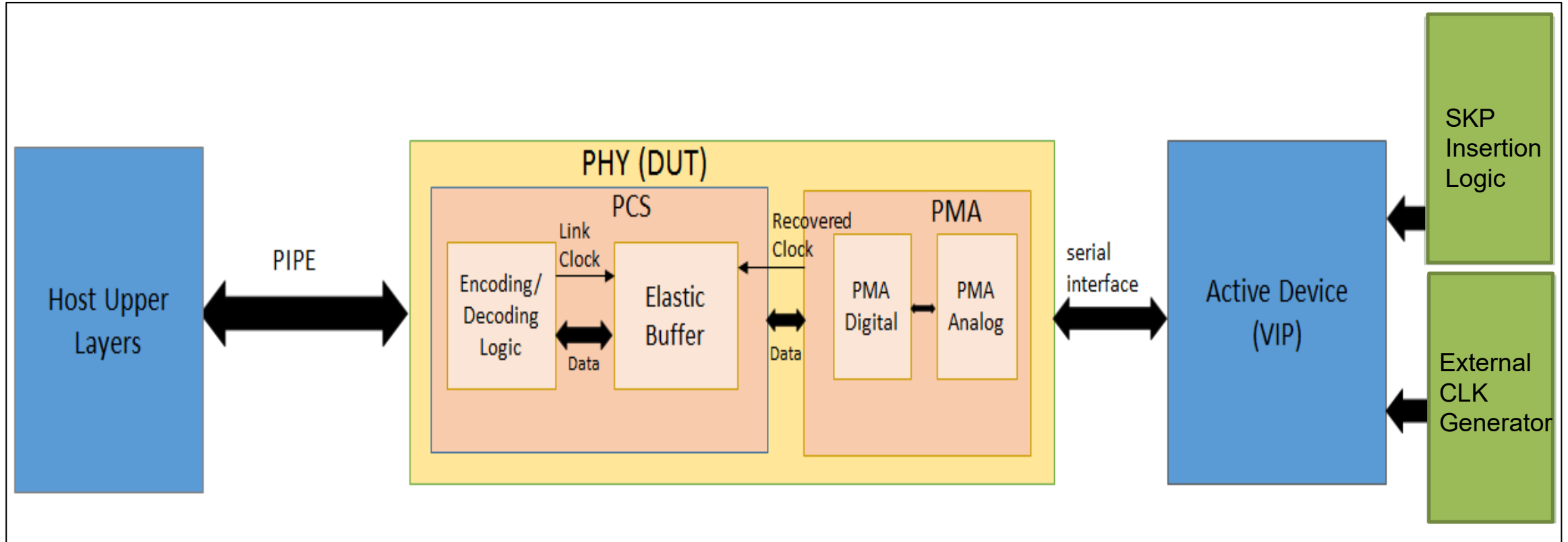
Verifying Elastic Buffer

- Elastic Buffer operates on 2 Clock Domains:
 - Write Clock, Recovered from received Serial Data Stream.
 - Read Clock from Local PLL.
- To effectively test EB, the Write/Read pointers needs to be moved suitably w.r.t. each other
- Factors playing major role in controlling pointers:
 1. **Write Clock period**: Can be achieved by having frequency variation in the Rx serial Data
 2. **Read Clock period**: Can be achieved by enabling SSC in the local PLL
 3. **SKP Symbols** : Can be achieved by varying number, length and position of SKP symbols/Ordered sets in the received serial data.

Challenges in EB Verification

- UI variation: Getting the desired frequency variation in the serial data-bit stream received by PHY
 - Needs control over several complex factors like SSC, jitter, PPM offset, Ref. Clock variation etc.
- SKP Handling: SKP insertion at designated data symbols/blocks, depending on rates.
- Ability to simultaneously select random SSC profile along with the dynamic handling of SKP insertion

TB Setup



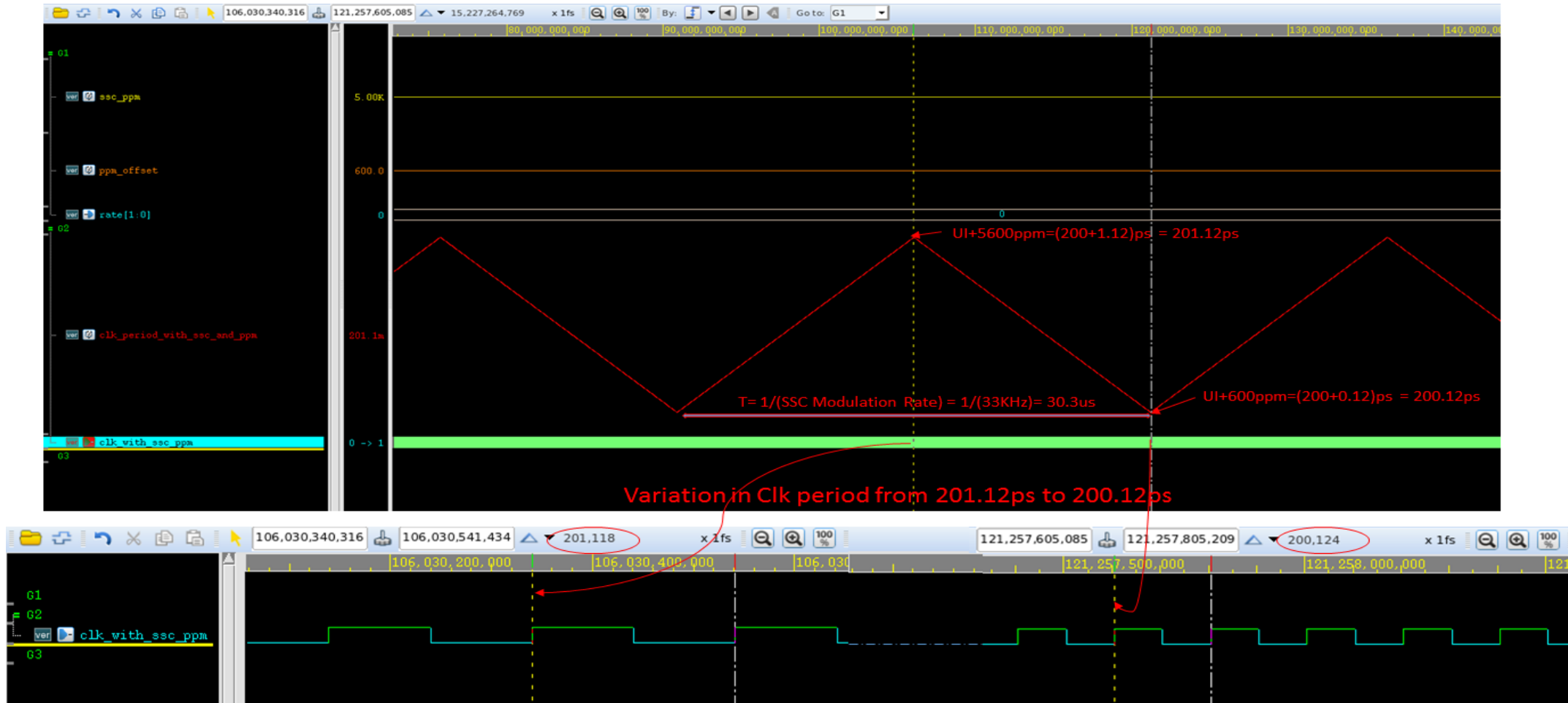
External CLK Generator

- A portable and reusable SV module, giving clock of desired rate
- Connected to Device BFM for controlling UI of serially transmitted data
- External CLK parameters
 - Rate or speed(USB): Gen1 - 5Gbps or Gen2 - 10Gbps
 - SSC: Modulation rate - 30KHz to 33KHz , Max Frequency Deviation- 5000ppm
 - PPM Offset: Fixed offset - 0 to 600 ppm
 - Jitter: Depends on Jitter Budgeting; Periodic Jitter(Pj) has been modeled. Other kinds of Jitter can also be added if necessary.

External CLK Generator(contd...)

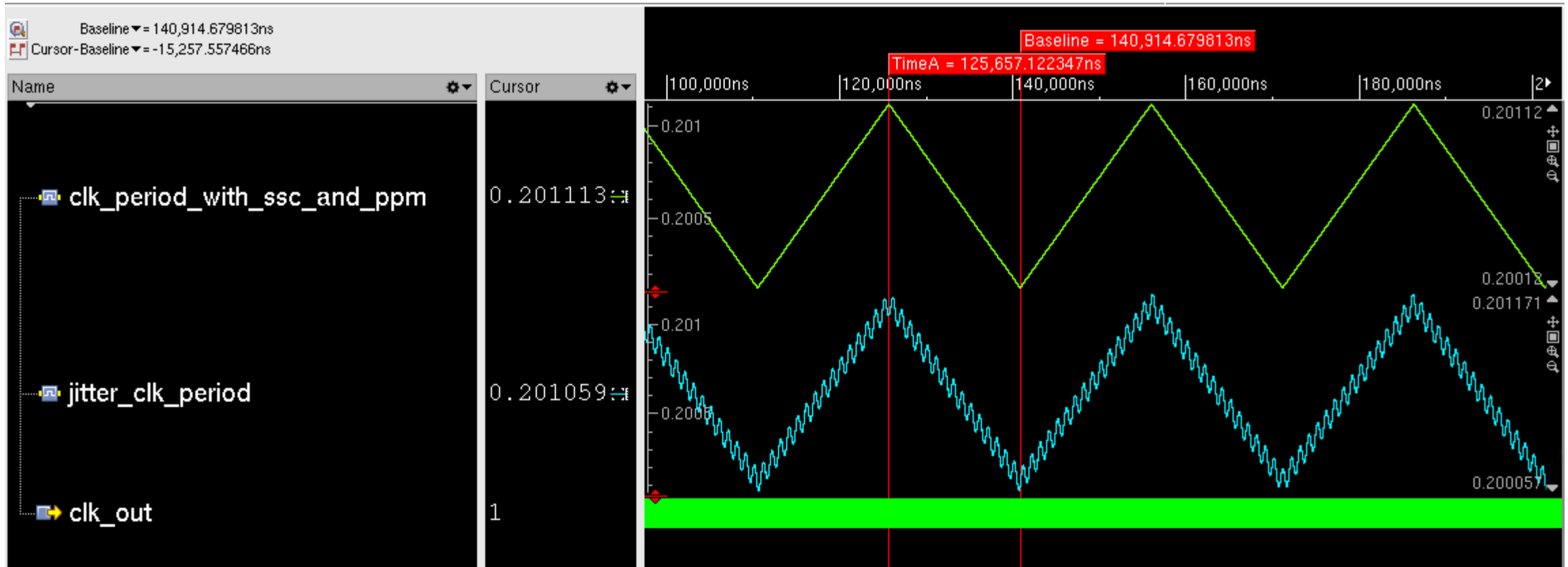
- If maximum frequency deviation due to SSC = 5000ppm (downspread), then the UI should rise from 200ps (Ideal UI) to 201ps [$\text{Ideal UI} + 200 \times (5000/10^6)$] and then again fall back to 200ps.
- In Gen1 speed, Suppose during simulation, there is no ppm offset on DUT side, then in order to account for a possible -300ppm offset on the read CLK and +300ppm offset on write CLK, one can configure the external CLK with a fixed PPM offset of +600ppm (or $200 \times (600/10^6) = 0.12\text{ps}$).
- Now the UI profile due to SSC + ppm offset would rise from 200.12ps to 201.12ps

External CLK Generator(contd...)



Variation of External Clk UI profile with **SSC** and **PPM** offset

External CLK Generator (contd...)



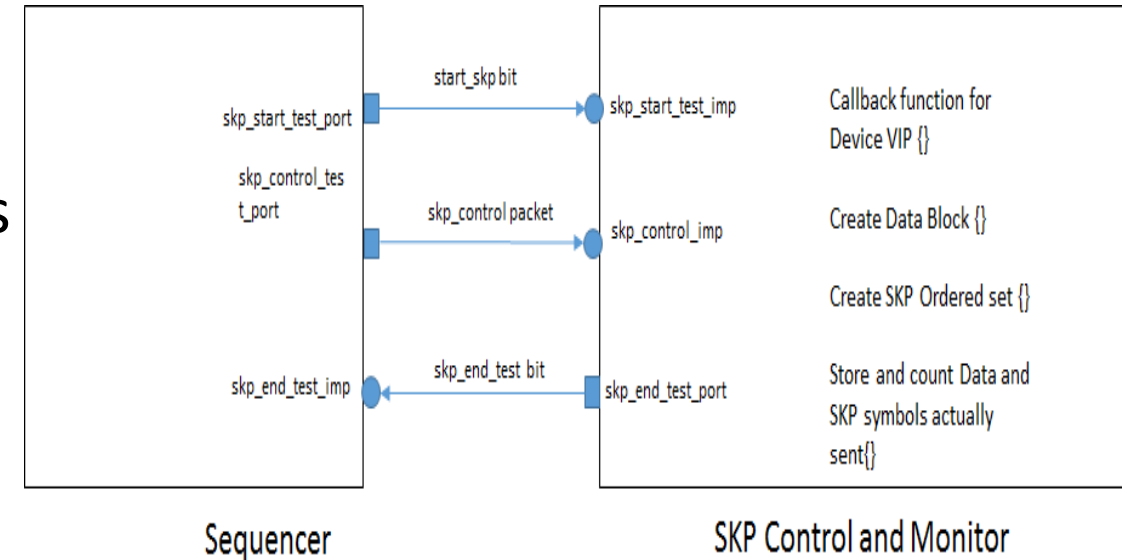
External Clk UI profile with **SSC**, **PPM** Offset and added **Periodic Jitter**

USB SKP Insertion & Reception

- Partner should transmit:
 - USB Gen1(5 Gbps speed): 1 Gen1 SKP ordered set every 354 symbols
 - USB Gen2, (10 Gbps speed): 1 Gen2 SKP Ordered set every 40 blocks
- Worst case scenario:
 - Inserting 4 SKP Ordered sets after 1416 symbols in Gen1.
 - Three SKP Ordered Sets after 120 blocks in Gen2.
- Usually EB can add/remove SKP only when there are SKP symbols on Received Serial Data
- Re-timers present between source and destination can also add/remove SKP symbols as needed

Customizable Skip Insertion Logic (contd...)

- Callbacks have been used to customize the size of the SKP ordered sets and their positions in the data stream.
- Starting point for counting SKP intervals is controlled from the sequencer.
- Sequencer and the SKP control_monitor are connected through multiple analysis ports as illustrated in fig.
- Create symbols/blocks using custom function `create_data_block{}` and start injecting them into the Transmission Queue of the Device BFM.



Customizable Skip Insertion Logic (contd...)

- Keep Counting the symbols/blocks being injected.
- Desired number of SKP symbols/Ordered sets (as targeted or randomized) are injected into Transmission Queue of the Device BFM
- SKP ordered set of required length is made using the custom function create_skp_block{}
- No. of SKP intervals, no. of SKPs in each SKP ordered set, no. of data symbols/blocks coming before SKP ordered SET are all assigned to the skp_control packet -> ported from the sequencer to the SKP Control and Monitor block through skp_control_test analysis port.

```
class skp_control_pkt_c extends uvm_sequence_item ;

    bit gen1_skp_control ;
    int  gen1_num_skp_interval ;
    int  gen1_num_skp_sym_arr[] ;
    int  gen1_num_data_sym_arr[] ;

    bit gen2_skp_control ;
    int  gen2_num_skp_interval ;
    int  gen2_num_skp_blk_arr[] ;
    int  gen2_num_sym_per_skp_blk_arr[] ;
    int  gen2_num_data_blk_arr[] ;

    `uvm_object_utils_begin(skp_control_pkt_c)
    `uvm_object_utils_end

    function new (string name = "skp_control_pkt_c");
        super.new(name);
    endfunction : new

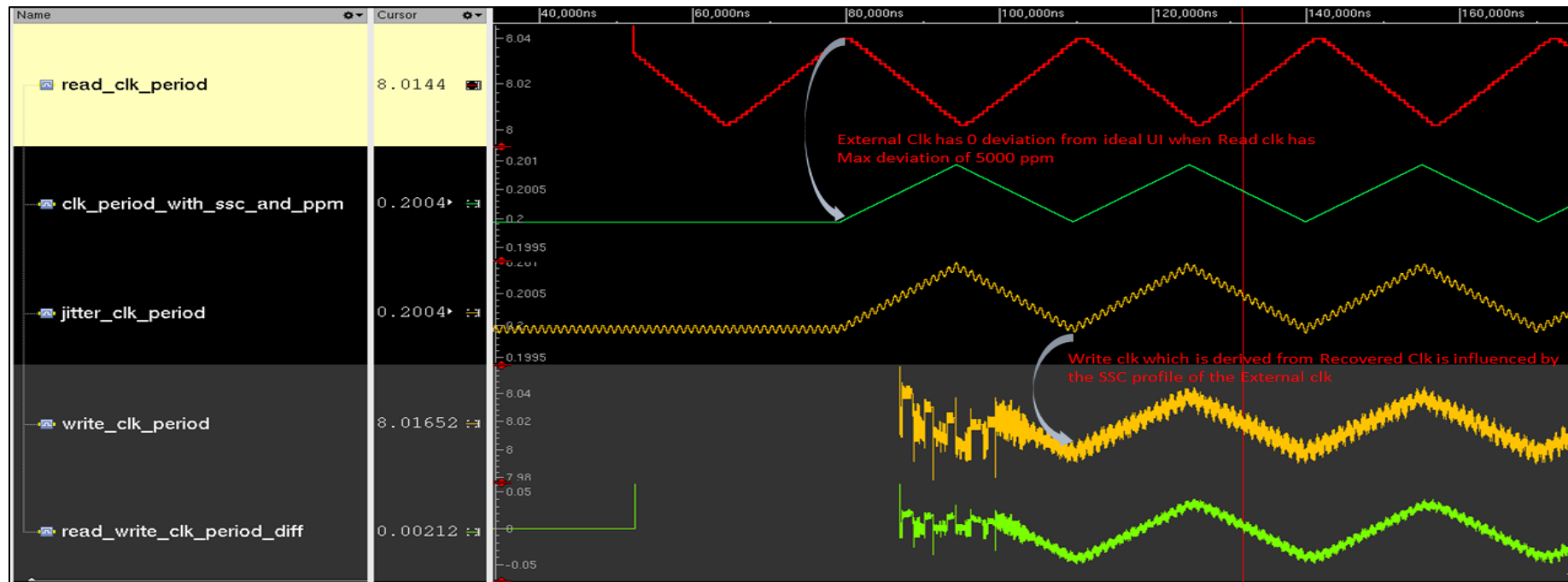
endclass: skp_control_pkt_c
```

Typical Scenarios

- Normal data flow
- Testing at Protocol Boundary
- Error Scenarios: Overflow, Underflow Custom Scenarios for Silicon Testing

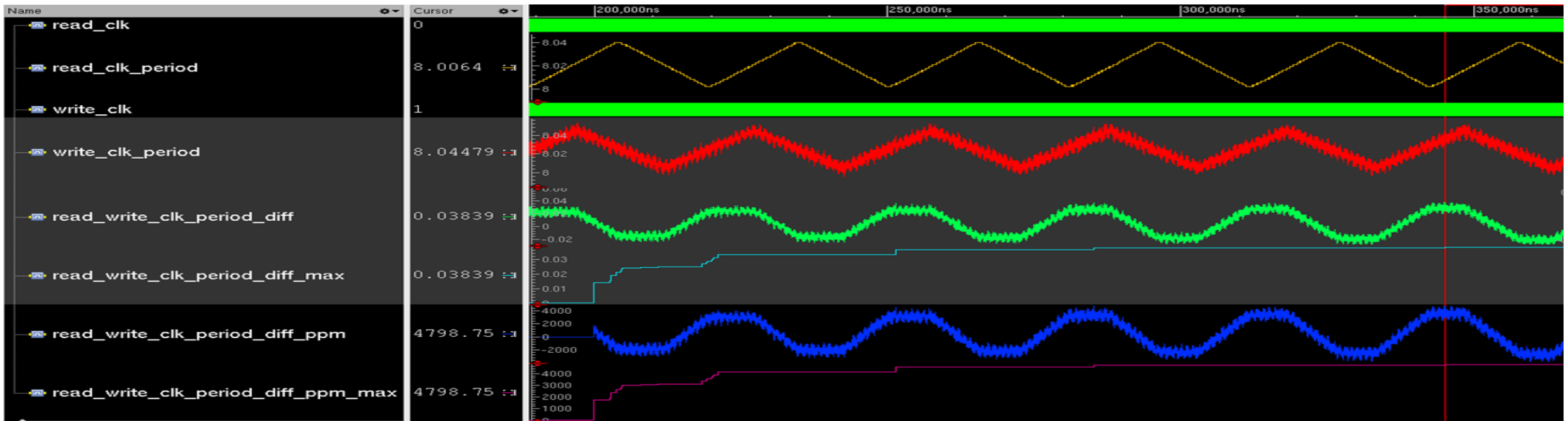
Scenario: Creating Frequency Deviation

- Realtime scenario: SSC “ON” on both Transmit and receive side.
 - Create frequency deviation between. Read and write clocks.
 - Max Deviation: Shift the UI profile of the recovered CLK or write CLK of the EB with respect to the local CLK of the DUT or read CLK of the elastic buffer



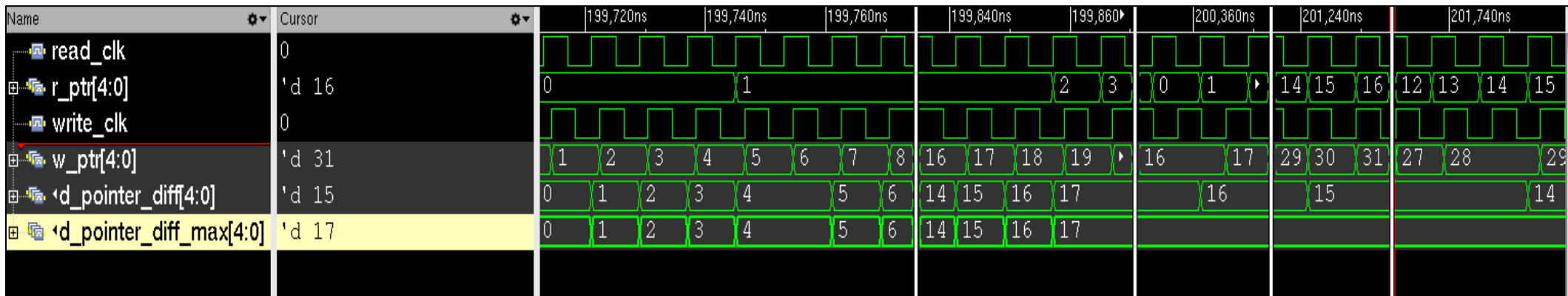
Debugging using Signals

- Creating TB Signals and Plotting Parameters:
 - To Cover scenarios involving different range of frequency deviation between the 2 CLKs. This would be further confirmed by functional Coverage.



Checks and Assertions on Pointers

- Monitoring movement of Read and Write pointers of Elastic Buffer and EB depth to check the following:
 - Pointer difference direction needs to be matched with direction of frequency deviation between Read and Write CLK of EB.
 - Read & Write pointers should go to their initial/default states, after RxStatus errors like Overflow or Underflow



SKP Checking

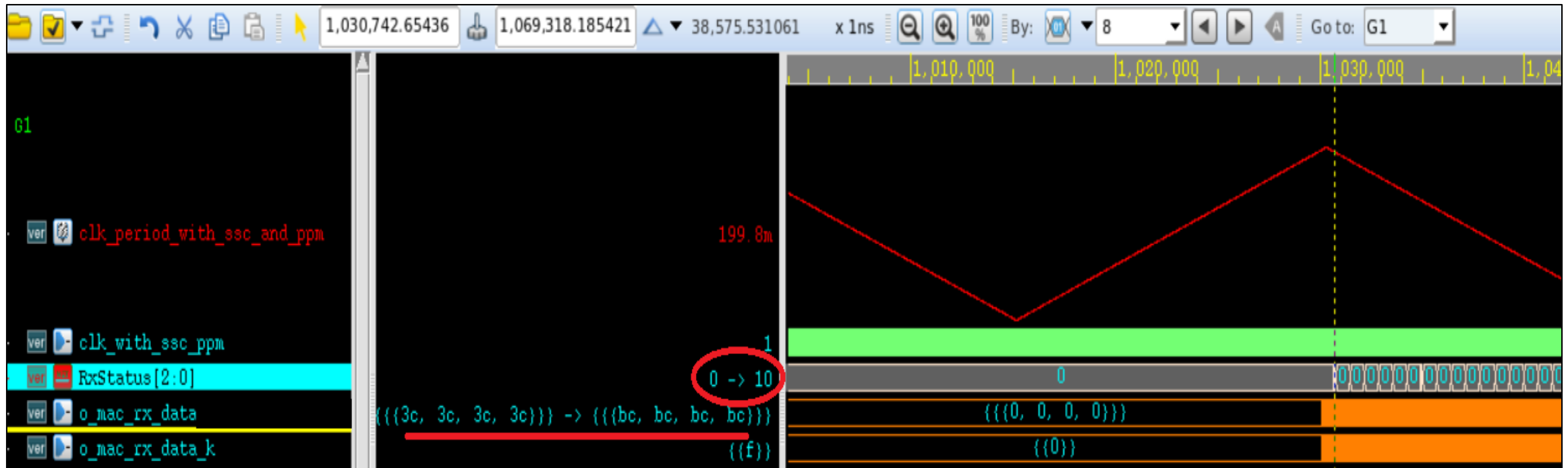
- Monitoring SKP count:
 - For USB Gen1, protocol mandates that only 1 SKP Ordered set can be added or removed.
 - For USB Gen2, SKP added or removed should be multiples of 4 symbols
 - SKP monitoring Block checks whether these conditions are fulfilled by sampling SKPs transmitted by Device BFM and received at the RxData of DUT(PHY)

Coverage space

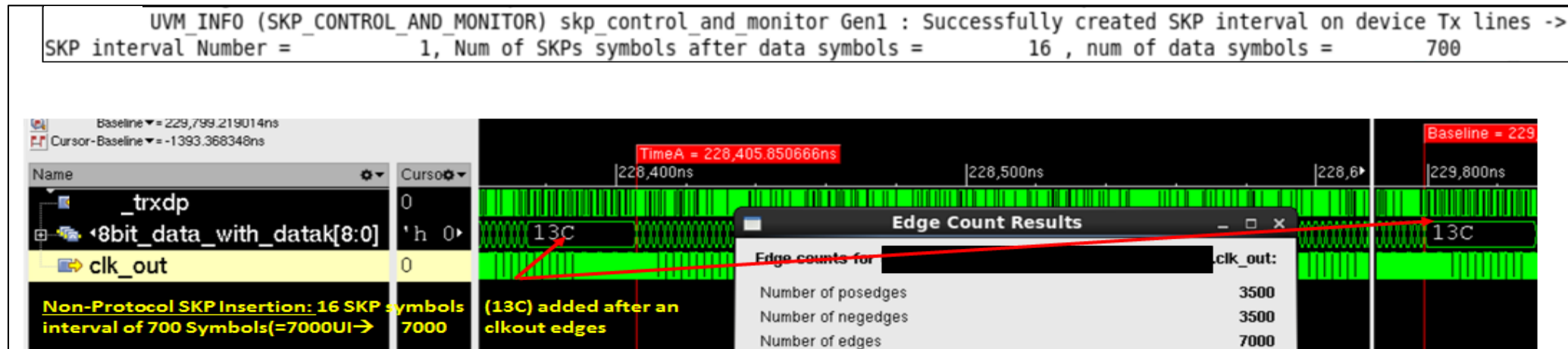
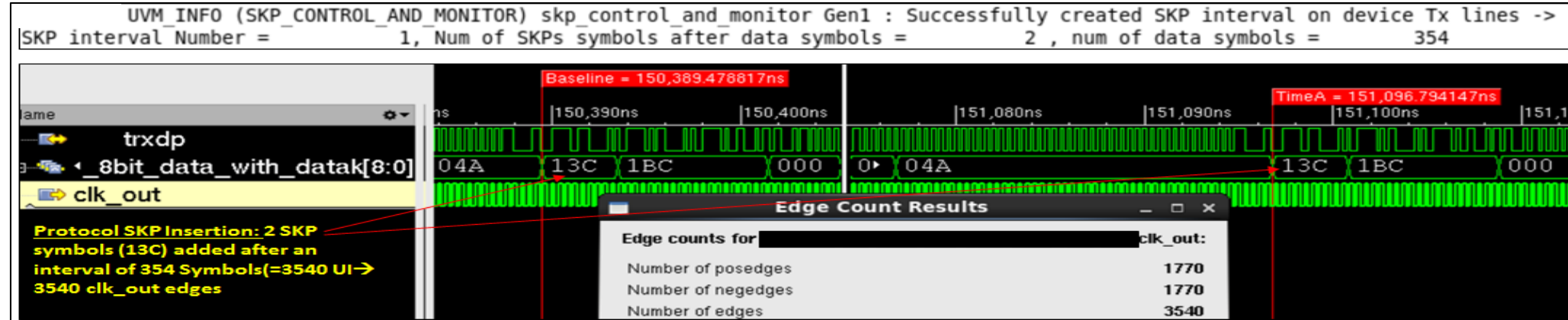
- In order to thoroughly test all possible scenarios, functional Covergroup including coverpoints for configurable parameters related to External clock and SKP insertion were created
- Buffer modes: Nominal Half-full or Nominal-empty
- Error Scenarios: Overflow, Underflow
- To test all the related CLK and SSC combinations, proper cross coverages were also created.
- Flexibility in terms of all the configurable parameters: proper switches created so that one or multiple CLK features such as SSC, PPM or Jitter can be turned on or off for particular directed or corner scenarios.

Results

PCS- SKP removal to avoid overflow

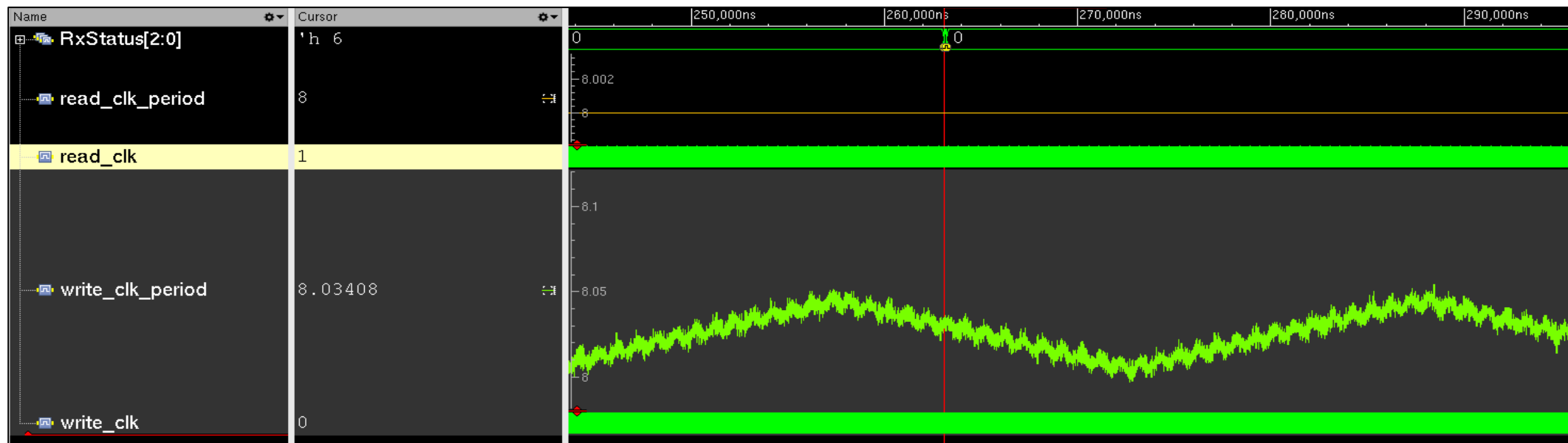


PCS- Custom SKP Insertion



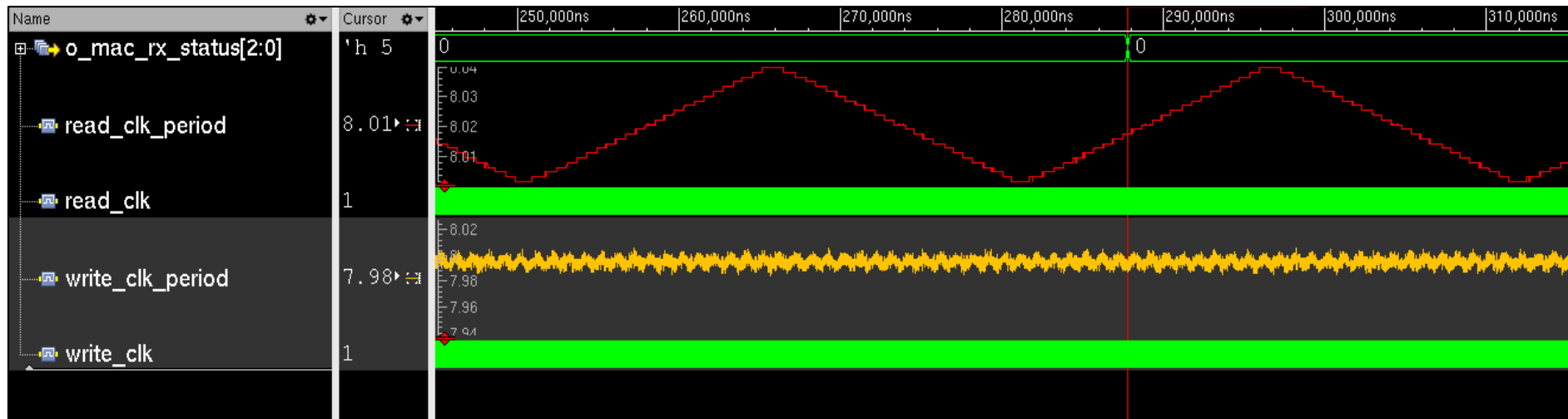
Underflow

- DUT Clk(read_clk) is SSC disabled, External CLK modulates Device TX UI with a fixed offset of 600ppm, SSC of 33 KHZ ranging from 0 to 5000ppm which ultimately reflects on write_clk.
- SKP ordered sets were being sent after more than 1416 symbols have been transmitted.



Overflow

- DUT (Read) CLK has SSC of 33 KHZ ranging from 0 to 5000ppm, External CLK modulates Device TX UI with a fixed offset of -600ppm and hence the write_clk also has only -600ppm offset.
- SKP ordered sets were being sent after more than 1416 symbols have been transmitted



Questions