Cadence vManager Platform and Virtuoso ADE Verifier
Leading-edge technologies provide methodology for mixed-
signal verification closure

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Motivation

- Many projects need analog, digital, and mixed-signal verification
- Requirements-driven verification needs top-down verification planning
- Standards like IEC 61601 (medical equipment), ISO 26262 (automotive), etc. require a bottom-up results reporting, traceability and tracking
- Domain-specific solution provided by Cadence
  - vManager™ Metric-Driven Signoff Platform
  - Virtuoso® ADE Verifier
- Project success requires
  - A common signoff criteria for the entire project
  - Ability to create and refine a verification plan across analog and digital domains
  - Formal way for team interactions (interface definition, spec values, assumptions...)
  - Common view of the results and traceability into the entire tool flow
Design Complexity

Line between what is an IC and what is a System is fading

More than Moore

Analog Design Complexity

Analog/RF Power Sensors Fluidics
Analog RF

MEMs

Photonics, RF

Imaging

CMOS Analog / RF

More Moore

Process Node Complexity

180nm 130nm 90nm 45nm 28nm 22nm 16nm 10nm 7nm 5nm 3nm

More Moore

GPU

CPU

FPGA

NAND

Mixed-signal

Imaging

Photonics, RF

RF

MEMs

Analog

Analog/RF Passives Fluidics

Sensors

Analog

Analog/RF
**Production Goals Alignment**

You can’t view the design task in isolation anymore.

**Chip Architect**
- Translate customer/business goals to specific design measurements
- Distribute design tasks, track and report progress

**Product Engineer**
- Improper handoffs lead to expensive fixes, missed schedules, and goal misalignment

**Design Engineer**
- Determine physical layout impacts on design specifications

**Layout Engineer**
- 

x 3

x 4

x 10

x 20
Design Verification Quality
Are you ever really sure you got everything?

- Analog verification is often randomly intermingled with the design flow
- Designers may use Virtuoso® ADE Assembler without specification limits defined
- Updates are difficult to track and can slip through

Ad hoc status
Did everyone update the spreadsheet?

Test targets
Did you get them all?

Manual updates and analysis
Did you get the latest updates?

Results(?)

What's needed to sign off?

Medical

Automotive

Consumer
Requirements-Driven Mixed-Signal Verification

Bridge the verification gap between analog and digital domains

**Requirements**

**Cadence® vManager™**

SoC Planning & Results Collection

**System Development Suite**

**Digital planning/execution**

**Digital Simulation & Emulation**

**Accellera**

**Systems Initiative**

**DVCon Europe 2019**
Requirements-Driven Mixed-Signal Verification

Bridge the verification gap between analog and digital domains

Analog specifications can be managed via Excel spreadsheet

Analog and digital specifications and results can be co-managed and synched using the vManager™ Metric-Driven Signoff platform

Familiar domain working environments
Cadence vManager Platform and MDV Methodology
1. MDV provides **schedule predictability**
   - As much as 50% uncertainty in most projects
   - Answers the question – “are we done yet?”
   - MDV uses plan-to-closure proven process

2. MDV offers **verification productivity**
   - Execute on optimized engines / combine results
   - Reduction in test time and farm utilization

3. MDV provides **improved quality**
   - Verification consistency thru all levels of abstraction
   - Direct measurement of quality thru metrics
Metric-Driven Verification (MDV)
Planning and management with unified verification metrics

Failure and Metric Analysis

Done

Signoff?

Yes

No

Plan

Construct

Measure and analyze

Execute

Results/Coverage

Metric definitions

Testbench
Tests
Checks
Coverage
Mixed-signal : Metric-Driven Verification (MDV)

All stakeholders

Digital Team

vManager™
Platform

Analog Team
## Analysis Center

![Analysis Center Window](image)

### Metrics Display

<table>
<thead>
<tr>
<th>Name</th>
<th>Overall Average Grade</th>
<th>Overall Covered</th>
<th>Assertion Status Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>vManager no-prabha3001 (64) (Analysis - Metrics)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Details**

- **Overall**
  - Code
  - Block
  - Statement
  - Expression
  - Taggle
  - PSM

- **Functional**
  - Assertion
  - CoverGroup

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While you didn’t plan for it, you notice there are some cross coverage elements as well. Create respective planned coverage for these items and go ahead and map those as well.
Virtuoso ADE Verifier
Overview of the Virtuoso ADE Product Suite

Right tool for the right job

• Virtuoso ADE Explorer
  – Highly interactive, single testbench analyzer that assists engineers at the earliest stages of circuit design

• Virtuoso ADE Assembler
  – Interactive, multi-testbench environment that is designed to pull together all the parts of the design and their various specs to begin centering the design for manufacturing

• Virtuoso ADE Verifier
  – Introduces a formalized method for doing overall electrical specification verification of analog circuits

• Virtuoso Variation Option
  – Extensive statistical verification for designs requiring high-sigma validation and for advanced nodes
Virtuoso ADE Verifier
Enabling analog coverage within the new Virtuoso ADE Product Suite

- Project-level verification management
  - Plan-based verification for analog designs
  - Enabling results traceability
  - Excel import/export

- Top-down requirements driven analog verification flow

- Visibility and reporting of analog coverage metrics
  - Result traceability to track progress

- Regression running capabilities enable more automated verification
Engineers can import specification titles, values, ownership, etc. from a spreadsheet into ADE Verifier.

Post-simulation and evaluation, the data can be exported back to the original Excel spreadsheet or hyperlinked html-based datasheets can be created.
Analog Coverage Driven Verification Methodology

Setup Library Assistant facilitates uniformity in a multi-user sharing and coverage environment.

Coverage is the metric to measure completeness of your analog verification in reference to the defined goals.
Use Virtuoso ADE Verifier to Manage Very Large Verification Problems

• Virtuoso® ADE Verifier can be used hierarchically to efficiently monitor large groups of design engineers working on different pieces of the complete chip

• Distribution provides performance gains using a highly parallel infrastructure
Why Use Virtuoso ADE Verifier?
Create analog coverage metrics necessary for certification

- Virtuoso ADE Verifier approach
  - Increases analog verification quality and efficiency
  - Provides designers with guided and verifiable methodology
    - A requirement of every ISO standard
  - Manages larger verification projects
    - Assume you have a project with 10 engineers each supporting 5 ADE Assembler suites of tests – ADE Verifier allows you to keep a real-time project overview
Requirements-Driven Mixed-Signal Verification
Bridge the verification gap between analog and digital domains

- Analog specifications can be managed via Excel spreadsheet
- Analog and digital specifications and results can be co-managed and synched using the vManager™ Metric-Driven Signoff platform

Familiar domain working environments

Digital simulation and emulation

System Development Suite

Analog/MS Simulators

Virtuoso ADE Assembler

Virtuoso® ADE Verifier

Analog planning/execution

Cadence® vManager™ SoC Planning & Results Collection

Digital planning/execution
Demo Example
Demo: Mixed-Signal Design Architecture and Configuration

Features Specification

<table>
<thead>
<tr>
<th>Features</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>RISC / 160Mhz</td>
</tr>
<tr>
<td>Memory</td>
<td>SRAM 4KB</td>
</tr>
<tr>
<td>HBUS</td>
<td>160 Mhz</td>
</tr>
<tr>
<td>JTAG</td>
<td>25Mhz</td>
</tr>
</tbody>
</table>

F. CLOCK
CLOCK Lock <=45us
VDD_AON 1.25V ± 0.2V
VDD_PROC 0.9V ± 0.1V
vPlan: Defined, Agreed Goals and Metrics for Entire Team

Define
- Design Features
  - Requirements Management System

Outline from a Functional Spec

Brainstorming
Common Understanding of All Stakeholders

Define
- Tests
- Coverage needs
- Checks

Triple Check VIP vPlans

accellera
SYSTEMS INITIATIVE
Develop the vPlan
Starting Point Top-Level Structure

- LPMS_SoC
  - 1 Core features
  - 2 Interface
  - 3 Functional feature
Functional Feature AKA Black-Box Feature

- LPMS_SoC
  - 1 Core features
  - 2 Interface
  - 3 Functional feature
    - 3.1 Describe the black-box functionality of the DUT
Interface

LPMS_SoC
- 1 Core features
- 2 Interface
- 3 Functional feature

LPMS_SoC
- 1 Core features
- 2 Interface
  - 2.1 JTAG_VIP
  - 2.2 HBUS
  - 2.3 Power supply
- 3 Functional feature

LPMS_SoC
- 1 Interface
  - 1.1 JTAG_VIP
  - 1.2 HBUS
  - 1.3 Power supply
    - 1.3.1 External voltage regulator
- 2 Core features
- 3 Functional features
Mixed-Signal Planning for Power Supply

- LPMS_SoC
  - Interface
    - JTAG_VIP
    - HBUS
  - Power supply
    - External voltage regulator
      - RNM
      - External current exceeds 50 mA
  - Core features
  - Functional features

- Expand Sub Tree
- Collapse Sub Tree
- Clear Filters
- Copy Cell
- Copy Row
- Add section as sibling (Ctrl+B)
- Add section as child (Insert)
- Add new planned coverage (Ctrl+G)
- Add new planned checker (Ctrl+K)
- Add new planned test case (Ctrl+T)
- Reference a vPlan (Ctrl+R)
- Find and Replace
- Reload referenced vPlan
- Import vPlan
- Delete (Delete)
- Indent (Tab)
- UnIndent (Shift+Tab)
- Cut (Ctrl+X)
- Copy (Ctrl+C)
- Copy as reference
- Paste (Ctrl+V)
- Paste as sibling
..and the Analog Requirements
Core Feature AKA White-Box Feature
Core features of VREG to be verified

- **2.1 VREG**
  - **2.1.1 LDOs**
    - 2.1.1.1 LDO_MASTER_VOUT
    - 2.1.1.2 LDO_AON_VOUT
    - 2.1.1.3 LDO_PROC_VOUT
    - 2.1.2 Bandgap
    - 2.1.3 Yield Verification (LDOs + BG) >98%

    - 2.1.1.1 LDO_MASTER_VOUT
      - 2.1.1.2.1 input voltage
      - 2.1.1.2.2 output voltage (1.1V - 1.5V)
        - 2.1.1.2.2.1 RNM
        - 2.1.1.2.2.2 Analog
      - 2.1.1.2.3 PSRR (< 2%)
      - 2.1.1.2.4 Startup time (< 500n)
      - 2.1.1.2.5 loading behavior (> 5m)
    - 2.1.1.3 LDO_PROC_VOUT
      - 2.1.1.3.1 input voltage
      - 2.1.1.3.2 output voltage (1.1V - 1.5V)
        - 2.1.1.3.2.1 RNM
        - 2.1.1.3.2.2 Analog
      - 2.1.1.3.3 PSRR (< 2%)
      - 2.1.1.3.4 Startup time (< 500n)
      - 2.1.1.3.5 loading behavior (> 5m)
Plan Assertion to Check..

- 2.1.1.2 LDO_AON_VOUT
  - 2.1.1.2.1 input voltage
  - 2.1.1.2.2 output voltage (1.1V - 1.5V)
  - 2.1.1.2.2.1 RNM
    - 2.1.1.2.2.2 Analog
    - 2.1.1.2.3 PSRR (< 2%)
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Plan Assertion to Check (cont’d)

2.1.1.2 LDO_AON_VOUT
  - 2.1.1.2.1 input voltage
  - 2.1.1.2.2 output voltage (1.1V - 1.5V)

  2.1.1.2.2.1 RN
  - 2.1.1.2.2.1.1 maximal negative slew for vout
  - 2.1.1.2.2.1.2 CHECK_MIN_NEG_VOUT_SLEW
  - 2.1.1.2.2.1.3 minimal negative slew for vout
  - 2.1.1.2.2.1.4 maximal positive slew for vout

  2.1.1.2.2.2 Analog
  - 2.1.1.2.3 PSRR (< 2%)
  - 2.1.1.2.4 Startup time (< 500n)
  - 2.1.1.2.5 loading behavior (> 5m)
Agreement on Analog Requirements...

- LDO_AON_VOUT
  - input voltage
  - output voltage (1.1V - 1.5V)
  - RNM

- Analog
  - PSRR (< 2%)
  - Startup time (< 500n)
  - loading behavior (> 5m)
Decide on the Domain

- 2.1.1.2 LDO_AON_VOUT
  - 2.1.1.2.1 input voltage
  - 2.1.1.2.2 output voltage (1.1V - 1.5V)
- 2.1.1.2.3 PSRR (< 2%)
- 2.1.1.2.4 Startup time (< 500n)
- 2.1.1.2.5 loading behavior (> 5m)
Initial vPlan

- **LPMS_SoC**
  - 1 Interface
    - 1.1 JTAG_VIP
    - 1.2 HBUS
  - 1.3 Power supply
    - 1.3.1 External voltage regulator
      - 1.3.1.1 RNM
      - 1.3.1.2 Analog
  - 2 Core features
    - 2.1 VREG
      - 2.1.1 LDOs
        - 2.1.1.1 LDO_MASTER_VOUT
        - 2.1.1.2 LDO_AON_VOUT
        - 2.1.1.3 LDO_PROC_VOUT
        - 2.1.2 Bandgap
      - 2.1.3 Yield Verification (LDOs + BG) >98%
    - 2.2 PLL
      - 2.2.1 CLK_FREQ
      - 2.2.2 Lock_Time
    - 2.3 MCU
      - 2.3.1 LowPower
        - 2.3.1.1 Core Power Mode Coverage
          - 2.3.1.1.1 Coverage
          - 2.3.1.1.2 Assertions
      - 2.3.2 PowerControlModule
        - 2.3.2.1 VCT Voltages
        - 2.3.2.2 UPF Supply Nets
        - 2.3.2.3 Isolation Signals
        - 2.3.2.4 Retention Signals
        - 2.3.2.5 Supply Set Sim States
    - 2.3.3 Processor
      - 2.3.3.1 SEQUENCER
      - 2.3.3.2 ALU
      - 2.3.3.3 DCACHE
      - 2.3.3.4 ICACHE
      - 2.3.3.5 REGISTERFILE
  - 3 Functional features
    - 3.1 Describe the black-box functionality of the design
Virtuoso ADE Verifier-vManager Connection Demo
Virtuoso ADE Verifier Uses the vManager Server Architecture

Virtuoso® ADE Verifier Client

vManager Client

Results DB

vAPI

Web Client

vManager Server

vPlan

Setting.v3 + Results
Summary
Summary: Virtuoso ADE Verifier

Analog, RF, and mixed-signal coverage is managed effortlessly.

Virtuoso® ADE Verifier

Analog Coverage Enhances Quality

Domain Bridging Reduces Complexity

Formalized Tracking Method Solves Integration Issues
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accelleras
SYSTEMS INITIATIVE

DSN DESIGN AND VERIFICATION
CONFERENCE AND EXHIBITION
EUROPE 2019
Summary

• Metric-Driven Verification (MDV) provides a framework for a formalized verification approach
  – Requirements-driven verification and verification planning is the starting point

• vManager™ Platform and Virtuoso® ADE Verifier provide domain specific solutions

• vManager and ADE Verifier connection
  – Bridges the gap between development environments
  – Enables combined analog, digital and mixed-signal verification methodology
  – Improves team communication

• The connection delivers a truly mixed-signal project management view
  – Traceability to fulfils quality needs, ISO 26262, ...
Questions