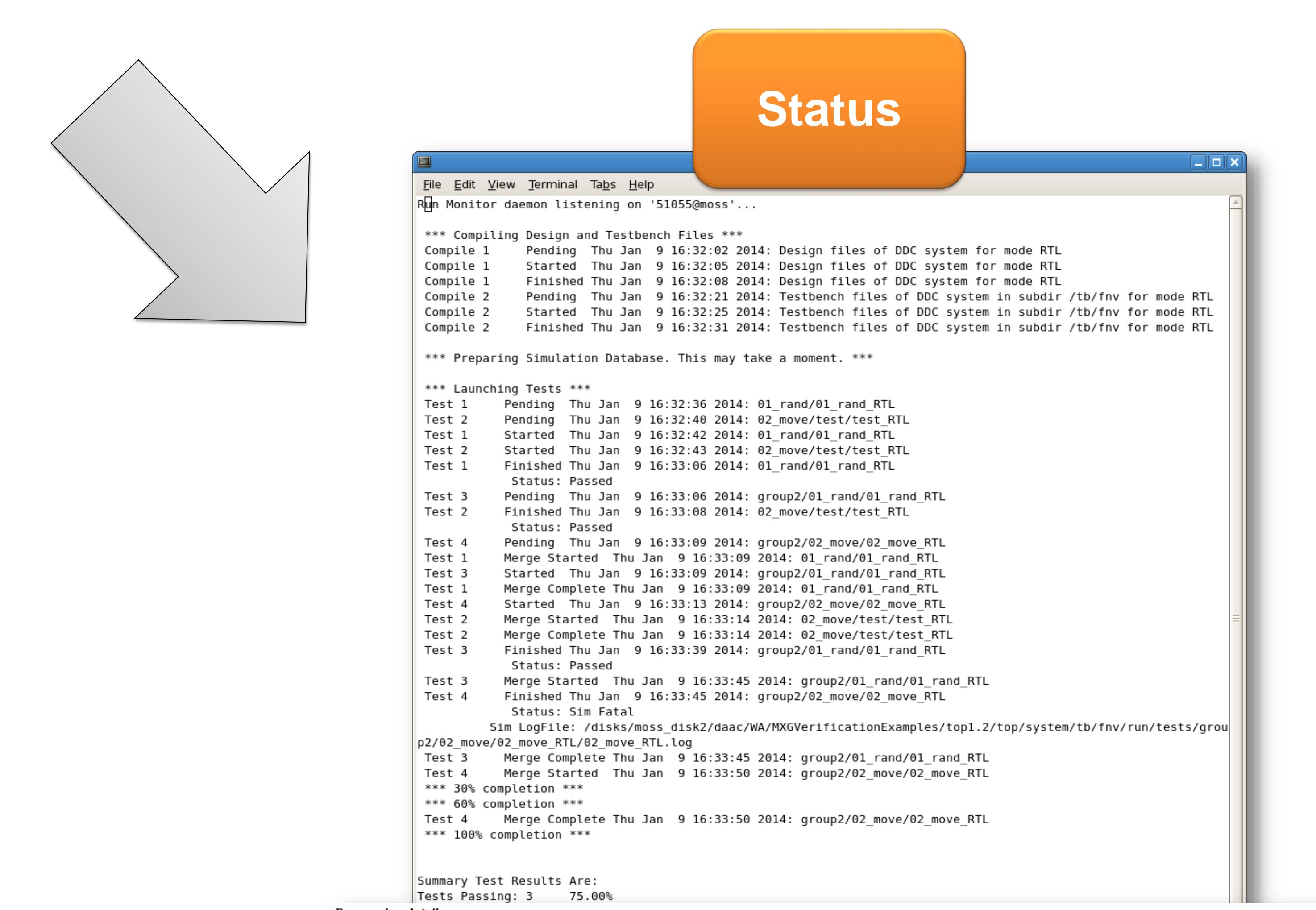
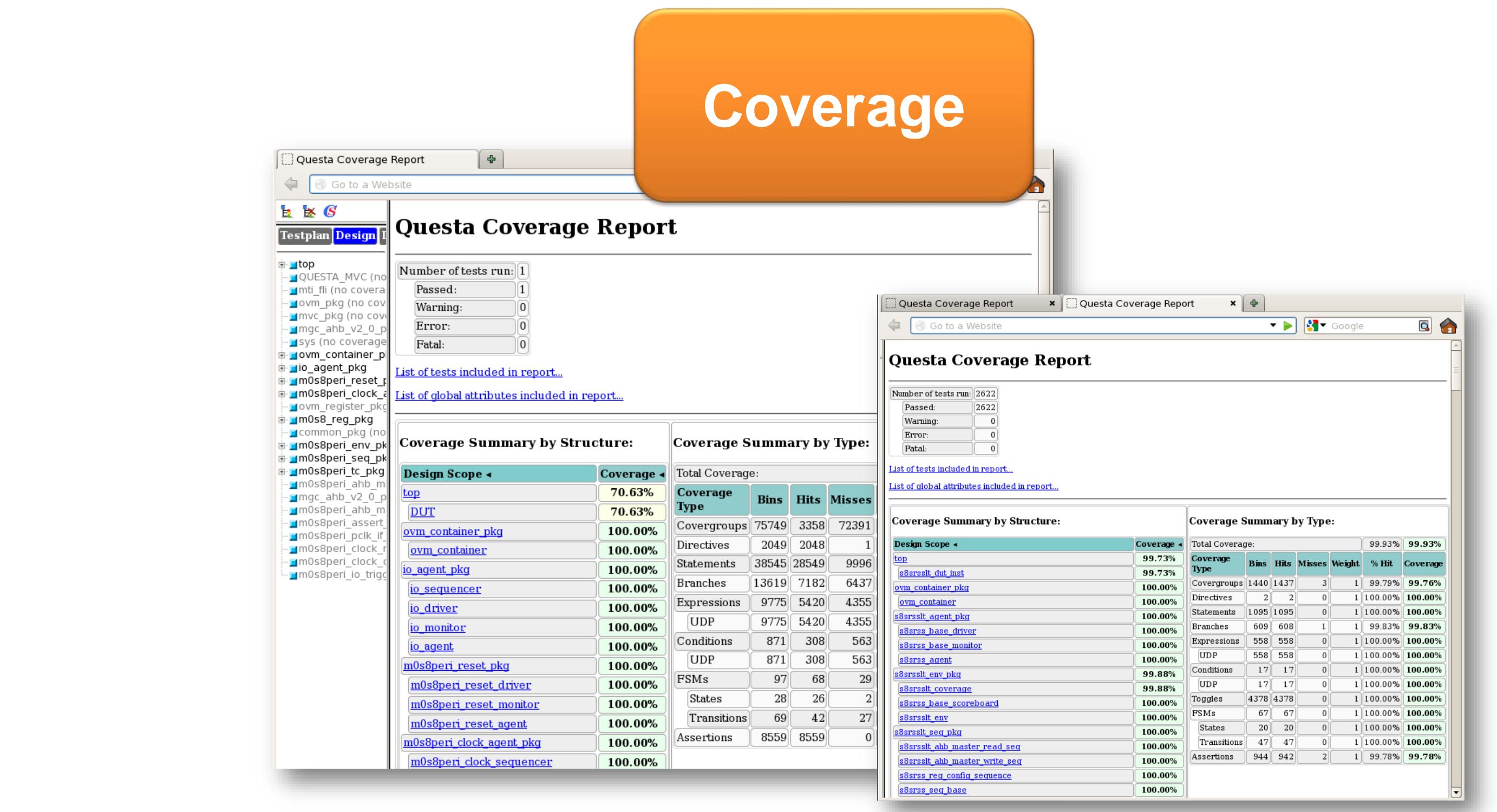
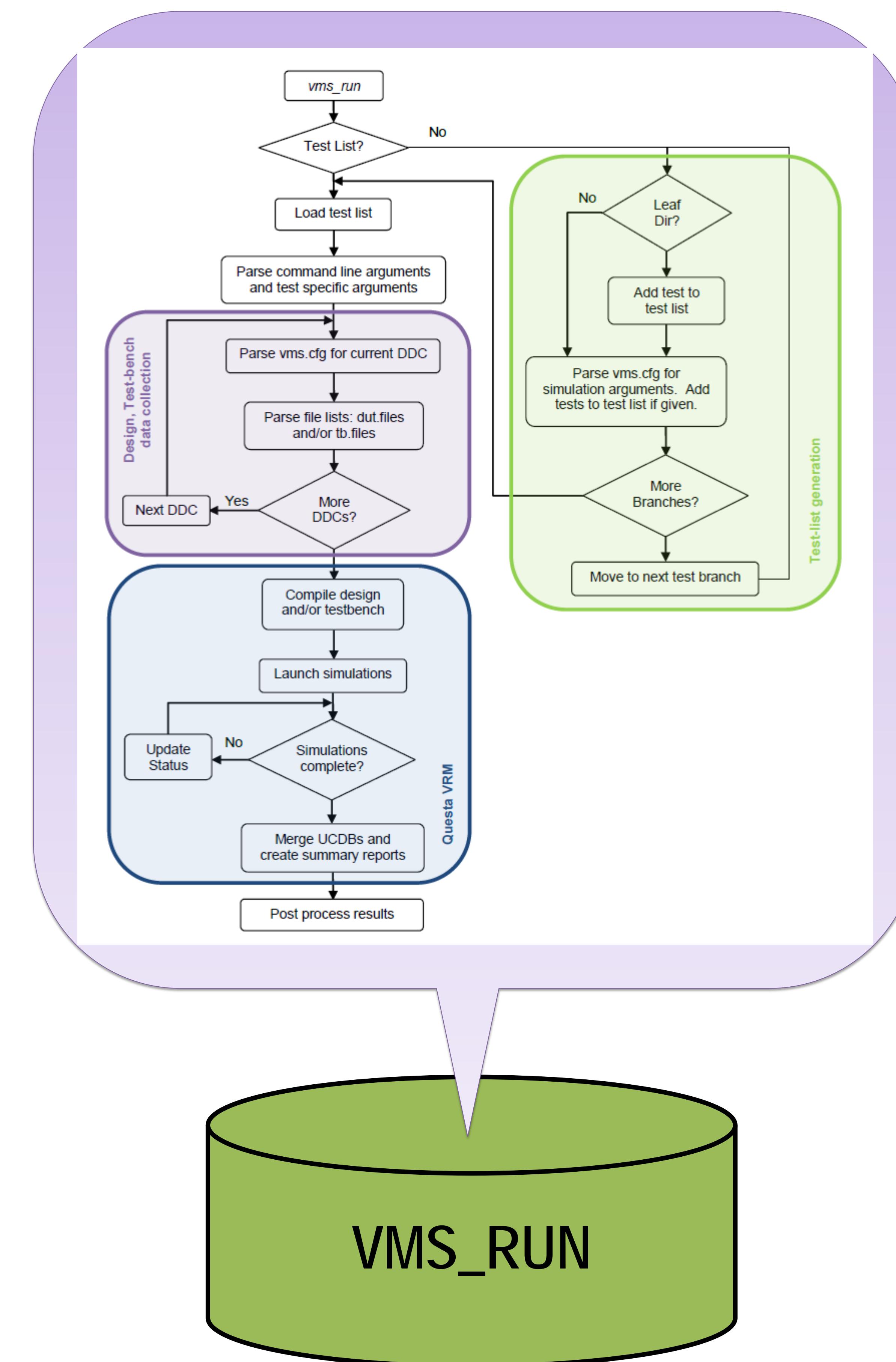
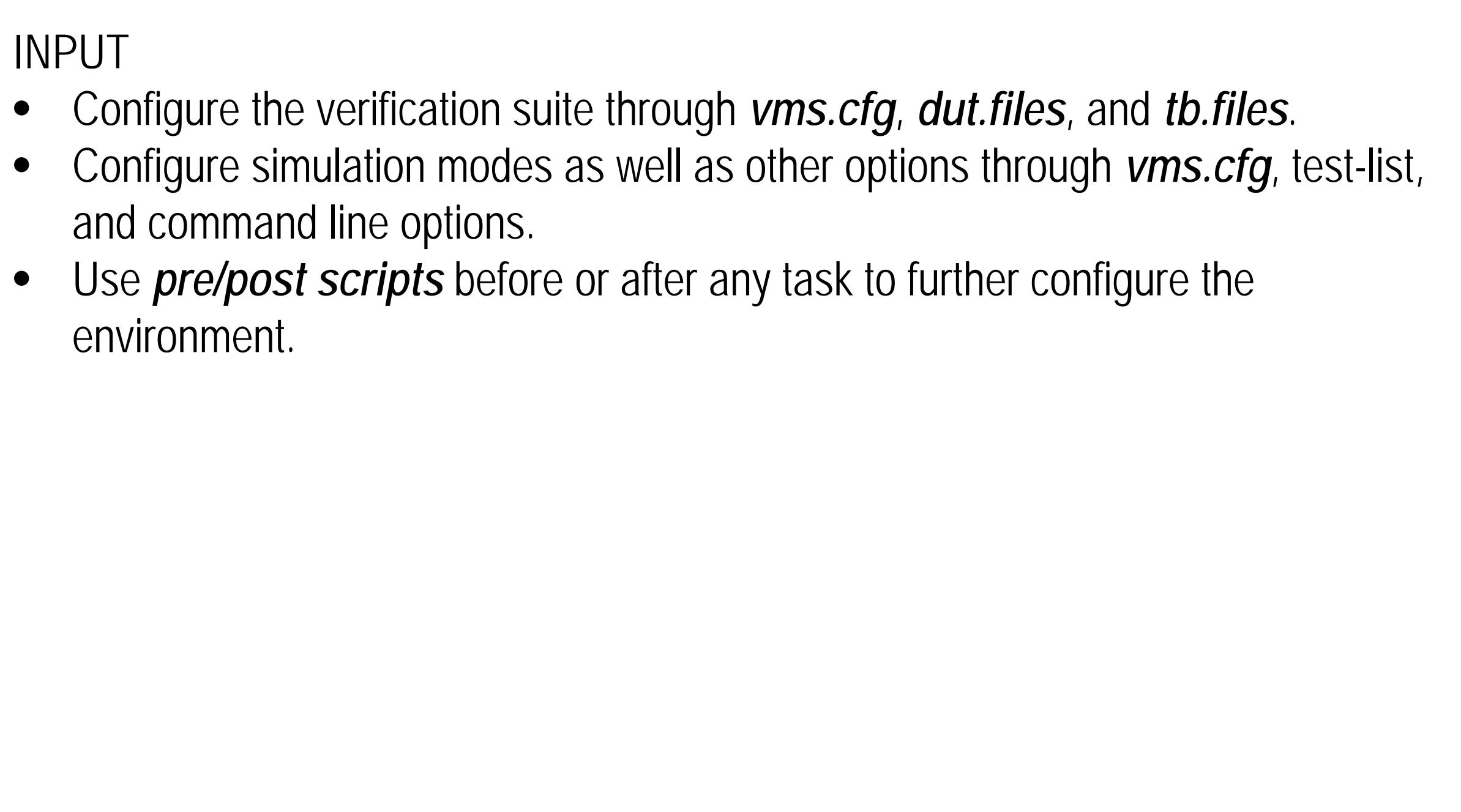


# Bringing Regression Systems into the 21<sup>st</sup> Century

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```
*** Compiling Design and Testbench Files ***
Compile 1 Pending Thu Jan 9 16:32:36 2014: Design files of DDC system for mode RTL
Compile 1 Started Thu Jan 9 16:32:40 2014: Design files of DDC system for mode RTL
Compile 1 Finished Thu Jan 9 16:32:48 2014: Design files of DDC system for mode RTL
Compile 2 Pending Thu Jan 9 16:32:21 2014: Testbench files of DDC system in subdir /tb/fnv for mode RTL
Compile 2 Started Thu Jan 9 16:32:25 2014: Testbench files of DDC system in subdir /tb/fnv for mode RTL
Compile 2 Finished Thu Jan 9 16:32:31 2014: Testbench files of DDC system in subdir /tb/fnv for mode RTL

*** Preparing Simulation Database. This may take a moment. ***

```

```
*** Starting Tests ***
Test 1 Pending Thu Jan 9 16:33:09 2014: 01_rand/01_rand RTL
Test 2 Pending Thu Jan 9 16:32:49 2014: 02_move/test/test RTL
Test 1 Started Thu Jan 9 16:32:42 2014: 01_rand/01_rand RTL
Test 2 Started Thu Jan 9 16:32:43 2014: 02_move/test/test RTL
Test 1 Finished Thu Jan 9 16:33:06 2014: 01_rand/01_rand RTL
Status: Passed
Test 3 Pending Thu Jan 9 16:33:06 2014: group2/01_rand/01_rand RTL
Test 2 Started Thu Jan 9 16:33:08 2014: 02_move/test/test RTL
Test 4 Pending Thu Jan 9 16:33:09 2014: group2/02_move/02_move RTL
Test 1 Merge Started Thu Jan 9 16:33:09 2014: 01_rand/01_rand RTL
Test 3 Started Thu Jan 9 16:33:09 2014: group2/01_rand/01_rand RTL
Test 2 Merge Complete Thu Jan 9 16:33:13 2014: 01_rand/01_rand RTL
Test 4 Started Thu Jan 9 16:33:14 2014: 02_move/test/test RTL
Test 2 Merge Complete Thu Jan 9 16:33:14 2014: 02_move/test/test RTL
Test 3 Finished Thu Jan 9 16:33:39 2014: group2/01_rand/01_rand RTL
Status: Passed
Test 3 Merge Started Thu Jan 9 16:33:45 2014: group2/01_rand/01_rand RTL
Test 4 Finished Thu Jan 9 16:33:45 2014: group2/02_move/02_move RTL
Sim File: ./moss_dac2/dac/MXGVerificationExamples/top1.2/top/system/tb/fnv/run/tests/group2/02_move/02_move RTL/moss_dac2/dac/MXGVerificationExamples/top1.2/top/system/tb/fnv/run/tests/group2/02_move/02_move RTL.log
Test 3 Merge Complete Thu Jan 9 16:33:45 2014: group2/01_rand/01_rand RTL
Test 4 Merge Started Thu Jan 9 16:33:50 2014: group2/02_move/02_move RTL
Status: Passed
*** 60% completion ***
Test 4 Merge Complete Thu Jan 9 16:33:50 2014: group2/02_move/02_move RTL
*** 100% completion ***

```

Summary Test Results Are:  
 Tests Passing: 3 75.00%

Regression details

Regression Stats	Stat	Value
Main Active Tests	1	
Avg Active Pkt Run	0	
Avg Active Main Run	1	

Test Results

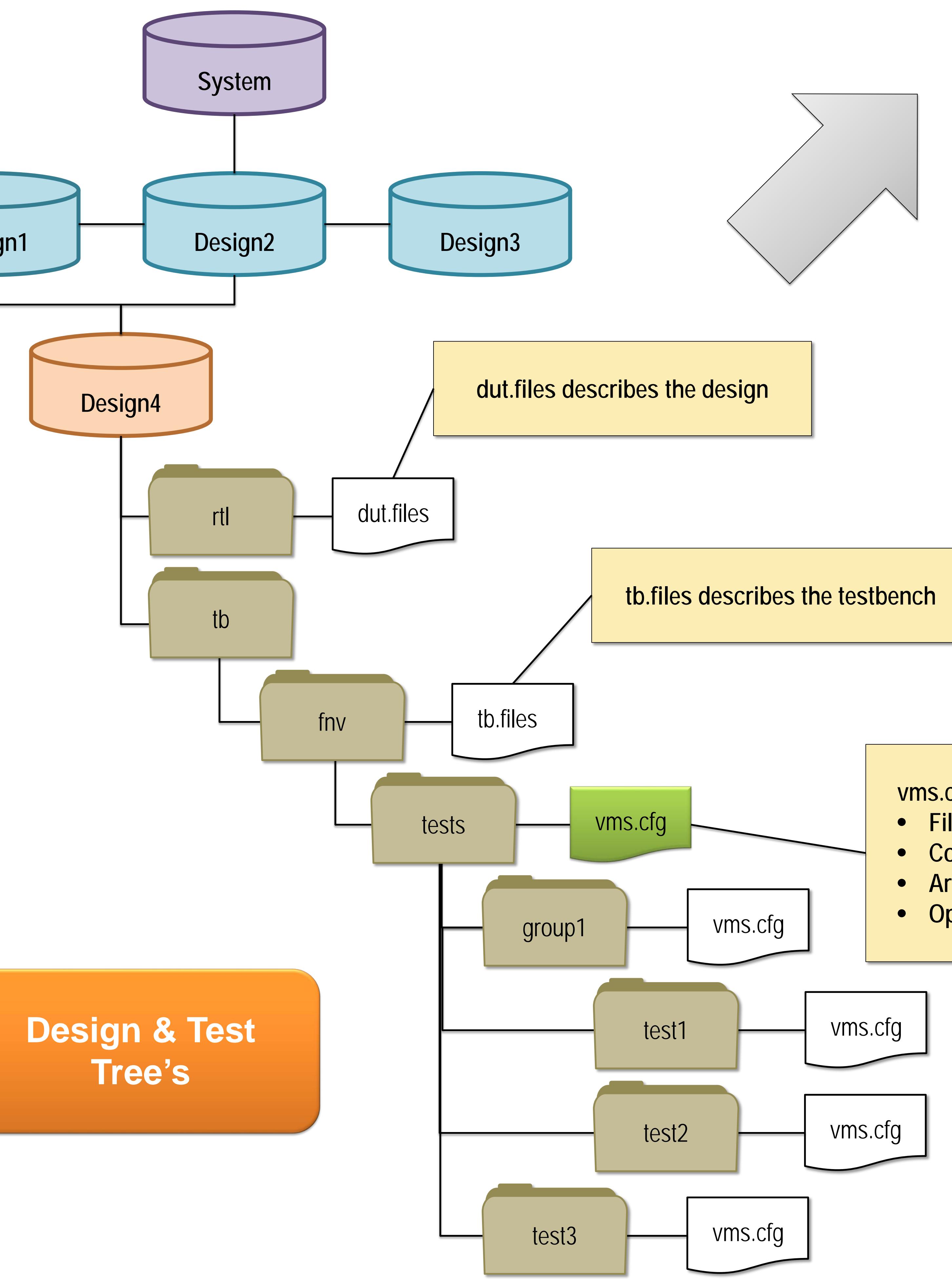
Testname (mode) (seed)	Status	ESF Job ID	Host CPU	CPU(T)	Wall Clock Times	Sim Virtual Memory(KB)	Sim Working Memory(KB)	Completion Time	
01_rand/01_rand RTL	Complete	721894	lbor9t	0.045497	0.000000000	45204	0.000000000	WedJan 29 15:48:00 2014	
02_move/test/test RTL	Complete	721895	lbor9t	0.045889	0.111780	24000000000	82164	WedJan 29 15:59:00 2014	
group2/01_rand/01_rand RTL	Complete	721896	lbor9t	0.049993	0.082629	30000000000	82168	45204	WedJan 29 15:59:10 2014
group2/02_move/02_move RTL	Complete	721897	lbor9t	0.002000	0.003	0.000000000	67832	37304	WedJan 29 16:00:20 2014

Profile of active tests in full run (until last test ended)

Active Frequency	1	2
Profile of active tests in main run (until last test started)	1	2

Active Frequency

1	2
---	---



**Design & Test Tree's**

**Ranked Reusults**

	Original Results			Ranked Results			CPU Perf Savings
	No. Tests	cvg	CPU(T)	No. Tests	cvg	CPU(T)	
Des1	25	99.7%	4 hr	16	99.7%	2 hr	50%
Des2	2622	99.9%	22.4 hr	306	99.9%	2.2 hr	90%
Des3	146	97.4%	16.4 hr	41	97.4%	8.94 hr	46%
Des4	45	99.9%	3.6 hr	28	99.9%	2 hr	46%