Boosting Debug Productivity Practical Applications of Debug Innovations in a UVM World

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SYNOPSYS[®]







Motivation

Efficient SV/UVM Testbench Debug

Rapid Root-Cause Analysis with Reverse Debug

Search-centric Debug with OneSearch

Embedded SW Debug





Verification Complexity Exponentially Increasing





CONFERENCE AND EXHIBITION

Scope of Debug Expanding









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Search-centric Debug with OneSearch

Embedded SW Debug





Testbench Debug Complexity





ESIGN AND VEF

Debug Testbenches Interactively

Full-visibility Testbench Debug in Verdi & VCS



- On-demand Debug
- Step forward/back/into testbench constructs
- Go back in time without restarting simulation OR setting checkpoints
- Full Visibility

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- Source code, dynamic objects, watch list etc.
- Call stack, members, local variables etc.
- Powerful Capabilities
- Trace value assignment into testbench
- Perform what-if analysis
- Enable day-to-day and batch simulation debug
 2017

DESIGN AND VERIFICATION

ELROPE



Key Elements for Efficient SystemVerilog TB Debug









2017

CONFERENCE AND EXHIBITION

EUROPE





Simulation Control & TB Behavior Tracking











Making Debug UVM Aware

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🚽 🍺 scoreboard0	xbus_demo_scoreboard	@1	0	28
🖻 🍺 xbus0	xbus_env	@1	0	28
🖭 🍺 bus_monitor	xbus_bus_monitor	@1	0	28
🖨 🍺 masters	xbus_master_agent[]			
🖃 🍺 [0]	xbus_master_agent	@1	0	28
🗌 🎯 driver	xbus_master_driver	@1	0	28
🖭 🍺 monitor	xbus_master_monitor	@1	0	28
🕀 🍺 sequencer	xbus_master_sequencer	@1	0	28
표 🍺 [1]	xbus_master_agent	@2	0	28
🖻 🍺 slaves	xbus_slave_agent[]			
🖭 🍺 [0]	xbus_slave_agent	@1	0	28
🕀 🍺 [1]	xbus_slave_agent	@2	0	28
🕀 🍺 [2]	xbus_slave_agent	@3	0	28
🕀 🍺 (3)	xbus_slave_agent	@4	0	28
🖭 🍺 [4]	xbus_slave_agent	@5	0	28
🕀 🍺 [5]	xbus_slave_agent	@6	0	28
± 🍺 [6]	xbus_slave_agent	@7	0	28
÷ 🔒 [7]	xbus slave agent	@8	0	28





Buried in logfiles?



There has to be a better way to browse data across all these logs!

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SmartLog to the Rescue

- Smart browsing of log files
 - Hyperlinks
 - Message filtering: UVM, VCS, Severity...
 - Time visualization and navigation
 - Message navigation
 - File view or structure view
 - Searching and text based filtering
 - Customize and add own log parsing rules (for custom log files)



SmartLog – File View

SmartLog							🖋 🖅 🗕 🗆 🗙
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2645 [O] integral	6,510	Info	UVM_INFO xbus_demo_	scoreboard.sv(75) 🖞 65	510: UY	/m_test_top	op.xbus_demo_tb0.scoreboard0 [xbus_demo_scoreboard] READ to existing addressChecking addre
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2651 begin_time time			addr	integral	16	'h12	
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2655 UVM INFO © 6510: UVM test top.xbus demo th	6,510	Info	[0]	integral	8	'h12	
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Message Interactive Console OneSearch SmartLog			end_time	time	64	6510	
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	-						DESIGN AND VÈRIEICATION™



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Motivation

Efficient SV/UVM Testbench Debug

Rapid Root-Cause Analysis with Reverse Debug

Search-centric Debug with OneSearch

Embedded SW Debug





Productivity with Reverse Debug



Finding Failures

Diagnose and Debug - Moving forward and backward in time





What-if Analysis

Fix and Validate in One Simulation



Regression Debug



Interactive Debug Flows

Interactive debug for both day-to-day and batch simulation tasks

1. User runs and debugs interactive simulation in Verdi

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2. User runs batch/interactive simulation, saves sessions, later restores sessions and debugs interactively





Verdi Reverse Debug













Motivation

Efficient SV/UVM Testbench Debug

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Search-centric Debug with OneSearch

Embedded SW Debug





Search Queries...



Now, how would designers and verification engineers like to search?

2017

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OneSearch

A single search for the entire verification environment

- Single and simple user interface
- Fast search engines



Using Verdi OneSearch





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Verdi OneSearch









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Motivation

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Embedded SW Debug





SoC Debug Challenges

Lack of Visibility on the Software Side





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SoC Debug Challenges

Lack of Visibility on the Software Side





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Verdi HW SW Debug

- Enables co-debug between HW and SW
- HW and SW debug synchronized in time
- View C/Assembly source, C variables, stack, memory
- Debugs multiple cores simultaneously
- Simulation supports all ARM[®] Cortex[®] cores
- Easy to support additional cores or custom cores







Embedded Software Debug in Eclipse



Provides programmer's view of code running on simulated processor

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Combined HW and SW Debug







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Debugging Multi-Core



Provides programmer's views into multiple cores simultaneously

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No modifications needed - Enable CPU log during simulation

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Verdi HW SW Debug









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Verdi HW SW: Getting Started





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Summary



Interactive Debug

- Full-featured, full visibility debug for SV/UVM testbench
- Run forward and backwards for improved debug efficiency

OneSearch

- Fast and efficient search
- Search entire verification environment at once

SmartLog

- Organized logs in table format with time and other filters
- Parse logs with hyperlinks to source

HW SW Debug

- Synchronized HW and SW debug
- Multi-core support
- Performance profiling and embedded SW code coverage







Motivation

Efficient SV/UVM Testbench Debug

Rapid Root-Cause Analysis with Reverse Debug

Search-centric Debug with OneSearch

Embedded SW Debug





References

- Synopsys Verification Home <u>https://www.synopsys.com/verification.html</u>
- Synopsys Verdi Debug Platform <u>https://www.synopsys.com/verification/debug.html</u>
- Synopsys Verdi HW/SW Debug <u>https://www.synopsys.com/verification/debug/verdi-hw-sw-debug.html</u>





