Automating Netlist Modifications required by Functional Safety

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INTRODUCTION (or REQUIREMENTS)

Developing semiconductor products targeted towards a functional safety application impose an additional set of challenges for the involved development teams. Requirements like "freedom of interference", redundant execution and cross-checking of functionality, as well as countermeasures for possible common cause failures need to be taken into account for every step of the design cycle. The implementation of corresponding features and the reuse of IP and subsystems/platforms involves often netlist modifications of non-trivial nature; i.e. new or modified hierarchy levels, additional device modes, and the insertion of additional logic or logic blocks.

Functional safety standards, like the ISO26262 for the Automotive Industry, require a high degree of repeatability of the corresponding work. Here, the early adoption of the IP-XACT standard for netlist assembly allowed us to exploit related benefits for several earlier products. The most recent family of safety devices developed by Freescale™ for one automotive customer is extending on these capabilities. Automation of further netlist modifications is employed to implement many safety relevant features, like logic built-in-self-test (LBIST), online memory built-in self-test (MBIST), independent physical hierarchies and their separation by X-bounding, as well as the required bypass and comparison logic.

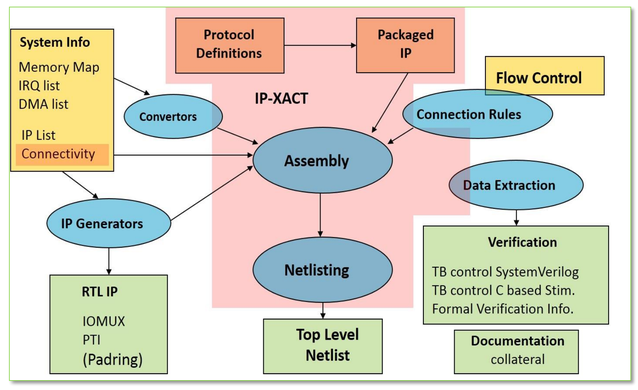

INTERNATIONAL STANDARD
ISO 26262-1
First edition 2011-11-15
Road vehicles — Functional safety —
Part 1: Vocabulary
Véhicules routiers — Sécurité fonctionnelle —
Partie 1: Vocabulaire

Vendor independence is another benefit of using an industry standard like IP-XACT. It enables easier extension of the required capabilities but also enabled a faster switching between tool vendors.

OBJECTIVES

Semiconductor devices targeting an application in the area of functional safety often provide or implement some specific features or functionality. The intention of those features is in many cases a better or easier detection of faults that might lead to a malfunction of the device. Other features might support fault avoidance or be beneficial to prevent failures that could not be detected or avoided otherwise.

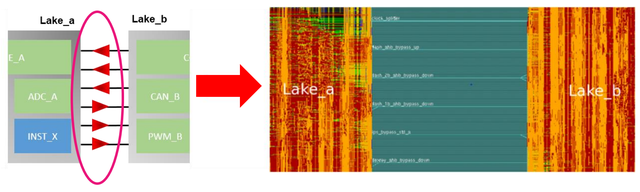
Systems targeted towards applications in the field of functional safety have always required a rigid, well organized and structured design style to ensure a repeatable and well documented development effort. The benefits of automated netlist generation, and the increased reuse capabilities, have led to an early adoption of the IP-XACT standard for several aspects of the development work within our organization.

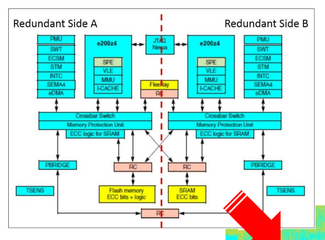


The flexibility of this standard makes it suitable for many areas of design work; the most common one is for netlist generation and for processing and maintaining register descriptions, e.g. for header file generation and memory map definition. We describe the experiences when further extending an already automated development step, the netlist assembly, with additional capabilities that are required due to the system targeting an application in the field of functional safety.

OBJECTIVES

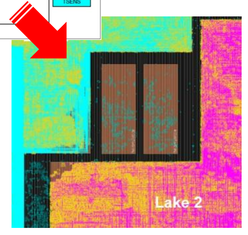
- Extend an existing IP-XACT based netlist generation flow to generate the additional design elements required to fulfill functional safety specific requirements:
- Modify existing deliverables to make them compliant with functional safety architecture needs:
  - ➢ Insertion of buffers to decouple Lakes.
  - ➢ Insertion of additional logic required for "X-bounding" of an LBIST partition.
  - ➢ Modify or insert additional hierarchies.
    - Required for definition of Lakes.
    - Required for logic BIST implementation.

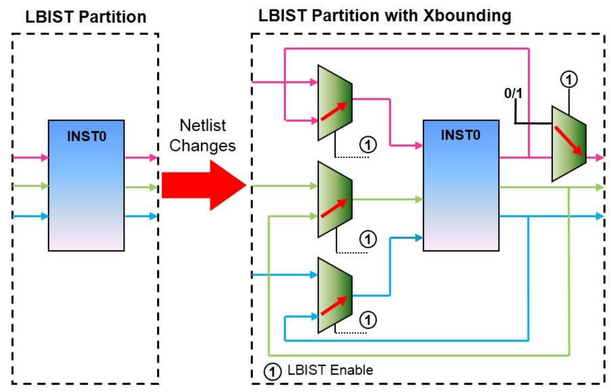




Additional logic must be inserted between the lakes/partitions to decouple internal logic from external influences

Redundant elements must be located in different lakes to minimize possibility of common cause failures



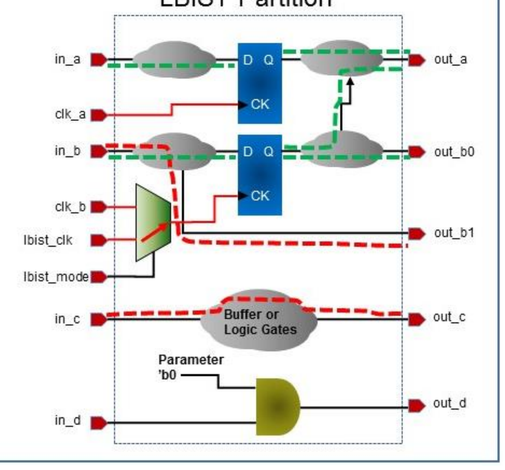


EXAMPLE: X-BOUNDING FLOW

- Identify and confirm clocks, resets, and required mode selection input settings.
- Extracting structural information from the RTL netlist via a 3rd party tool.
- Determine input and output cone for every FF, as well as feedthrough paths.
- Parse the resulting report to create additional logic/connectivity required for the X-bounding of this LBIST partition; re-read design; subsequent verification is then performed on the full-chip:
  - ✓ Using logic equivalence checks to verify that the X-bounding did not alter the functional mode.
  - ✓ Logic BIST mode is verified by injecting X at the interfaces while running a logic BIST simulation.

Flow permits incremental refinements

```
=======================================
=  Clock Domain Crossing Check (Summary)
=======================================
|      Source --> Destination
| -------------------------------
| -from PI
| in_a --> clk_a                    Path type: data
| in_b --> lbist_clk                Path type: data_feedthrough
| in_b --> out_b1                   Path type: feedthrough
| in_c --> out_c
| -to PO
| clk_a --> out_a                   Path type: data
| in_b --> out_b1
| in_c --> out_c                    port can be associated to n clocks
| lbist_clk --> out_a               Path type: data
| lbist_clk --> out_b0              Path type: data
```



CONCLUSIONS

The implementation of safety requirements within a semiconductor device requires complex and massive manipulations of the RTL database. The expectation of functional safety standards on the development process is a repeatable and state-of-the-art implementation with high quality results:

- ➢ IP-XACT interfaces allow a significant reduction of connectivity data by bundling several signals to a single interface connection. Connection rules included in interfaces can be checked automatically. Incorrect connections can be reported at implementation time which reduces the verification effort.
- ➢ The usage of IP-XACT for the netlist assembly automation helps to increase design efficiency; enables repeatable implementation and further automation and reduces the possibility of manual errors.
- ➢ Complex netlist operations (e.g. hierarchy creation) can be performed quickly, repeatable and with high quality results.
- ➢ Partitioning of the design data (e.g. IP integration, clock/reset, analog, DFT, safety, debug) enables a parallel development approach. Concurrent development is supported and allows quick progress.
- ➢ Reuse of connectivity data and quick adaption of connection tables allows continuous improvement and fast generation of prototypes.

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