Automatic Firmware Verification for Automotive Applications

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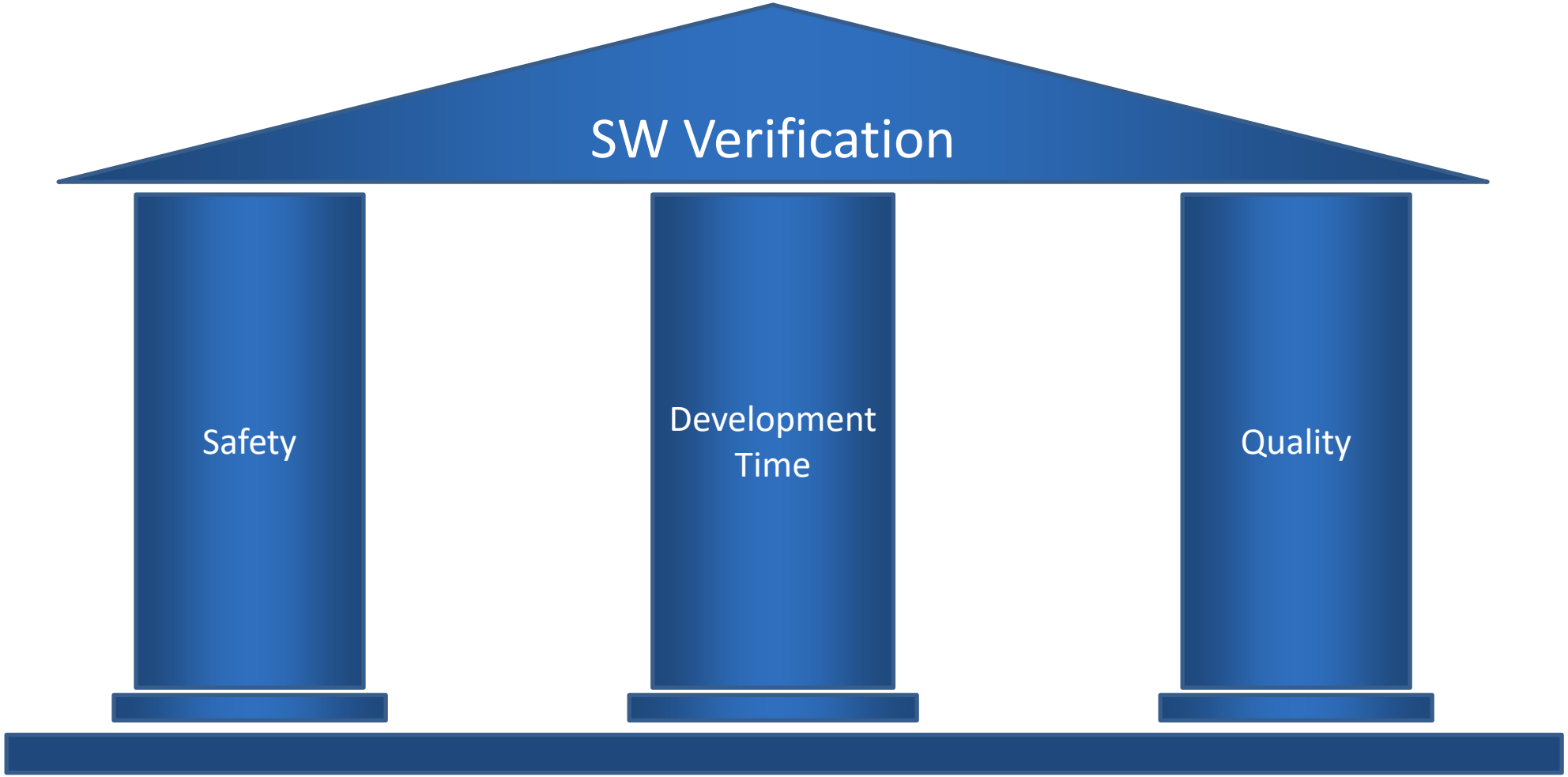
Motivation



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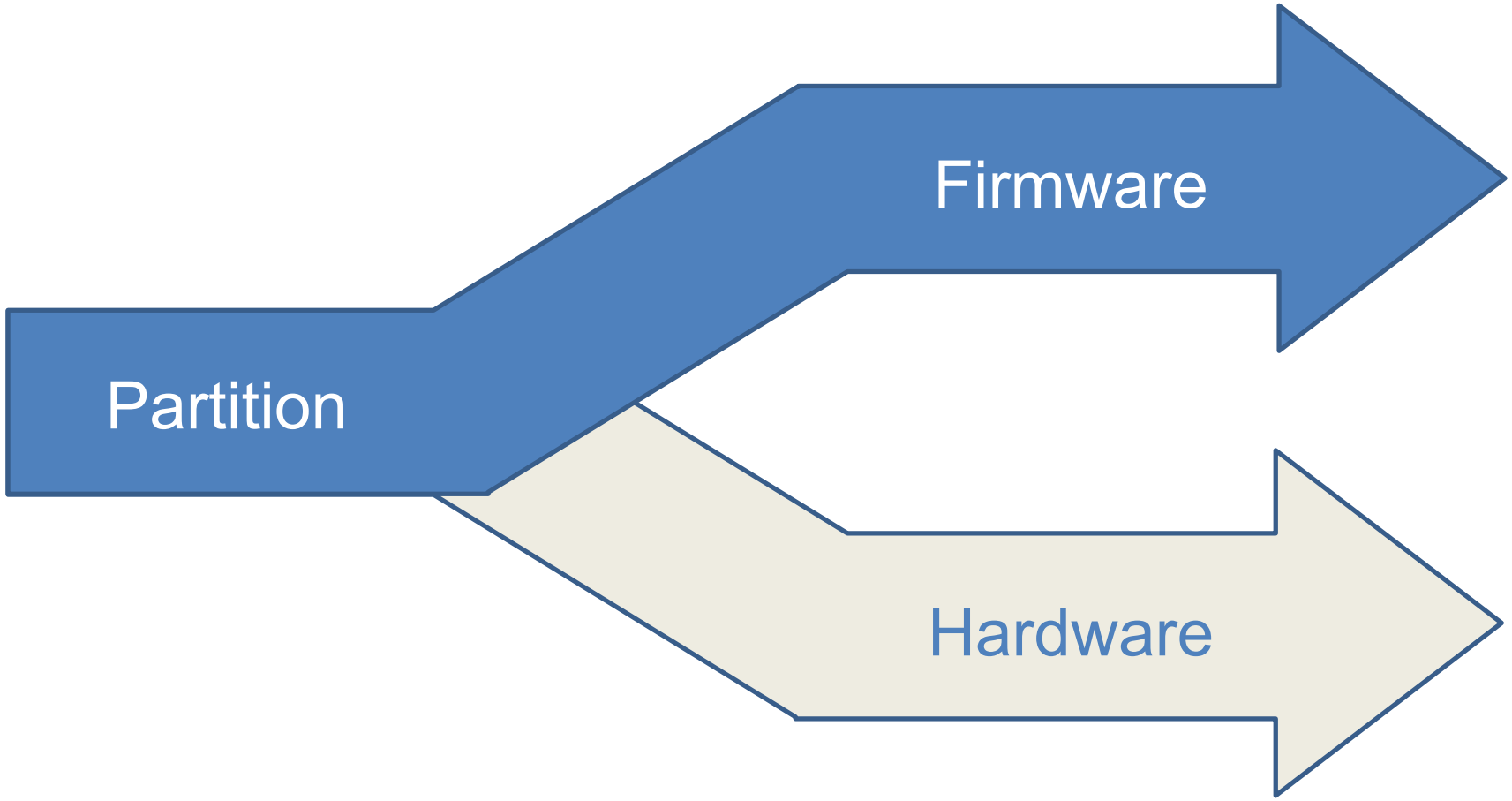
Development Time



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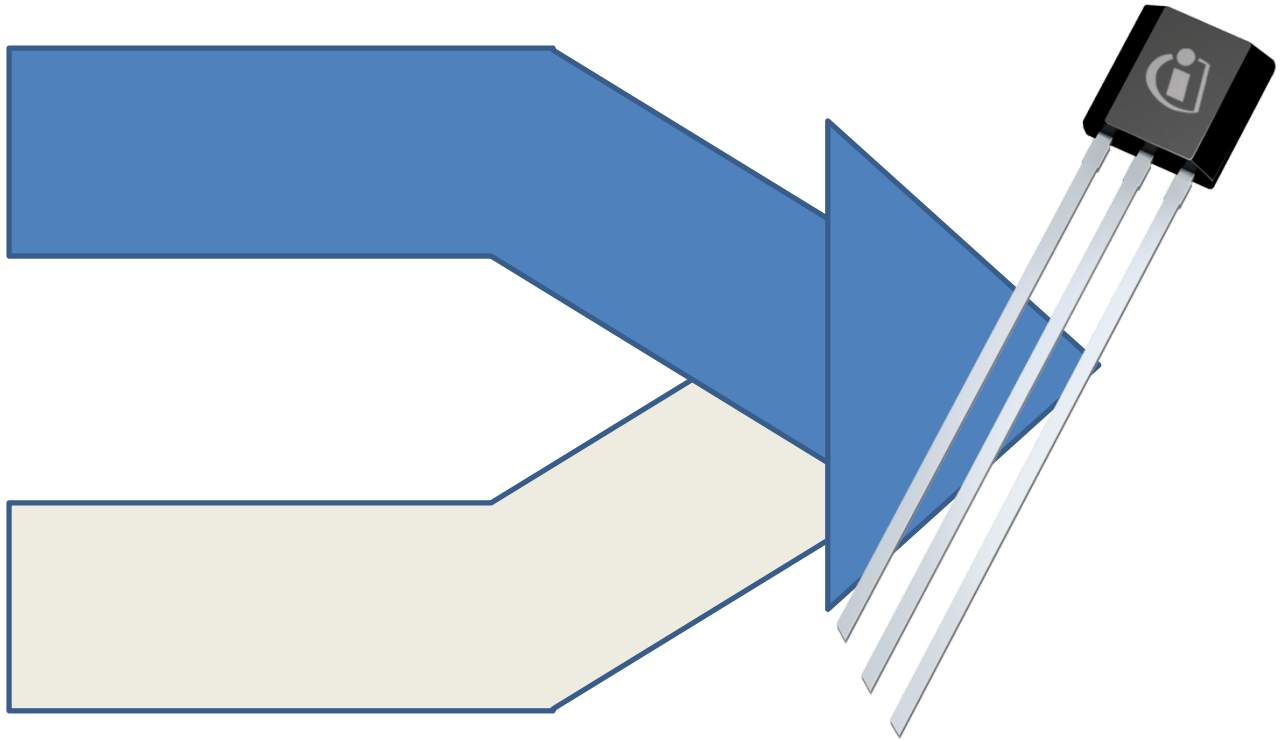
Parallel Development



- **Parallel** development
- **Influencing** development
  - Confirm feasibility of partitioning
  - React quickly if unfeasible

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Quality of Verification

- Functional requirements
  - Behavior
  - Non-behavior
- Non-functional requirements
  - Resource constraints (e.g. timing, memory size)

✓ Fault tolerant time interval (FTTI)

✓ Timing Limitations
- Processing delay
- Acceptable jitter
- Refresh rates

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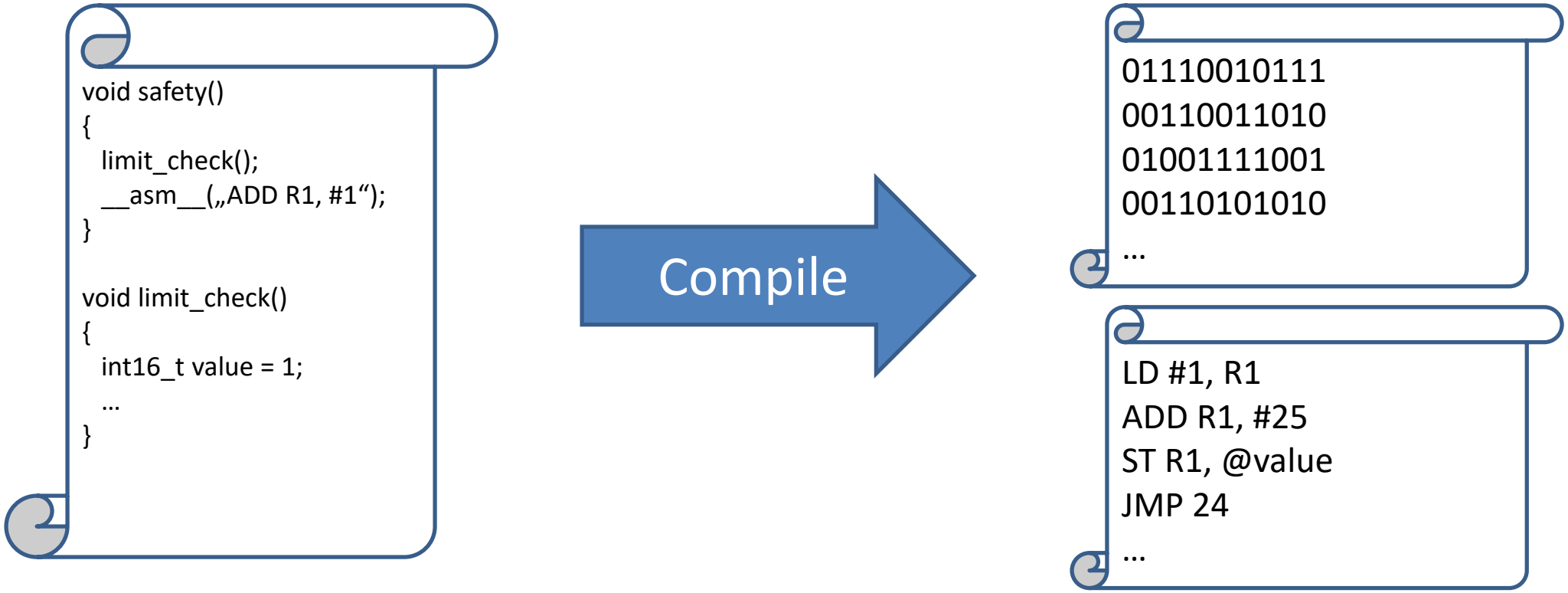
Host vs. Target Verification



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ISO 26262

ISO 26262-6:2011 9.4.6

"The test environment for software **unit testing** shall correspond as closely as possible to the target environment. […]"

ISO 26262-6:2011 10.4.8

"The test environment for software **integration testing** shall correspond as closely as possible to the target environment. […]"

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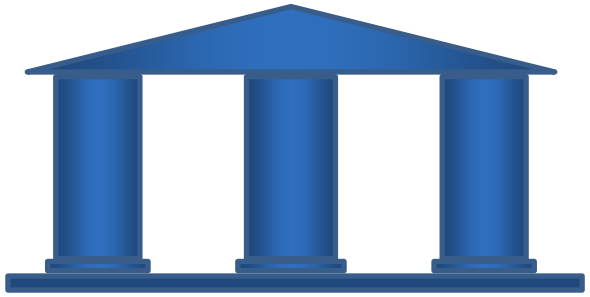
Implications in a Nutshell

Pro's Host Verification

- Many tools to choose from
- Verify C code



Pro's Target Verification

- Enable parallel development
- Non-functional requirement verification
- Supports verification of native assembler statements
- ISO 26262
- Verify machine code (do not depend on compiler)

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Evaluation Criteria

- Comprehensive verification
- Easy to use
- Low overhead
- Fast execution
- Support regression
- FW Unit verification
- FW Unit Integration verification
- Independent of hardware development
- High level of reuse
- Reliability tooling
- Simple result interpretation

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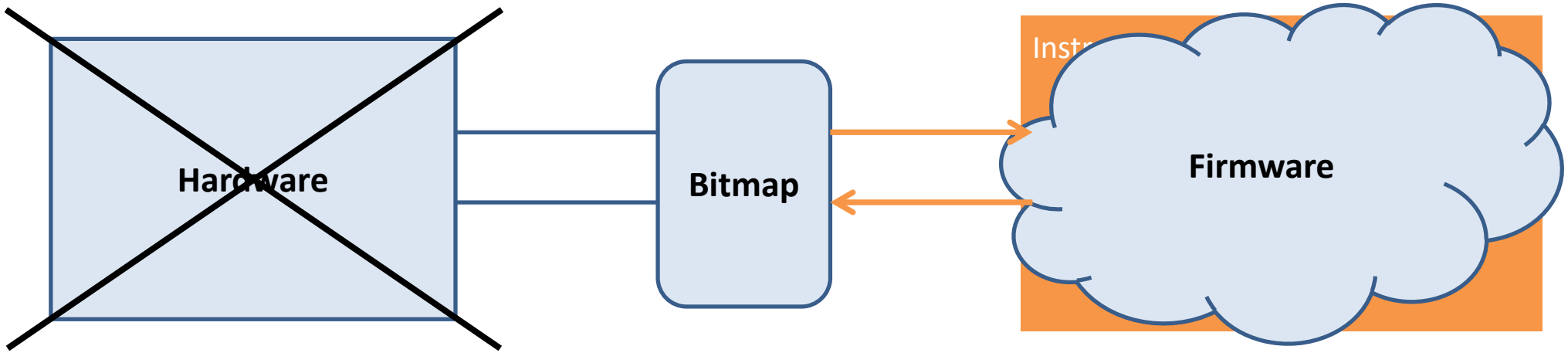
Hardware Abstraction

- **Bitmap:** All registers accessible by HW and FW



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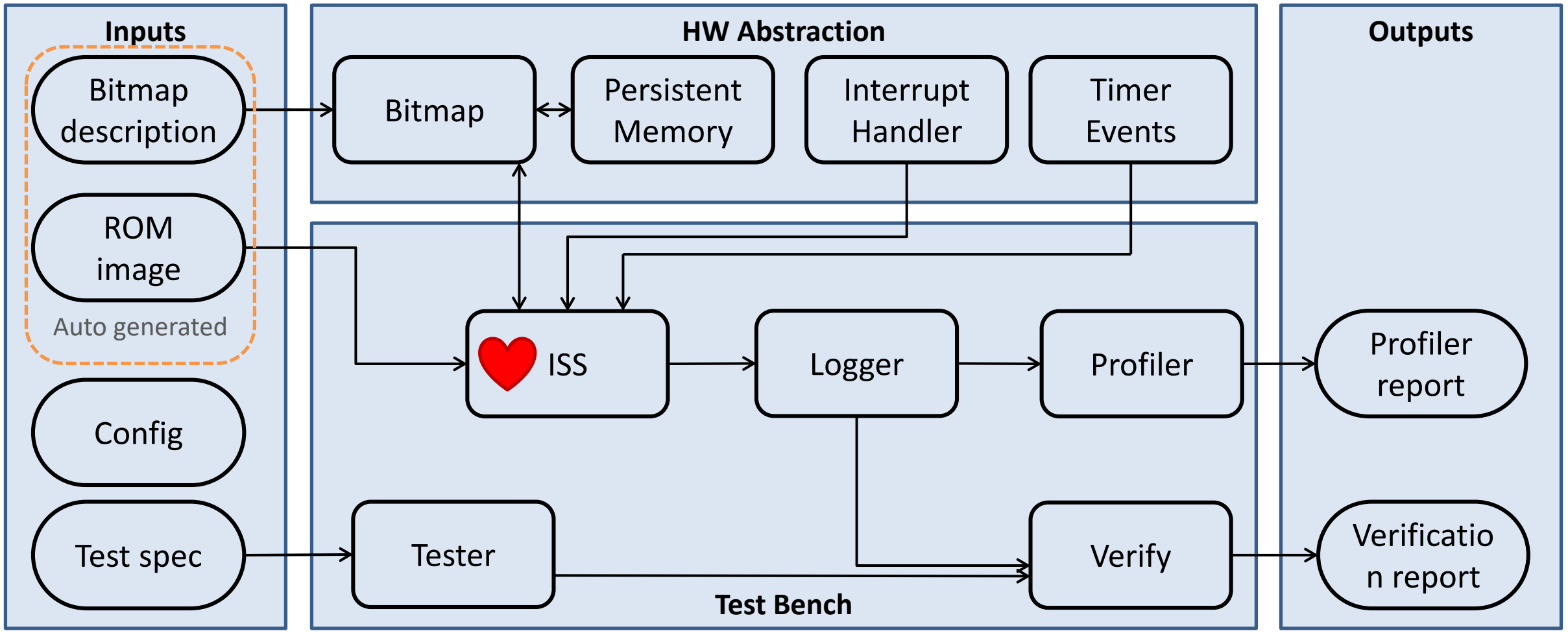
Verification Tool Architecture



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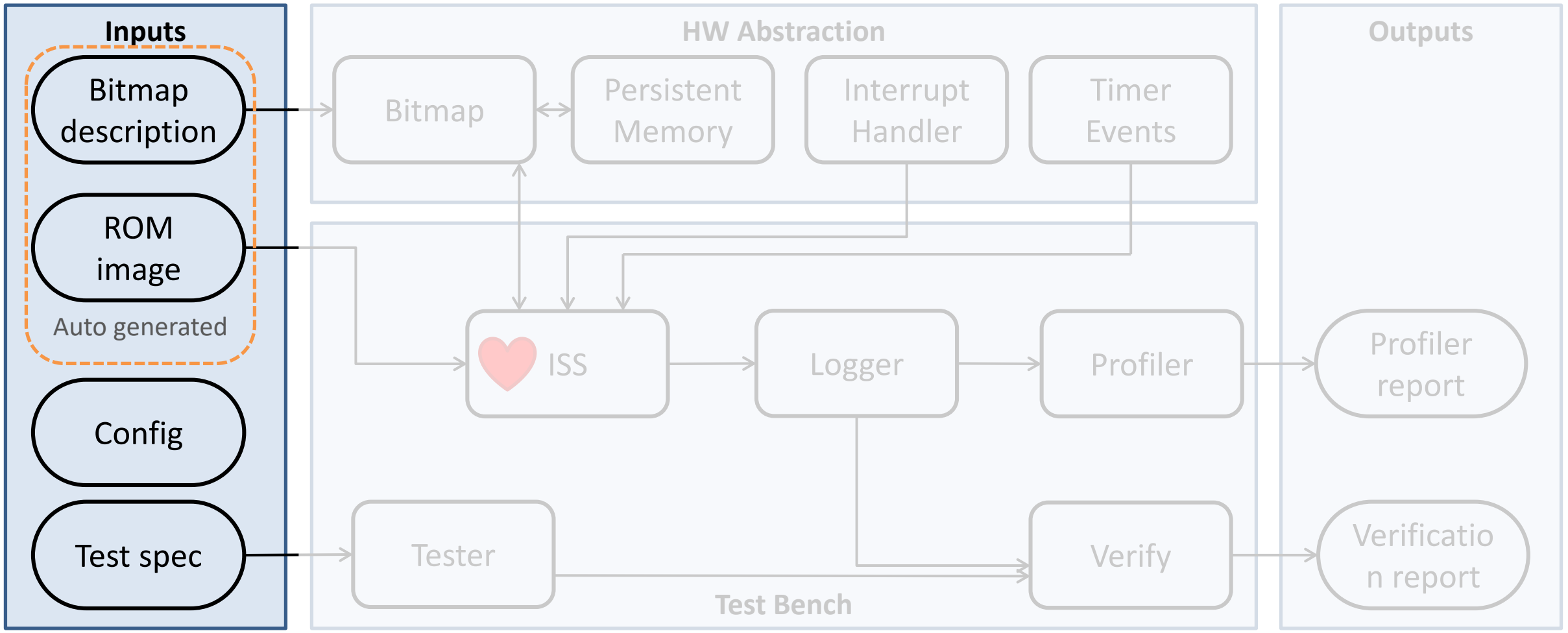
Verification Tool Architecture



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Inputs

- **Bitmap Description**
  - Register specification
  - Auto-generated from central specification
- **ROM image**
  - Binary FW image
  - Compiled from high level language
- **Config**
  - Project specific adaptation
  - Specified once per project

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Test Specification

- Input stimuli
- Expected values
- Test definition in Microsoft Excel
  - Well-known tool
  - Reliable libraries available to enable parsing by framework
  - Reference implementation using Excel formulas
  - CSV import from other tools for reference implementation (e.g. Matlab)

	A	B	C	D
1	Inputs			Expected Output
2	algo_value	Lower limit	Upper limit	Limit error
3	-15	-25	25	0
4	-35	-25	25	1
5	…	…	…	…

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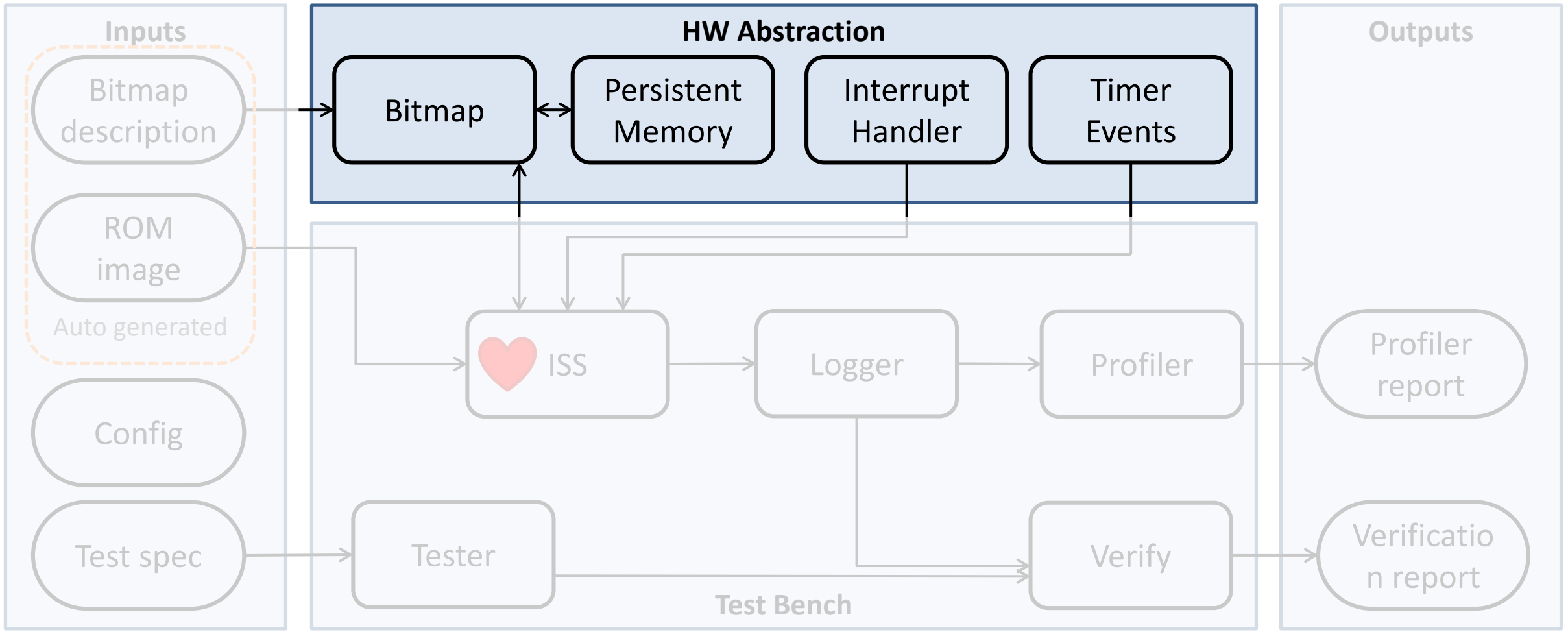
Verification Framework Architecture



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HW Abstraction

- **Bitmap**
  - Automatically generated from bitmap specification
- **Persistent memory**
  - Models specific behavior to retrieve data, e.g. EEPROM paging
- **Interrupt/Event handler**
  - Register behavior based on conditions/time

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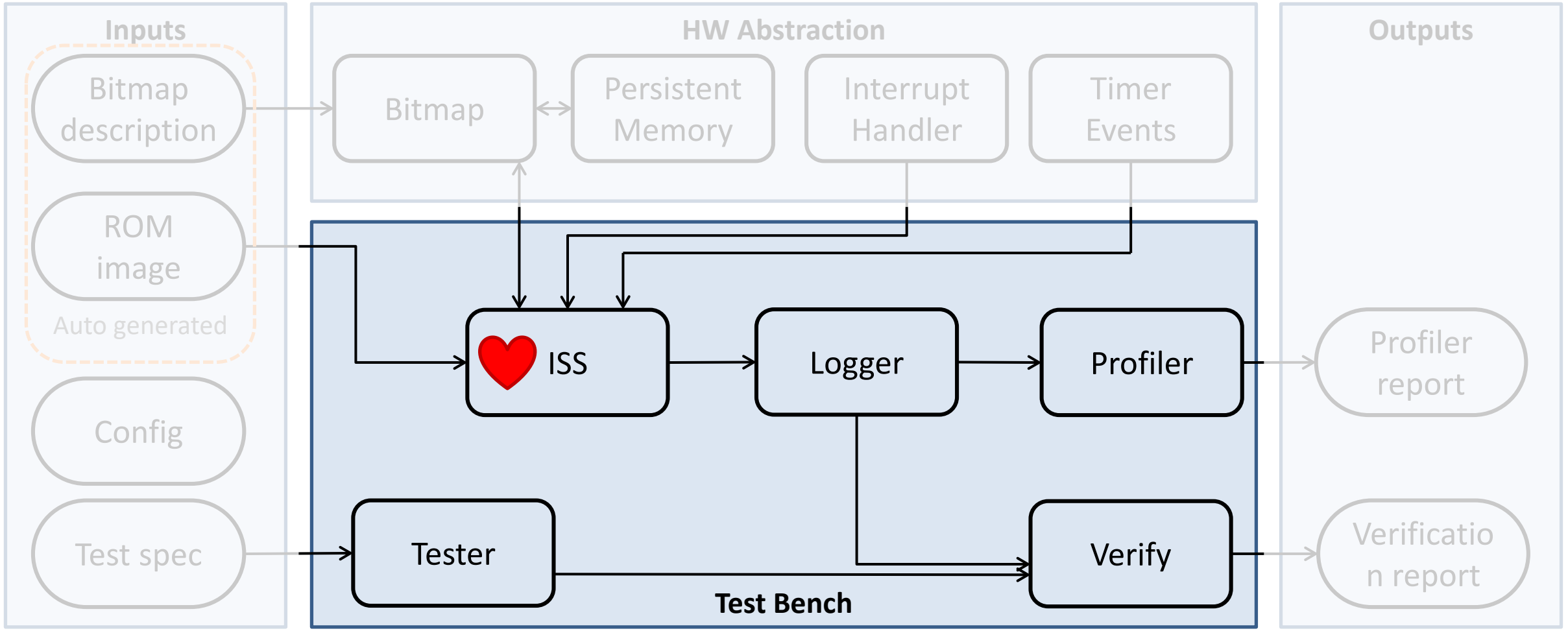
Verification Tool Architecture



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Test Bench

- **Instruction Set Simulator (ISS)**
  - Allows execution of native FW image
  - Cycle accurate
- **Tester**
  - User defined
  - Maps input stimuli to FW units

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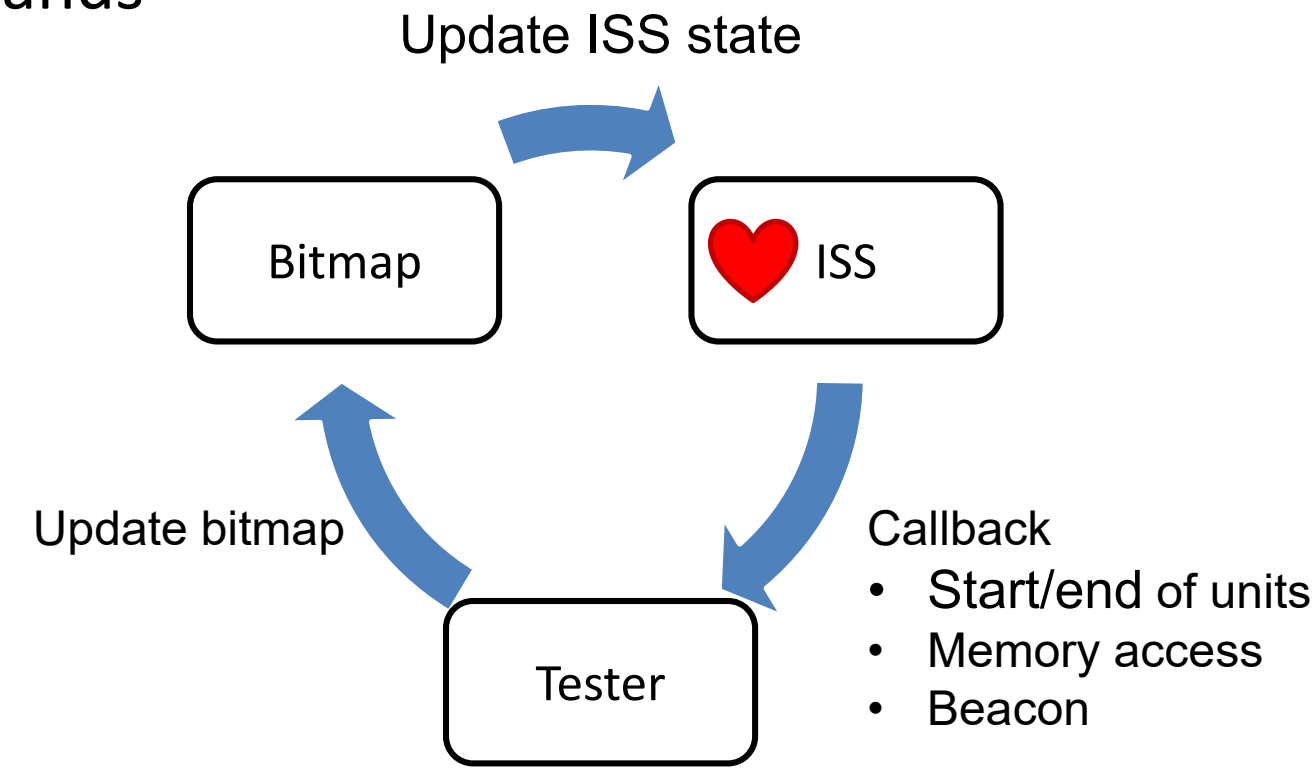
Instruction Set Simulator (ISS)

- FW enriched with triggers/commands

```
void safety()
{
  VERIFICATION_CMD(SAFETY_START);
  limit_check();
  regbist();
}

Void limit_check()
{
  VERIFICATION_CMD(LIMIT_CHK_START);
  int16_t a = GET(EEP1_LOWER_LIMIT);
  …
}
```



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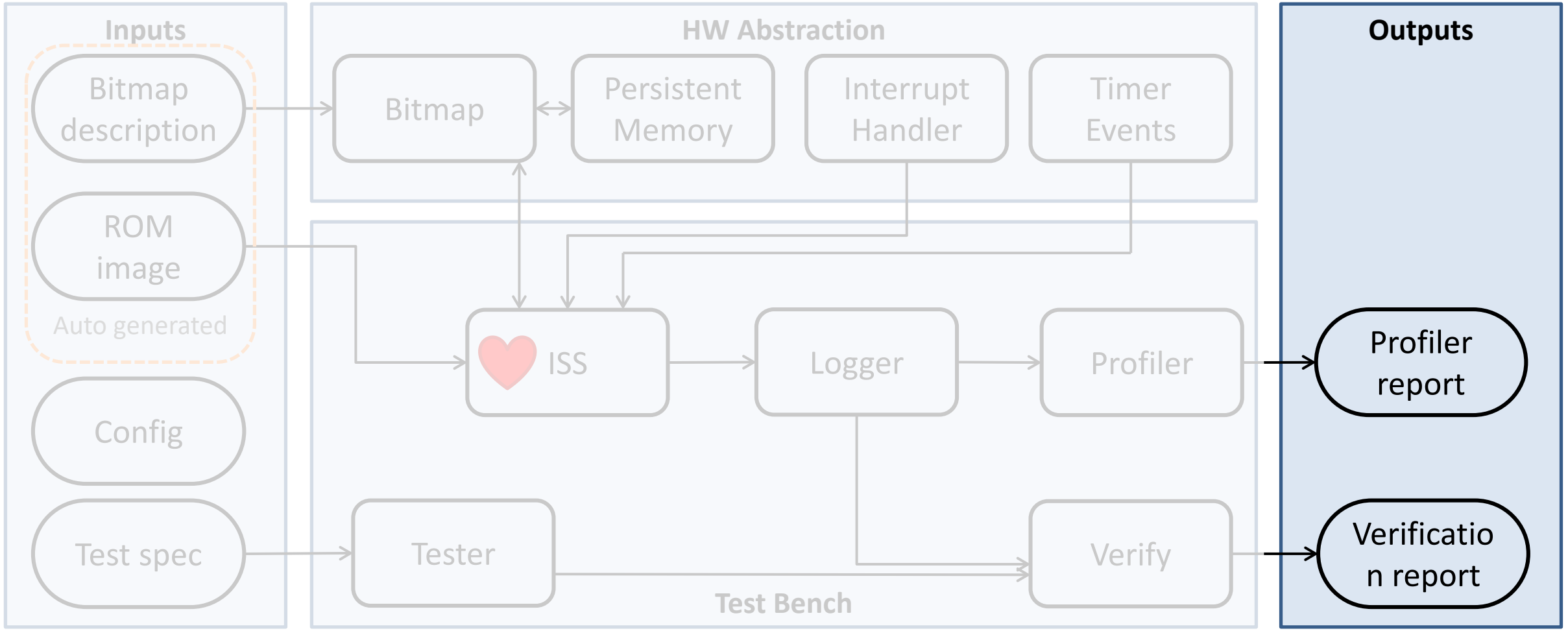
Verification Tool Architecture



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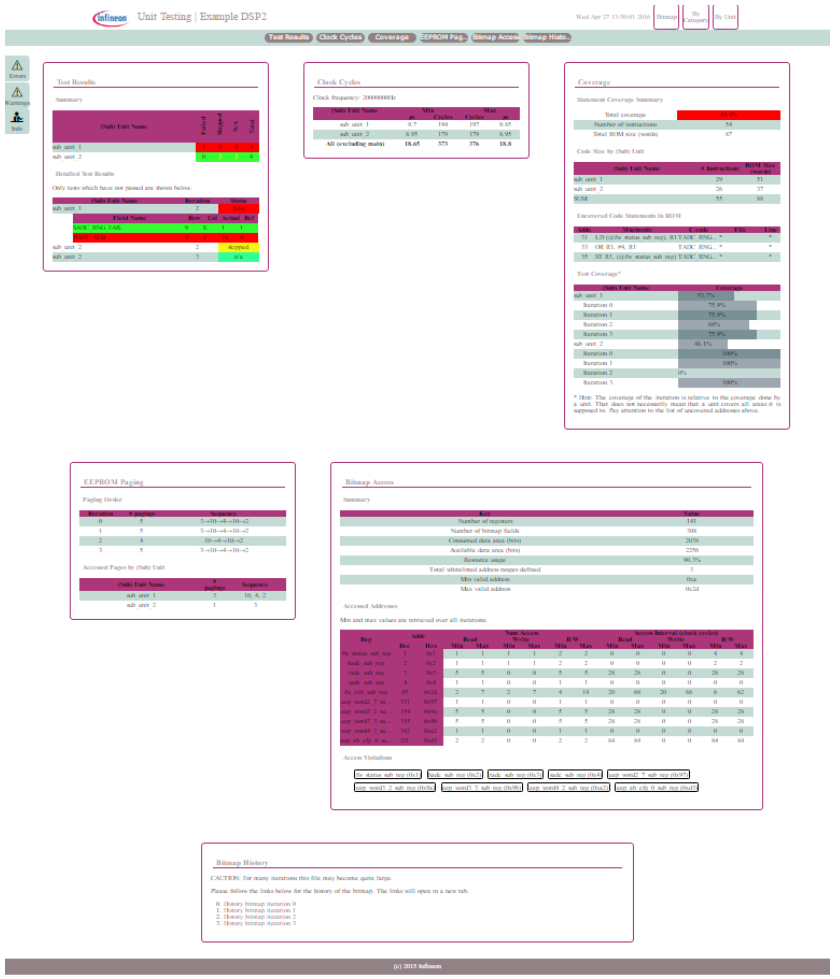
Outputs

- **Profiler Report**
  - Statement coverage
  - Branch coverage
- **HTML Verification Report**
  - Test summary (skipped, pass, fail)
  - Profiling information (# opcodes, execution time)
  - Access order to persistent memory
  - Bitmap access (when, how often, min/max interval)
  - Memory access violations



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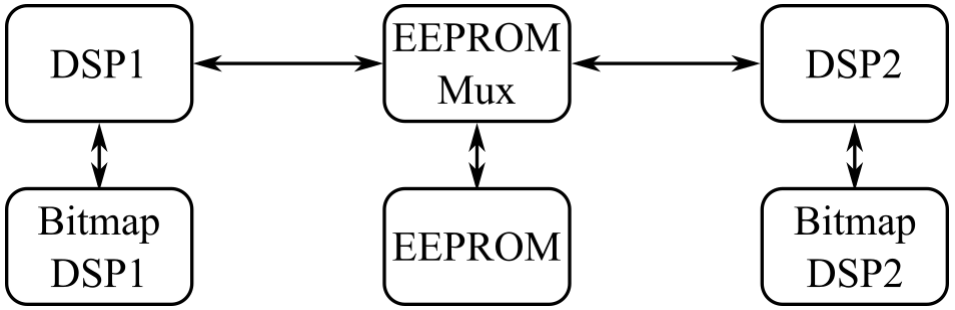
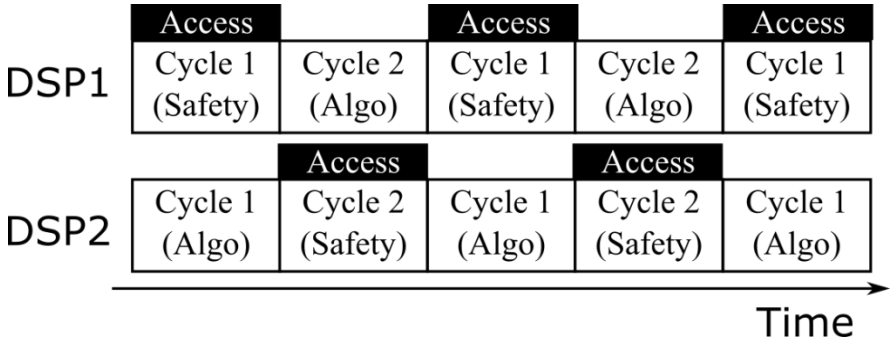
Application Example

- Application example in the paper
- Two units (algo, safety)





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Conclusions

- Verification tool for target architecture
- Safe and high quality verification
- Fast and parallel development

Questions

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